CMOS 4-BIT MICROCONTROLLER

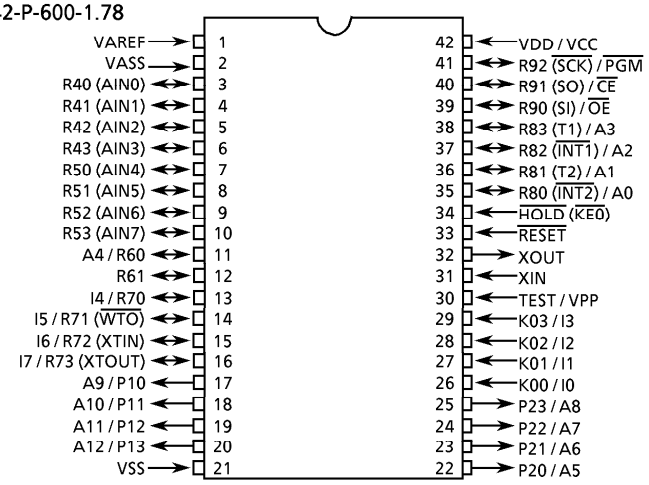
TMP47P840VN
TMP47P840VF

The 47P840V is the OTP microcontroller with 64Kbits PROM. For program operation, the programming is achieved by using with EPROM programmer (TMM2764AD type) and adapter socket.
The function of this device is exactly same as the 47C640/840.

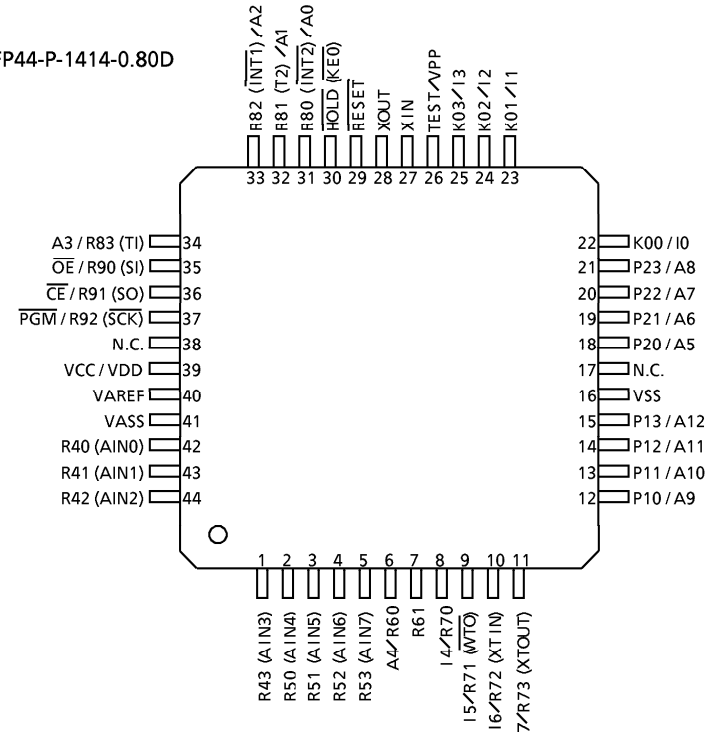
PART No.	ROM	RAM	PACKAGE	ADAPTER SOCKET
TMP47P840VN	OTP 8192×8-bit	512×4-bit	SDIP42-P-600-1.78	BM1171
TMP47P840VF			QFP44-P-1414-0.80D	BM1172

PIN ASSIGNMENT (TOP VIEW)

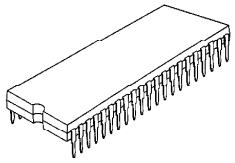
SDIP42-P-600-1.78



QFP44-P-1414-0.80D

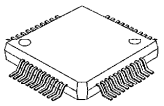


SDIP42-P-600-1.78



TMP47P840VN

QFP44-P-1414-0.80D



TMP47P840VF

PIN FUNCTION

The 47P840V has MCU mode and PROM mode.

(1) MCU mode

The 47C640/840 and the 47P840V are pin compatible (TEST pin for out-going test. Be fixed to low level.).

(2) PROM mode

PIN NAME	INPUT / OUTPUT	FUNCTIONS	PIN NAME(MCU mode)
A12 to A9	INPUT	Address inputs	P13 to P10
A8 to A5			P23 to P20
A4			R60
A3 to A0			R83 to R80
I7 to I4	I/O	Data outputs (Inputs)	R73 to R70
I3 to I0			K03 to K00
$\overline{PGM}$	Input	Program control input	R92
$\overline{CE}$		Chip Enable input	R91
$\overline{OE}$		Output Enable input	R90
VPP	Power supply	+ 12.5V / 5V (Program supply voltage)	TEST
VCC		+ 5V	VDD
VSS		0V	VSS
R43 to R40	I/O	Be fixed to low level	
R53 to R50			
R61			
$\overline{RESET}$	Input	PROM mode setting pin. Be fixed to low level.	
$\overline{HOLD}$	Input		
XIN	Input	Resonator connecting pin	
XOUT	Output		
VAREF	Power supply	Be fixed to low level	
VASS			

OPERATIONAL DESCRIPTION

The following is an explanation of hardware configuration and operation in relation to the 47P840V. The 47P840V is the same as the 47C640/840 except that an EPROM or OTP is used instead of a built-in mask ROM.

1. OPERATION mode

The 47P840V has an MCU mode and a PROM mode.

1.1 MCU mode

The MCU mode is set by fixing the TEST/VPP pin at the "L" level. Operation in the MCU mode is the same as for the 47C640/840, except that the TEST/VPP pin does not have built in pull-down resistor and cannot be used open.

1.1.1 Program Memory

The program storage area is the same as for the 47C840. Data conversion tables must be set in two locations when using the 47P840V to check 47C640 operation.

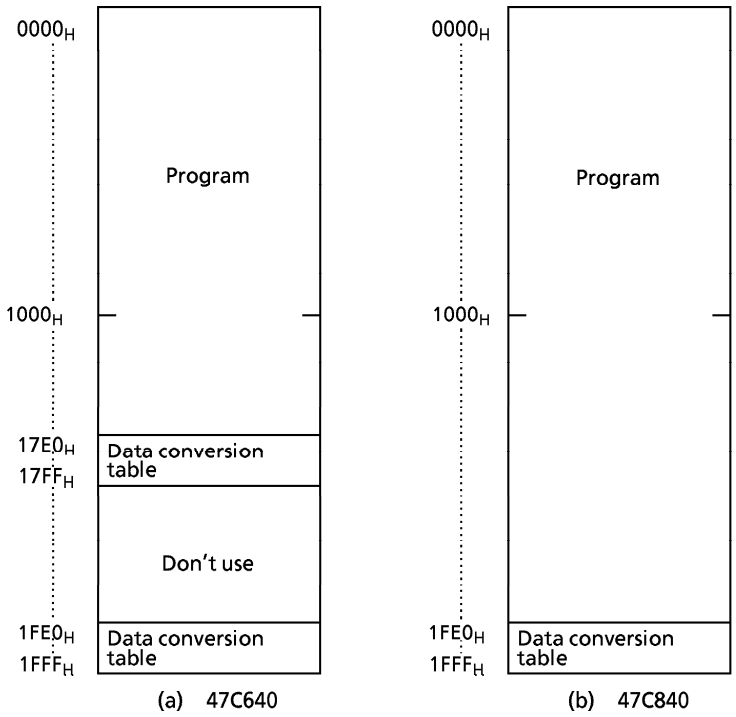


Figure 1-1. Program area

1.1.2 Data Memory

The 47P840V has 512 × 4-bit data memory bank (RAM).

When using the 47P840V as a 47C640 evaluator, do not write data to address 80_H and following, even though the bank 1 addresses are 00 to FF_H. There is no necessity to take into consideration a special common function area because one is built in bank 0.

1.1.3 Input/Output Circuitry

(1) Control pins
This is the same as for the 47C640/840 except that there is no built-in pull-down resistance for the TEST pin.

(2) I/O Ports
The input/output circuit of the 47P840V is the same as I/O code IA of the 47C640/840.
External resistance, for example, is required when using as evaluator of other I/O codes (IB, IC), (Refer to Figure 1.2)

(a) Equivalent to IO code IB (b) Equivalent to IO code IC

Figure 1-2. I/O code and external circuitry

1.2 PROM mode

The PROM mode is set by setting the $\overline{\text{RESET}}$ and $\overline{\text{HOLD}}$ pins to the "L" level. The PROM mode can be used as a general-purpose PROM writer for program writing and verification. (A high-speed program mode is used set the ROM type the same as for the TMM 2764AD.)

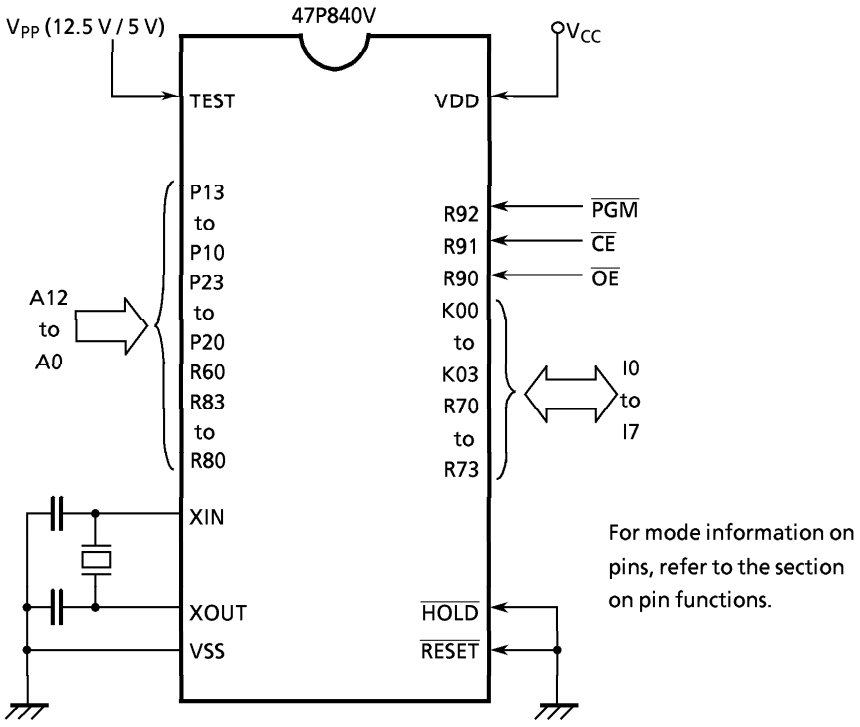


Figure 1-3. Setting for PROM mode

An adapter socket is available for connecting a PROM writer.

- BM1171 : TMP47P840VN
- BM1172 : TMP47P840VF

1.2.1 High Speed Programming Mode

The device is set up in the high speed programming mode when the programming voltage (12.5V) is applied to the Vpp terminal with Vcc = 6V and $\overline{PGM} = V_{IH4}$. The programming is achieved by applying a Single TTL low level 1 ms, pulse the $\overline{PGM}$ input after addresses and data are stable. Then the programmed data is verified by using program Verify Mode. If the programmed data is not correct, another program pulse of 1 ms is applied and then programmed data is verified. This should be repeated until the program operates correctly (max. 25 times). After correctly programming the selected address, one additional program pulse with pulse width 3 times that needed for programming is applied. When programming has been completed, the data in all addresses should be verified with Vcc = Vpp = 5 V.

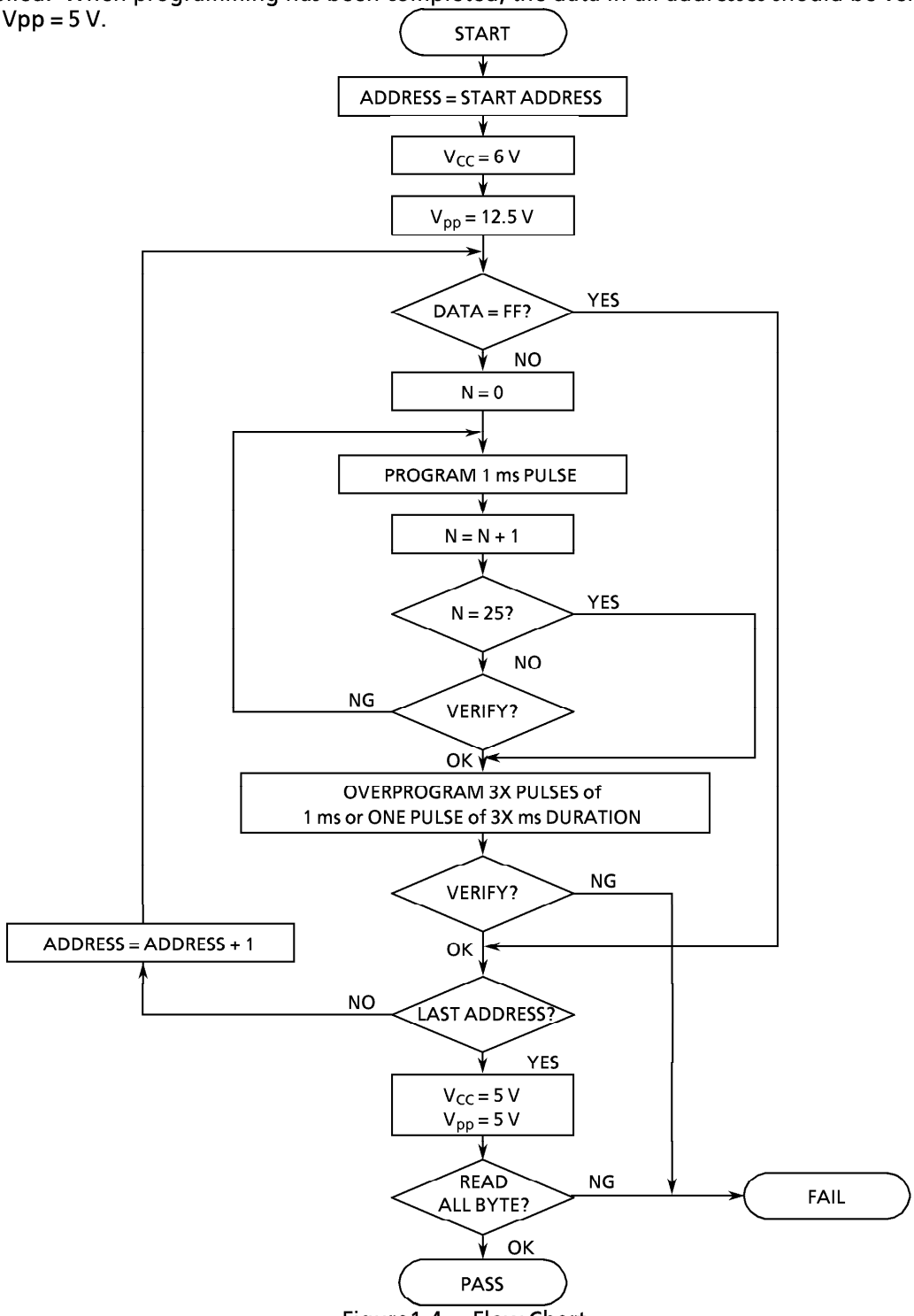


Figure1-4. Flow Chart

ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS (V_{SS} = 0V)

PARAMETER	SYMBOL	PINS	RATING	UNIT
Supply Voltage	V_{DD}		– 0.3 to 6.5	V
Program Voltage	V_{PP}	TEST / VPP pin	– 0.3 to 13.0	V
Input Voltage	V_{IN}		– 0.3 to V_{DD} + 0.3	V
Output Voltage	V_{OUT}		– 0.3 to V_{DD} + 0.3	V
Output Current (per 1 pin)	I_{OUT1}	Ports P1, P2	30	mA
	I_{OUT2}	Ports R4 to R9	3.2	
Output Currnent (Total)	ΣI_{OUT1}	Ports P1, P2	120	mA
Power Dissipation [T_{opr} = 70℃]	PD		600	mW
Soldering Temperature (time)	T_{sld}		260 (10 s)	°C
Storage Temperature	T_{stg}		– 55 to 125	°C
Operating Temperature	T_{opr}		– 40 to 70	°C

RECOMMENDED OPERATING CONDITIONS (V_{SS} = 0V, T_{opr} = – 40 to 70°C)

PARAMETER	SYMBOL	PINS	CONDITIONS	Min.	Max.	UNIT
Supply Voltage	V_{DD}		fc = 6 MHz	4.5	5.5	V
			fc = 4.2 MHz	2.7		
			In the SLOW mode	2.7		
			In the HOLD mode	2.0		
Input High Voltage	V_{IH1}	Except Hysteresis Input	$V_{DD} \geqq 4.5$ V	$V_{DD} \times 0.7$	V_{DD}	V
	V_{IH2}	Hysteresis Input		$V_{DD} \times 0.75$		
	V_{IH3}		$V_{DD} < 4.5$ V	$V_{DD} \times 0.9$		
Input Low Voltage	V_{IL1}	Except Hysteresis Input	$V_{DD} \geqq 4.5$ V	0	$V_{DD} \times 0.3$	V
	V_{IL2}	Hysteresis Input			$V_{DD} \times 0.25$	
	V_{IL3}		$V_{DD} < 4.5$ V		$V_{DD} \times 0.1$	
Clock Frequency	fc	XIN, XOUT		0.4	6.0	MHz
	fs	XTIN, XTOUT		30	34	kHz

Note. : Input voltage V_{IH3}, V_{IL3} : in the SLOW or HOLD mode

D.C. CHARACTERISTICS (V_{SS} = 0V, T_{opr} = – 40 to 70°C)

PARAMETER	SYMBOL	PINS	CONDITIONS	Min.	Typ.	Max.	UNIT
Hysteresis Voltage	V_{HS}	Hysteresis Input		–	0.7	–	V
Input Current	I_{IN1}	K0, TEST, $\overline{RESET}$, $\overline{HOLD}$	V_{DD} = 5.5V, V_{IN} = 5.5V / 0V	–	–	± 2	μA
	I_{IN2}	ports R (open drain)					
Input Resistance	R_{IN}	$\overline{RESET}$		100	220	450	kΩ
Output Leakage Current	I_{LO}	sink open drain	V_{DD} = 5.5V, V_{IN} = 5.5V	–	–	2	μA
Output Level Low Voltage	V_{OL}	Except Xout, ports P	V_{DD} = 4.5V, I_{OL} = 1.6mA	–	–	0.4	V
Output Level Low Voltage	I_{OL}	Ports P1, P2	V_{DD} = 4.5V, V_{OL} = 1.0V	–	20	–	mA
Supply Current (in the Normal mode)	I_{DD}		V_{DD} = 5.5V, fc = 4MHz	–	3	6	mA
Supply Current (in the SLOW mode)	I_{DDS}		V_{DD} = 3.0V, fs = 32.768kHz	–	30	60	μA
Supply Current (in the HOLD mode)	I_{DDH}		V_{DD} = 5.5V	–	0.5	10	μA

Note 1. Typ. values show those at T_{opr} = 25°C, V_{DD} = 5V.

Note 2. Input Current I_{IN1} ; The current through resistor is not included, when the input resistor (pull-up/pull-down) is contained.

Note 3. Supply Current I_{DD}, I_{DDH} ; V_{IN} = 5.3V/0.2V
The K0 port is open when the input resistor is contained. The voltage applied to the R port is within the valid range.
Supply Current I_{DDS} ; V_{IN} = 2.8V/0.2V
Low frequency clock is only osillated (connecting XTIN, XTOUT).

A / D CONVERSION CHARACTERISTICS (T_{opr} = – 40 to 70°C)

PARAMETER	SYMBOL	CONDITIONS	Min.	Typ.	Max.	UNIT
Analog Reference Voltage	V_{AREF}		V_{DD} – 1.5	–	V_{DD}	V
	V_{ASS}		V_{SS}	–	1.5	
Analog Reference Voltage Range	ΔV_{AREF}	$V_{AREF} - V_{ASS}$	2.5	–	–	V
Analog Input Voltage	V_{AIN}		V_{ASS}	–	V_{AREF}	V
Analog Supply Current	I_{REF}		–	0.5	1.0	mA
Nonlinearity Error		V_{DD} = 5.0V, V_{SS} = 0.0V V_{AREF} = V_{DD} ± 0.001V V_{ASS} = 0.000V	–	–	± 1	LSB
Zero Point Error			–	–	± 1	
Full Scale Error			–	–	± 1	
Total Error			–	–	± 2	

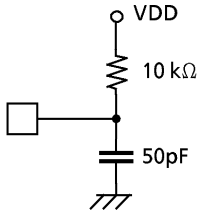
A.C. CHARACTERISTICS

(V_{SS} = 0V, V_{DD} = 4.5 to 6.0V, T_{opr} = – 40 to 70°C)

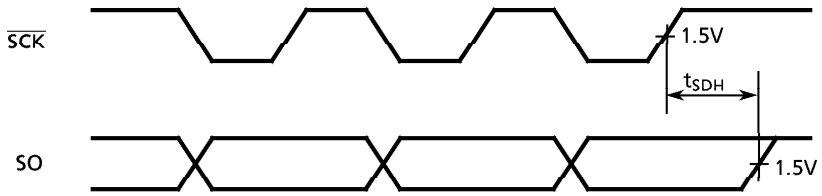
PARAMETER	SYMBOL	CONDITIONS	Min.	Typ.	Max.	UNIT
Instruction Cycle Time	t_{cy}	in the Normal mode	1.33	–	20	μs
		in the SLOW mode	235	–	267	
High Level Clock pulse Width	t_{WCH}	External clock mode	80	–	–	ns
Low Level Clock pulse Width	t_{WCL}					
A/D Sampling Time	t_{AIN}	fc = 4 MHz	–	4	–	μs
Shift Data Hold Time	t_{SDH}		$0.5t_{cy}$ – 300	–	–	ns

Note. Shift data Hold time :

External circuit for $\overline{SCK}$ pin and SO pin



Serial port (completion of transmission)



RECOMMENDED OSCILLATING CONDITIONS

(V_{SS} = 0V, V_{DD} = 4.5 to 6.0V, T_{opr} = – 40 to 70°C)

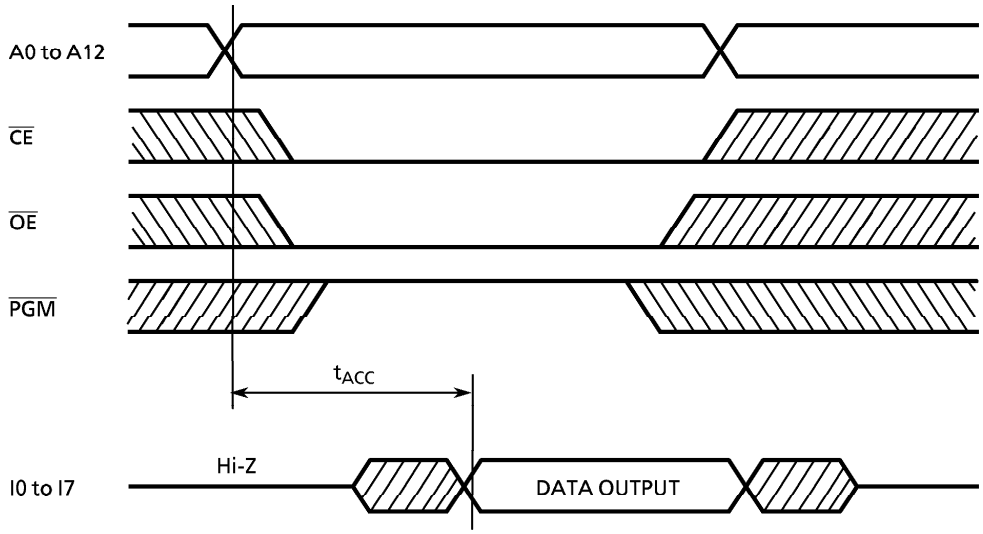
Recommended oscillating conditions of the 47P840V are equal to the 47C840's.

D.C./A.C. CHARACTERISTICS

(V_{SS} = 0V)

(1) Read Operation

PARAMETER	SYMBOL	CONDITION	Min.	Typ.	Max.	UNIT
Output Level High Voltage	V_{IH4}		$V_{CC} \times 0.7$	–	V_{CC}	V
Output Level Low Voltage	V_{IL4}		0	–	$V_{CC} \times 0.3$	V
Supply Voltage	V_{CC}		4.75	–	6.0	V
Programming Voltage	V_{PP}					
Address Access Time	t_{ACC}	V_{CC} = 5.0 ± 0.25V	0	–	350	ns



(2) High Speed Programming Operation

PARAMETER	SYMBOL	CONDITION	Min.	Typ.	Max.	UNIT
Input High Voltage	V_{IH4}		$V_{CC} \times 0.7$	–	V_{CC}	V
Input Low Voltage	V_{IL4}		0	–	$V_{CC} \times 0.3$	V
Supply Voltage	V_{CC}		4.75	–	6.0	V
V_{PP} Power Supply Voltage	V_{PP}		12.25	12.50	12.75	V
Programming Pulse Width	t_{PW}	V_{CC} = 6.0 ± 0.25V	0.95	1.0	1.05	ms