LSI/CSI
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LS7210

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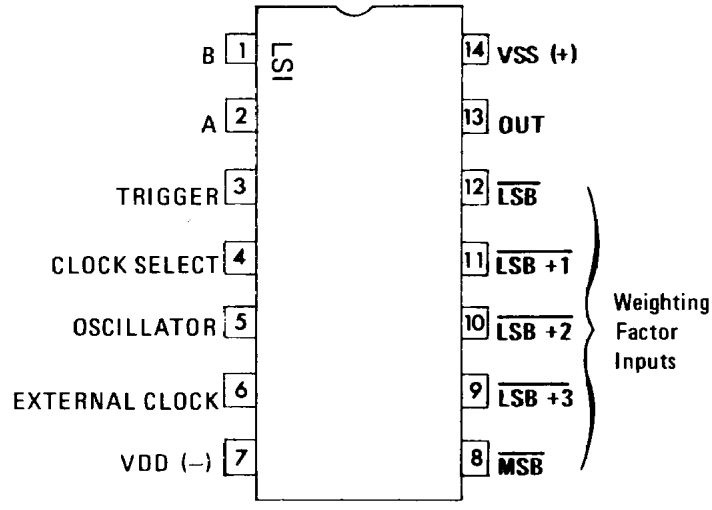
PROGRAMMABLE DIGITAL DELAY TIMER

FEATURES:

- Programmable Delay from Miliseconds to Hours
- Can be Cascaded for Sequential Events or Extended Delay
- Single Power Supply Operation +4.75V to +15V
- On Chip Oscillator
- Alternate Clock Input
- On Chip Power On Reset
- Internal Pull-ups on Inputs
- Frequency Range to 160 KHz
- CMOS Type Noise Immunity on All Inputs
- All Inputs are CMOS, PMOS & TTL Compatible

DESCRIPTION:

The LS7210 is a monolithic, ion implanted MOS programmable digital timer that can generate a delay in the range of 6ms to infinity. The delay is programmed by 5 binary weighted input bits in combination with the oscillator provided. The chip can be operated into 4 different modes: delayed operate, delayed release, dual delay and one-shot. These modes are selected by the control inputs A & B.



TOP VIEW
STANDARD 14 PIN DIP
Figure 1

INPUT/OUTPUT DESCRIPTION:

OSCILLATOR INPUT

The frequency of the internal oscillator is set by an RC network connected to the OSC input, as shown in Figure 2. The nominal oscillator frequency, f, at room temperature is given by $f \approx 1/RC$ where R values range from a minimum of 47KΩ to a maximum 3M Ω. (See Note 1)

EXTERNAL CLOCK INPUT

If the internal oscillator is not used, the chip can be driven by an external clock applied to this input.

CLOCK SELECT INPUT

The internal oscillator or the external clock is selected by the proper logical level applied to this input. A logic "1" selects the external clock and logic"0" selects the internal oscillator. The clock select input has an internal pull up resistor.

TRIGGER INPUT

A positive or a negative transition at the trigger input initiates a delay in turning on or off the output. A negative transition always turns on the output with or without delay depending on the selected mode. A positive transition at the trigger input always turns off the output (with the exception of one-shot mode) with or without delay depending on the the selected mode. The delay is a function of the oscillator frequency (or the external clock frequency) and the weighting factor programmed at the weighting factor inputs. The trigger input is clocked into the input latch with the negative edge of the external clock. All timings begin after the latch has been set up. The trigger input has an internal pull-up resistor.

NOTE 1: Oscillation accuracy from chip to chip for a fixed value of RC, is ± 10%. Parts can be supplied to tighter tolerances for small additional cost.

WEIGHTING FACTOR INPUT, LS8-MSB

A delay from the trigger input to the output is programmed by applying 1's complement binary weighted numbers at these 5 inputs. The exact equation for the delay is:

$$\text{Delay} = \frac{(1 + 1,023N)}{f}$$ See Fig. 5 Note 3

Where f = The oscillator frequency and N = Weighting factor. All the weighting factor inputs have internal pull-up resistors.

TABLE 1
WEIGHTING BITS ASSIGNMENT

INPUTS	VALUE
$\overline{\text{LSB}}$	1
$\overline{\text{LSB}+1}$	2
$\overline{\text{LSB}+2}$	4
$\overline{\text{LSB}+3}$	8
$\overline{\text{MSB}}$	16

Example: For a weighting factor of 25, inputs $\overline{\text{MSB}}$, $\overline{\text{LSB}+3}$, and $\overline{\text{LSB}}$ should be programmed to logic "0".

MODE SELECT INPUTS A & B

The chip can be programmed to operate in 4 different modes by applying the logic levels to inputs A & B as indicated in Table 2. The mode select inputs are clocked into the input latches with the negative edge of the external clock. These inputs should not be changed while a delay timing is in progress. The mode select inputs have internal pull-ups.

MODE DEFINITION: (See Figure 3)

DUAL DELAY MODE

This is the Default Mode when the inputs A & B are left unprogrammed. The function of the Dual Delay mode is to provide a time delay on both the turn-on and turn-off of the output. Once turned on, the output will remain on as long as the trigger input is logic "0". Once turned off, the output will remain off as long as the trigger input is a logic "1".

DELAYED OPERATE MODE

This mode causes a retriggerable delay in turning the output on in response to a negative edge at the trigger input. The output is turned off without delay in response to a positive transition at the trigger input.

DELAYED RELEASE MODE

This mode causes a retriggerable delay in turning off the output whenever there is a positive transition at the trigger input. The output is turned on without delay in response to a negative transition at the trigger input.

ONE-SHOT MODE

In this mode, the chip functions like a retriggerable monostable multi-vibrator. The output is turned on whenever there is a negative transition at the trigger input. At the end of the programmed delay, the output is turned off automatically. If there is a negative transition at the trigger input before the delay is over, the delay is restarted. A positive transition at the trigger input has no effect on the output in this mode.

NOTE: In one-shot mode, the TRIGGER input must be held at logic "1" during a power-up.

OUTPUT

The output is an open drain FET. To obtain proper switching of the output between logic "0" and "1" levels, an external pull down resistor to V_{DD} must be used. If the output is used only as a current source, no such pull down is needed. The output is logically inverted with respect to the trigger input.

TABLE 2
MODE SELECTION

CONTROL		MODE
A	B	
1	1	Dual Delay
1	0	Delayed Release
0	1	Delayed Operate
0	0	One Shot

ABSOLUTE MAXIMUM RATINGS: (All voltages referenced to V_{DD})

	SYMBOL	VALUE	UNITS
DC Supply Voltage	V_{SS}	+18	V
Voltage (Any Pin)	V_{IN}	0 to V_{SS} +.3	V
Operating Temperature	T_A	−25 to +70	°C
Storage Temperature	T_{stg}	−65 to +150	°C

DC ELECTRICAL CHARACTERISTICS:

(-25°C T_A +70°C unless otherwise specified.
All voltages referenced to V_{DD})

PARAMETER	SYMBOL	MIN	MAX	UNITS	CONDITIONS
Supply Voltage	V_{SS}	+4.75	+15.0	V	
Supply Current	I_{SS}	—	3.0	mA	V_{SS} = +15V, output off
Trigger Input					
Logical "1"	V_{TH}	+4	+ 5	V	@V_{SS} = + 5V
		+9	+10	V	@V_{SS} = +10V
		+14	+15	V	@V_{SS} = +15 V
Logical "0"	V_{TL}	0	+ 1	V	@V_{SS} = + 5V
		0	+ 2	V	@V_{SS} = +10V
		0	+ 3	V	@V_{SS} = +15V
All Other Inputs					
Logical "1"	V_{IH}	+4	+ 5	V	@V_{SS} = + 5V
		+8	+10	V	@V_{SS} = +10V
		+12	+15	V	@V_{SS} = +15V
Logical "0"	V_{IL}	0	+1.0	V	@V_{SS} = + 5V
		0	+2.0	V	@V_{SS} = +10V
		0	+3.0	V	@V_{SS} = +15V
Output					
Source Current	I_o	+550	—	μA	@V_0 = + 4.5V, V_{SS} = + 5V
		+1.0	—	mA	@V_0 = + 4.0V, V_{SS} = + 5V
		+2.8	—	mA	@V_0 = + 9.0V, V_{SS} = +10V
		+4.9	—	mA	@V_0 = + 8.0V, V_{SS} = +10V
		+4.2	—	mA	@V_0 = +14.0V, V_{SS} = +15V
		+8.1	—	mA	@V_0 = +13.0V, V_{SS} = +15V

SWITCHING CHARACTERISTICS:

(See Figure 4)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Oscillator Frequency	f_{osc}	—	—	100	KHz
External Clock Frequency	f_{ext}	DC	—	160	KHz
External Clock Positive Pulse Width	t_H	3	—	—	μs
External Clock Negative Pulse Width	t_L	3	—	—	μs
A, B and Trigger Input Set-Up Time	t_S	—	200	300	ns
EXT Clock to Output Delay (turn-on delay in delayed release mode and turn-off delay in delayed operate mode)	t_{nd}	—	700	1000	ns
EXT Clock to Output Delay at the End of Time Out	t_{od}	—	1	1.6	μs
EXT Clock to Output Delay (turn-on Delay in One Shot Mode)	t_{sd}	—	400	600	ns

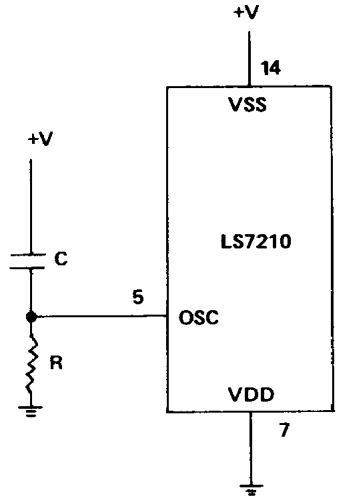


FIGURE 2 — LS7210 OSCILLATOR CONNECTION

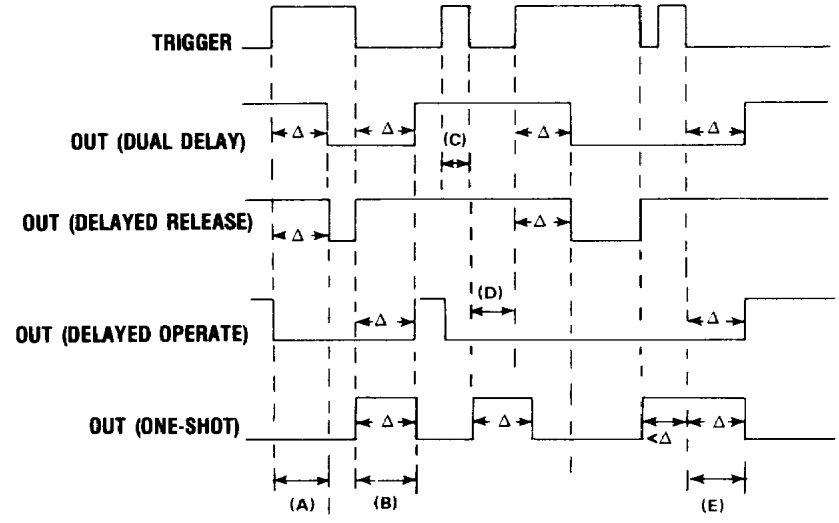


FIGURE 3 — MODE DEFINITION TIMING DIAGRAM

A — Turn-off delay in "Dual Delay" and "Delayed Release" mode.
B — Turn-on delay in "Dual Delay" and "Delayed Operate" mode; one-shot period in "one-shot" mode.
C — Output remains on in "Delayed Release" and "Dual Delay" modes due to negative "trigger" transition before the turn-off delay is over.
D — Output remains off in "Delayed Operate" mode due to positive trigger transition before the turn-on delay is over.
E — One-Shot period extended by re-triggering.
NOTE: Δ is the programmed delay.

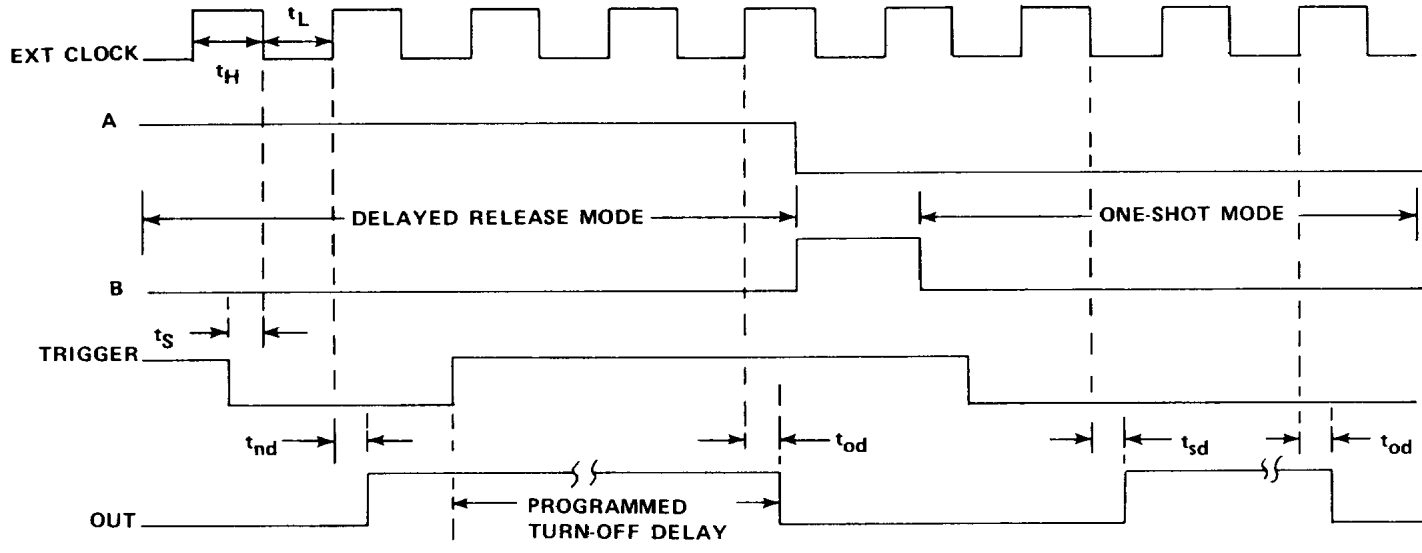


FIGURE 4 — LS7210 TIMING DIAGRAM

Note 1. — A,B and trigger inputs are clocked into the input latches with the negative edge of the ext. clock.

Note 2. — In all modes except One-Shot, the output changes with the positive transition of the ext. clock. In One-Shot mode the output is turned on with the negative transition and turned off with the positive transition of the ext. clock.

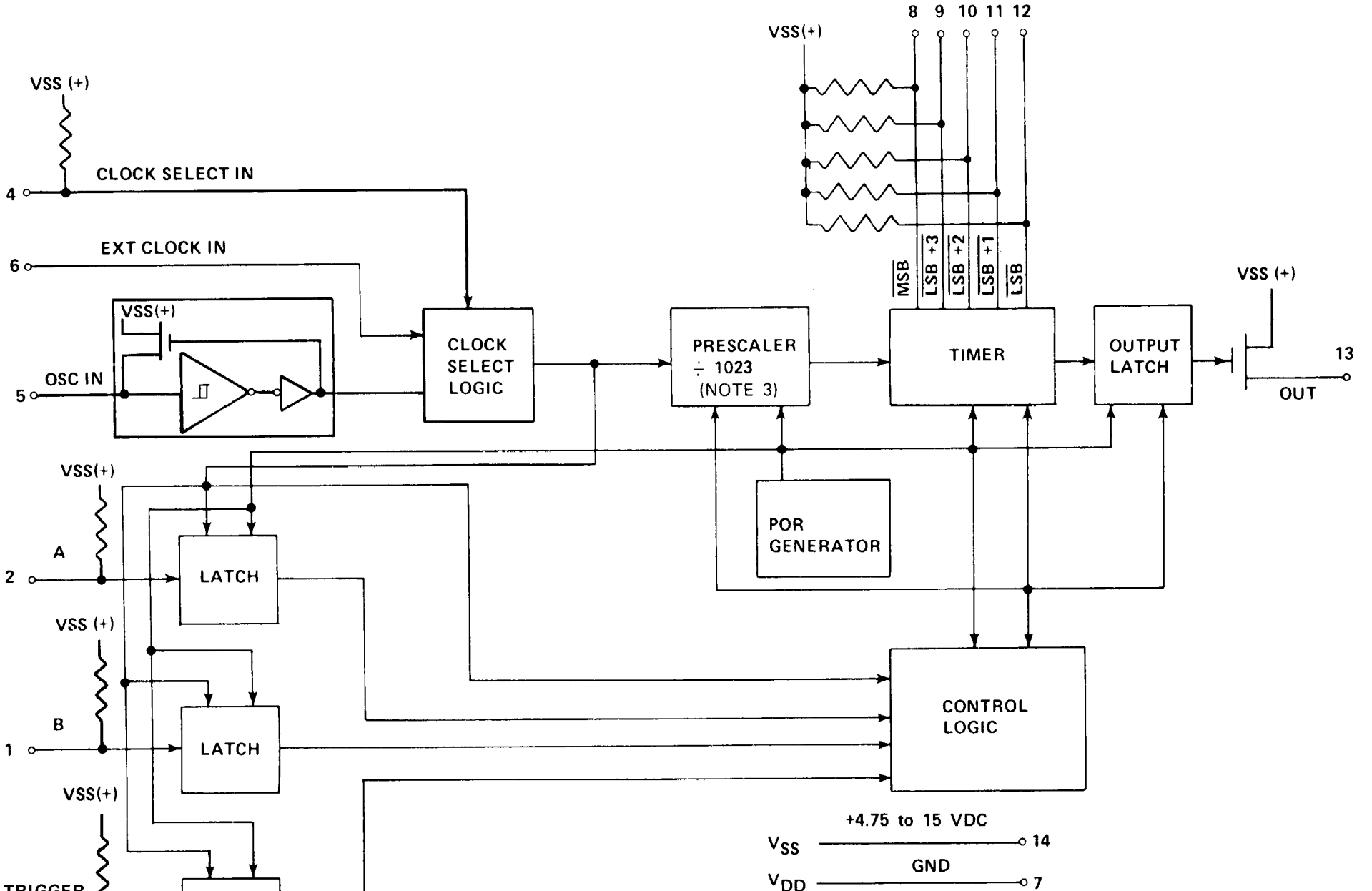


FIGURE 5
LS7210 BLOCK DIAGRAM

NOTES:

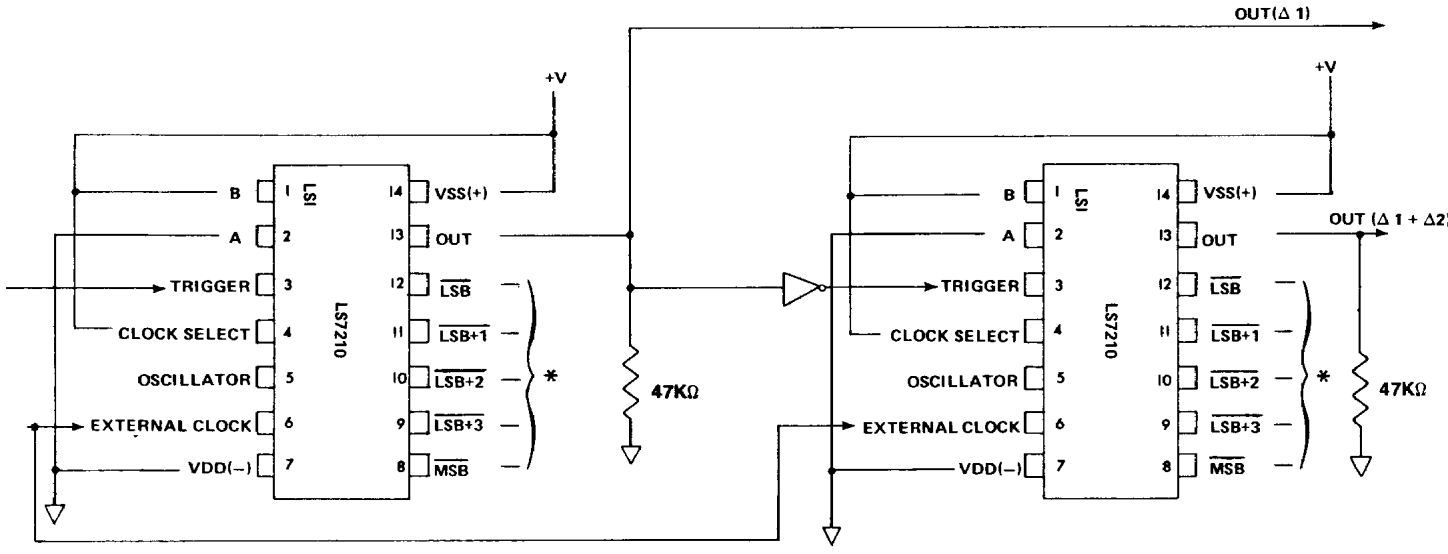
(1) Oscillator FET device can source: 0.6mA @ VSS = +5V
1.6mA @ VSS = +10V
2.7mA @ VSS = +15V

(2) All resistors shown represent a nominal 3 μa constant current source.

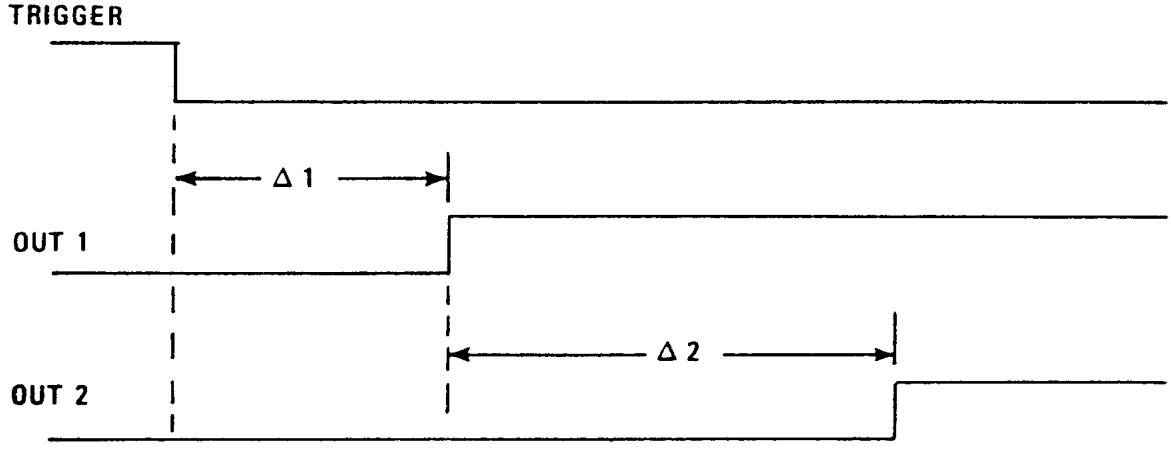
(3) ÷1023 is standard. Any number from 1 to 1022 can be mask programmed.

APPLICATION EXAMPLES

SEQUENTIAL TURN ON



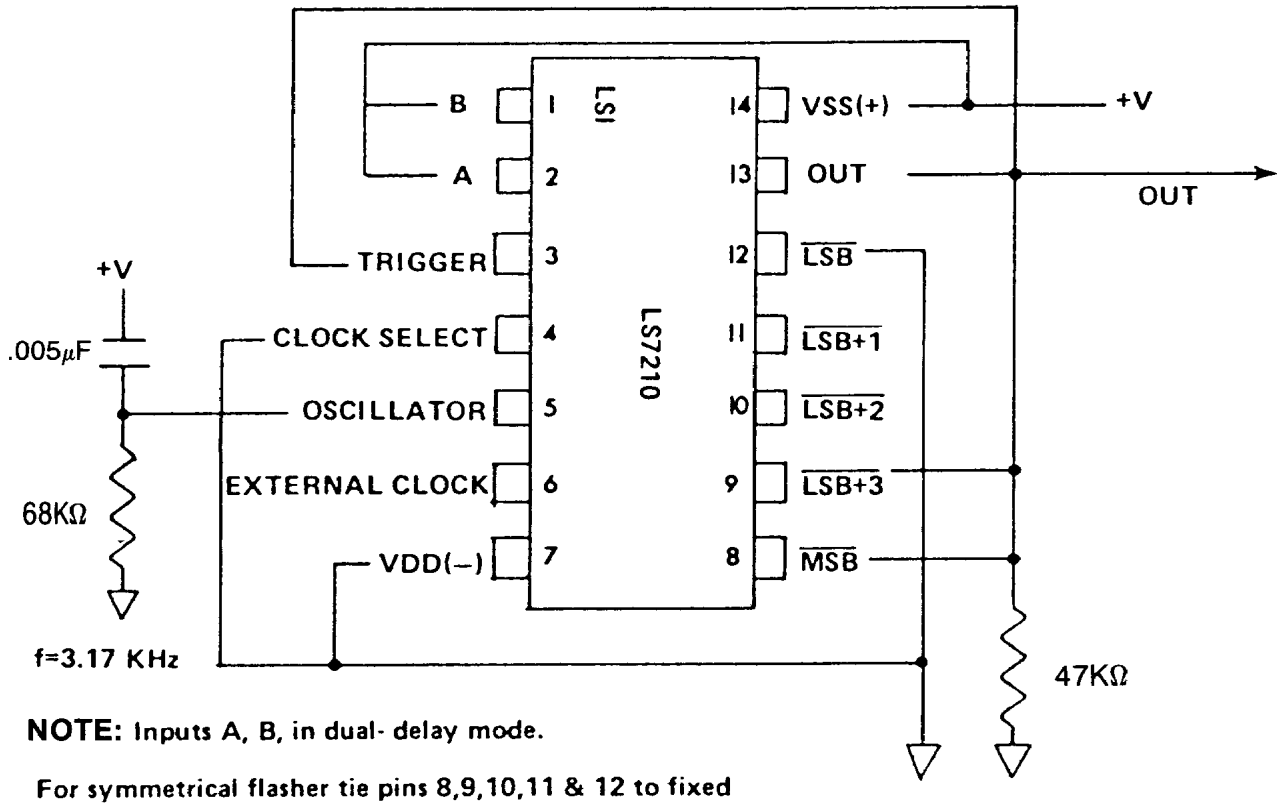
*Connect for desired weighting factor.



NOTE: Output of LS7210 is open drain FET. A Resistor to ground is required to cause output to go negative.

FIGURE 6

UNSYMMETRICAL FLASHER



NOTE: Inputs A, B, in dual- delay mode.

For symmetrical flasher tie pins 8,9,10,11 & 12 to fixed weighting factor.

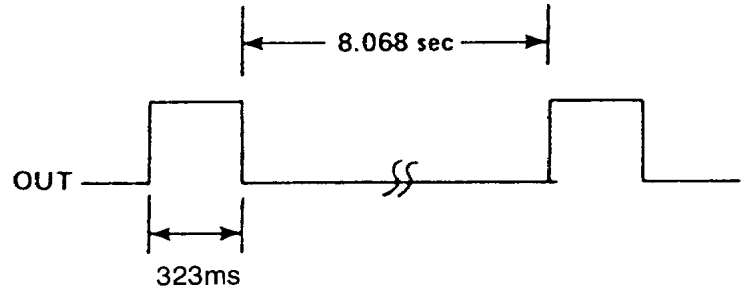


FIGURE 7

LS7210 IN DELAYED OPERATE MODE TO ACHIEVE ONE TO 31 MINUTE DELAY

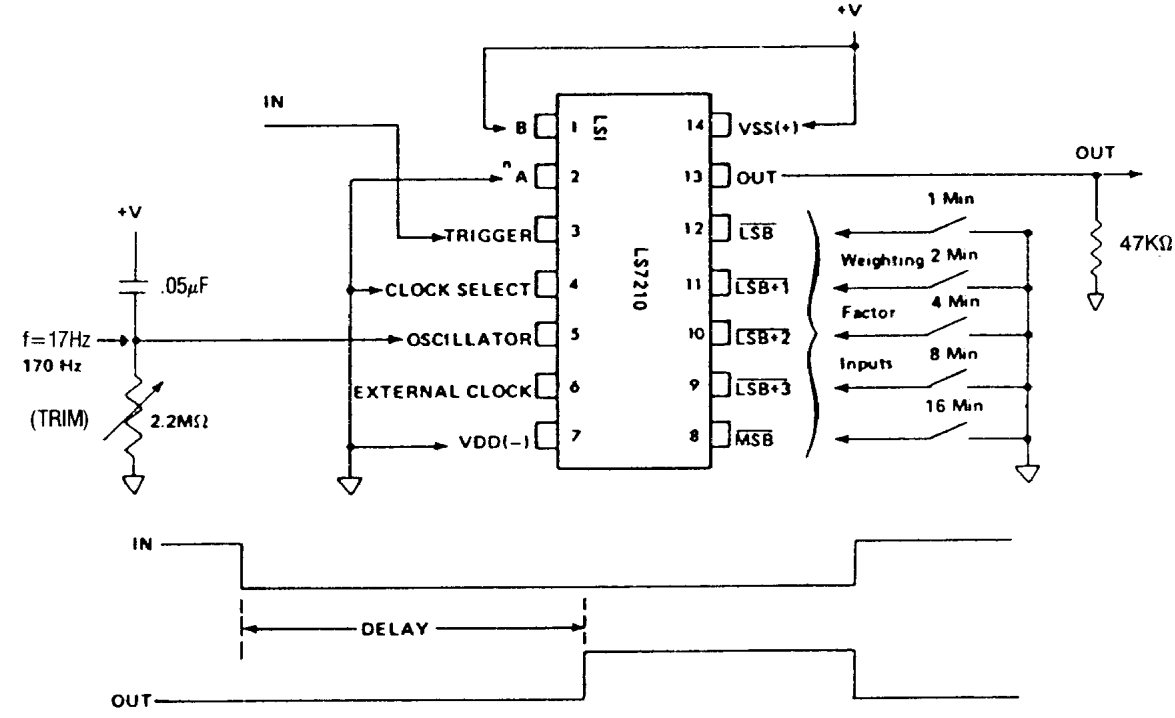
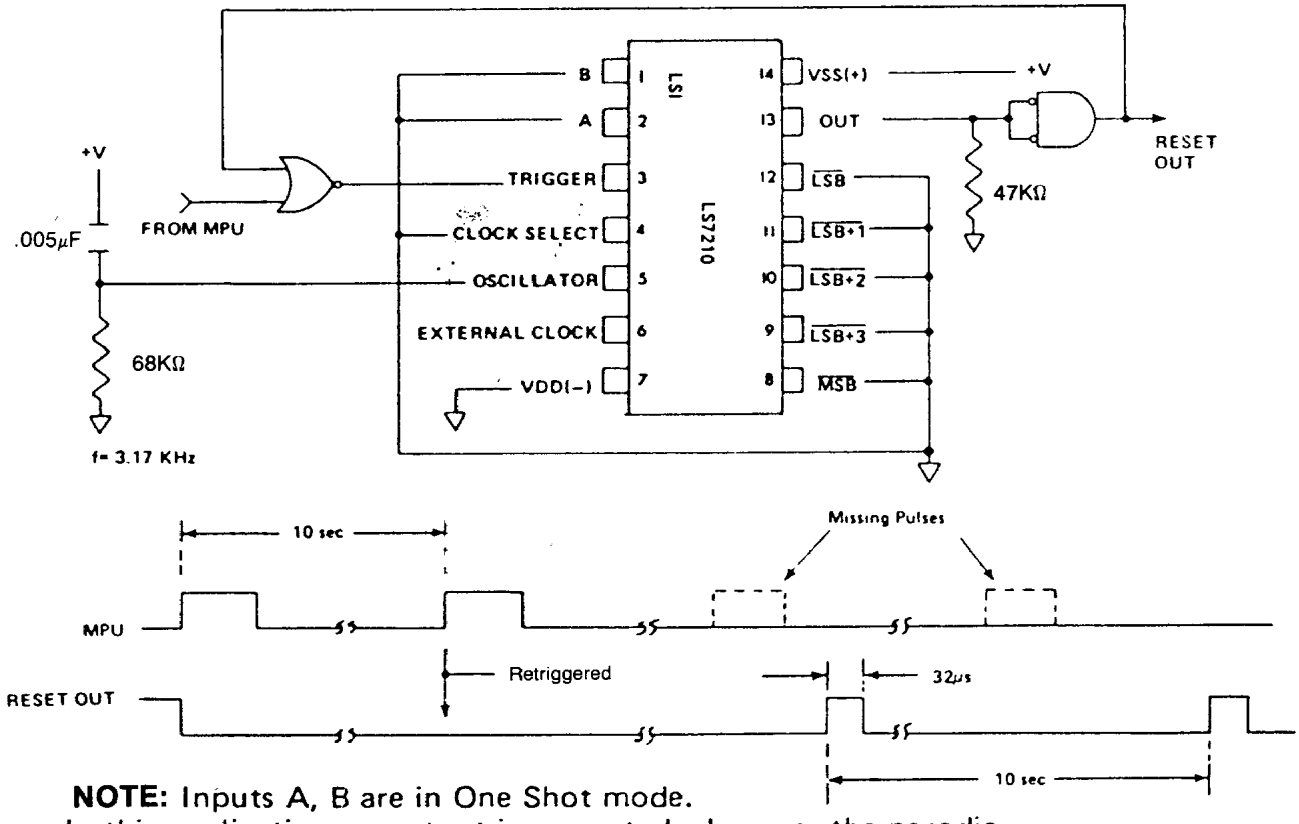


FIGURE 8

AUTO RESET WATCHDOG CIRCUIT



NOTE: Inputs A, B are in One Shot mode.
In this application an output is generated whenever the perodic sampling signal from the MPU is interrupted.

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FIGURE 9