Document Title

32Kx32-Bit Synchronous Pipelined Burst SRAM, 3.3V Power Datasheets for 100 QFP/TQFP

Revision History

Rev. No.	History	Draft Data	Remark
Rev.0.0	Initial draft	Oct. 28.1996	Preliminary
Rev.1.0	Final spec release	May.13. 1997	Final

32Kx32-Bit Synchronous Pipelined Burst SRAM

FEATURES

- Synchronous Operation.
- 2 Stage Pipelined operation with 4 Burst.
- On-Chip Address Counter.
- Self-Timed Write Cycle.
- On-Chip Address and Control Registers.
- V_{DD} = 3.3V-5%/+10% Power Supply
- 5V Tolerant Inputs except I/O Pins
- Byte Writable Function.
- Global Write Enable Controls a full bus-width write.
- Power Down State via ZZ Signal.
- LBO Pin allows a choice of either a interleaved burst or a linear burst.
- Three Chip Enables for simple depth expansion with No Data Contention ; 2cycle Enable, 1cycle Disable.
- Asynchronous Output Enable Control.
- ADSP, ADSC, ADV Burst Control Pins.
- TTL-Level Three-State Output.
- 100-QFP-1420C
- 100-TQFP-1420A

FAST ACCESS TIMES

Parameter	Symbol	-13	-15	Unit
Cycle Time	t_{CYC}	13	15	ns
Clock Access Time	t_{CD}	7.0	8.0	ns
Output Enable Access Time	t_{OE}	6.0	7.0	ns

GENERAL DESCRIPTION

The KM732V589A/L is a 1,048,576-bit Synchronous Static Random Access Memory designed for high performance second level cache of Pentium and Power PC based System.

It is organized as 32K words of 32bits and integrates address and control registers, a 2-bit burst address counter and added some new functions for high performance cache RAM applications; GW, BW, LBO, ZZ.

Write cycles are internally self-timed and synchronous.

Full bus-width write is done by GW, and each byte write is performed by the combination of WEx and BW when GW is high. And with CS_1 high, ADSP disable to support address pipelining.

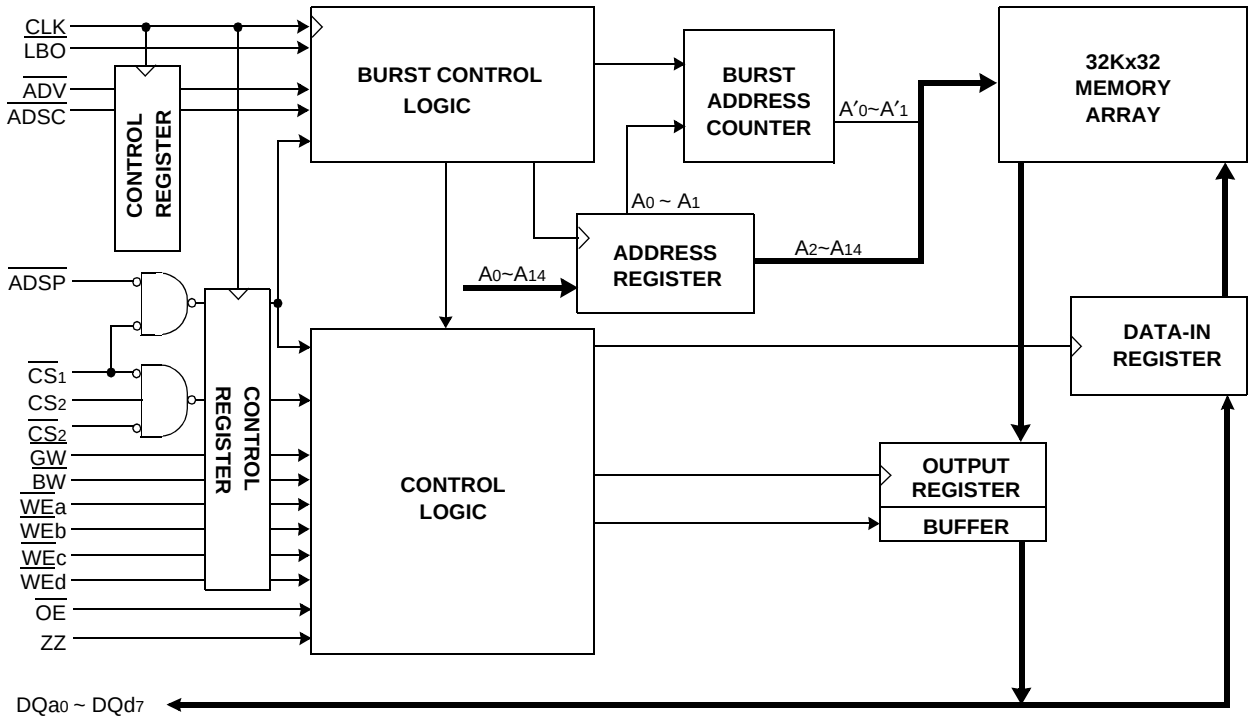
Burst cycle can be initiated with either the address status processor(ADSP) or address status cache controller(ADSC) inputs. Subsequent burst addresses are generated internally in the system's burst sequence and are controlled by the burst address advance(ADV) input.

LBO pin is DC operated and determines burst sequence(linear or interleaved).

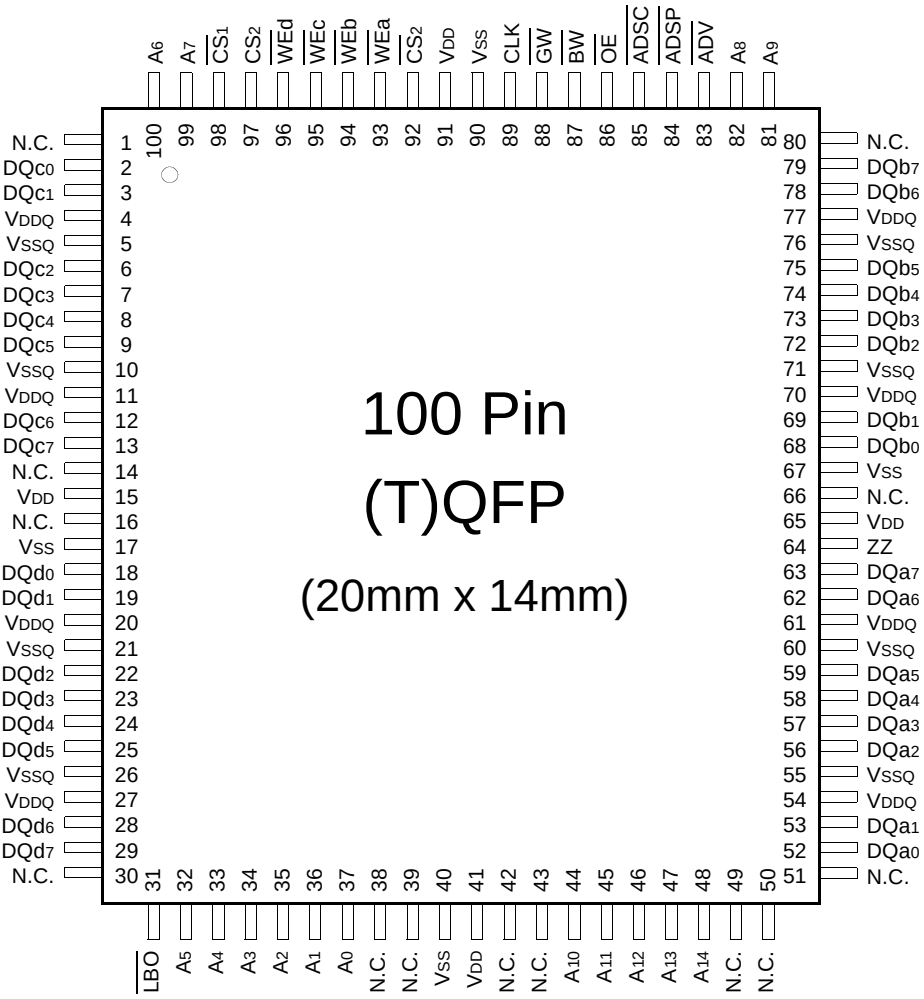
ZZ pin controls Power Down State and reduces Stand-by current regardless of CLK.

The KM732V589A/L is fabricated using SAMSUNG's high performance CMOS technology and is available in a 100pin QFP/TQFP package. Multiple power and ground pins are utilized to minimize ground bounce.

LOGIC BLOCK DIAGRAM



PIN CONFIGURATION(TOP VIEW)



PIN NAME

SYMBOL	PIN NAME	TQFP PIN NO.	SYMBOL	PIN NAME	TQFP PIN NO.
A0 - A14	Address Inputs	32,33,34,35,36,37, 44,45,46,47,48,81, 82,99,100	VDD	Power Supply(+3.3V)	15,41,65,91
			VSS	Ground	17,40,67,90
			N.C.	No Connect	1,14,16,30,38,39,42,43, 49,50,51,66,80
$\overline{ADV}$	Burst Address Advance	83			
$\overline{ADSP}$	Address Status Processor	84	DQa0~a7	Data Inputs/Outputs	52,53,56,57,58,59,62,63
ADSC	Address Status Controller	85	DQb0~b7		68,69,72,73,74,75,78,79
$\overline{CLK}$	Clock	89	DQc0~c7		2,3,6,7,8,9,12,13
CS1	Chip Select	98	DQd0~d7		18,19,22,23,24,25,28,29
$\overline{CS2}$	Chip Select	97			
CS2	Chip Select	92	VDDQ	Output Power Supply	4,11,20,27,54,61,70,77
$\overline{WEx}$	Byte Write Inputs	93,94,95,96			
$\overline{OE}$	Output Enable	86	VSSQ	Output Ground	5,10,21,26,55,60,71,76
$\overline{GW}$	Global Write Enable	88			
$\overline{BW}$	Byte Write Enable	87			
$\overline{ZZ}$	Power Down Input	64			
LBO	Burst Mode Control	31			

FUNCTION DESCRIPTION

The KM732V589A/L is a synchronous SRAM designed to support the burst address accessing sequence of the P6 and Power PC based microprocessor. All inputs (with the exception of $\overline{OE}$ and ZZ) are sampled on rising clock edges. The start and duration of the burst access is controlled by CS_1, $\overline{ADSC}$, $\overline{ADSP}$ and $\overline{ADV}$. The accesses are enabled with the chip select signals and output enabled signals. Wait states are inserted into the access with $\overline{ADV}$.

When ZZ is pulled high, the SRAM will enter a Power Down State. At this time, internal state of the SRAM is preserved. When ZZ returns to low, the SRAM normally operates after 2cycles of wake up time.

Read cycles are initiated with $\overline{ADSP}$(regardless of $\overline{WE}$x and $\overline{ADSC}$) using the new external address clocked into the on-chip address register whenever $\overline{ADSP}$ is sampled low, the chip selects are sampled active, and the output buffer is enabled with $\overline{OE}$. In read operation the data of cell array accessed by the current address, registered in the Data-out registers by the positive edge of CLK, are carried to the Data-out buffer by the next positive edge of CLK. The data, registered in the Data-out buffer, are projected to the output pins. $\overline{ADV}$ is ignored on the clock edge that samples $\overline{ADSP}$ asserted, but is sampled on the subsequent clock edges. The address increases internally for the next access of the burst when $\overline{WE}$x are sampled High and $\overline{ADV}$ is sampled low. And $\overline{ADSP}$ is blocked to control signals by disabling CS_1.

All byte write is done by $\overline{GW}$(regardless of $\overline{BW}$ and $\overline{WE}$x.), and each byte write is performed by the combination of $\overline{BW}$ and $\overline{WE}$x when $\overline{GW}$ is high.
Write cycles are performed by disabling the output buffers with $\overline{OE}$ and asserting $\overline{WE}$x. $\overline{WE}$x are ignored on the clock edge that samples $\overline{ADSP}$ low, but are sampled on the subsequent clock edges. The output buffers are disabled when $\overline{WE}$x are sampled Low(regardless of $\overline{OE}$). Data is clocked into the data input register when $\overline{WE}$x sampled Low. The address increases internally to the next address of burst, if both $\overline{WE}$x and $\overline{ADV}$ are sampled Low. Individual byte write cycles are performed by any one or more byte write enable signals($\overline{WE}$a, $\overline{WE}$b, $\overline{WE}$c or $\overline{WE}$d) sampled low. The $\overline{WE}$a controls DQa_0 ~ DQa_7, $\overline{WE}$b controls DQb_0 ~ DQb_7, $\overline{WE}$c controls DQc_0 ~ DQc_7, and $\overline{WE}$d controls DQd_0 ~ DQd_7. Read or write cycle may also be initiated with $\overline{ADSC}$, instead of $\overline{ADSP}$. The differences between cycles initiated with $\overline{ADSC}$ and $\overline{ADSP}$ as are follows;

- $\overline{ADSP}$ must be sampled high when $\overline{ADSC}$ is sampled low to initiate a cycle with $\overline{ADSC}$.
- $\overline{WE}$x are sampled on the same clock edge that sampled $\overline{ADSC}$ low(and $\overline{ADSP}$ high).

Addresses are generated for the burst access as shown below, The starting point of the burst sequence is provided by the external address. The burst address counter wraps around to its initial state upon completion. The burst sequence is determined by the state of the $\overline{LBO}$ pin. When this pin is Low, linear burst sequence is selected. When this pin is High, Interleaved burst sequence is selected.

BURST SEQUENCE TABLE

(Interleaved Burst)

$\overline{LBO}$ PIN	HIGH	Case 1		Case 2		Case 3		Case 4	
		A_1	A_0	A_1	A_0	A_1	A_0	A_1	A_0
First Address		0	0	0	1	1	0	1	1
↓		0	1	0	0	1	1	1	0
		1	0	1	1	0	0	0	1
Fourth Address		1	1	1	0	0	1	0	0

(Linear Burst)

$\overline{LBO}$ PIN	LOW	Case 1		Case 2		Case 3		Case 4	
		A_1	A_0	A_1	A_0	A_1	A_0	A_1	A_0
First Address		0	0	0	1	1	0	1	1
↓		0	1	1	0	1	1	0	0
		1	0	1	1	0	0	0	1
Fourth Address		1	1	0	0	0	1	1	0

NOTE : 1. $\overline{LBO}$ pin must be tied to High or Low, and Floating State must not be allowed.

TRUTH TABLES

SYNCHRONOUS TRUTH TABLE

$\overline{CS_1}$	CS_2	$\overline{CS_2}$	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	$\overline{WRITE}$	CLK	Address Accessed	Operation
H	X	X	X	L	X	X	↑	N/A	Not Selected
L	L	X	L	X	X	X	↑	N/A	Not Selected
L	X	H	L	X	X	X	↑	N/A	Not Selected
L	L	X	X	L	X	X	↑	N/A	Not Selected
L	X	H	X	L	X	X	↑	N/A	Not Selected
L	H	L	L	X	X	X	↑	External Address	Begin Burst Read Cycle
L	H	L	H	L	X	L	↑	External Address	Begin Burst Write Cycle
L	H	L	H	L	X	H	↑	External Address	Begin Burst Read Cycle
X	X	X	H	H	L	H	↑	Next Address	Continue Burst Read Cycle
H	X	X	X	H	L	H	↑	Next Address	Continue Burst Read Cycle
X	X	X	H	H	L	L	↑	Next Address	Continue Burst Write Cycle
H	X	X	X	H	L	L	↑	Next Address	Continue Burst Write Cycle
X	X	X	H	H	H	H	↑	Current Address	Suspend Burst Read Cycle
H	X	X	X	H	H	H	↑	Current Address	Suspend Burst Read Cycle
X	X	X	H	H	H	L	↑	Current Address	Suspend Burst Write Cycle
H	X	X	X	H	H	L	↑	Current Address	Suspend Burst Write Cycle

NOTE : 1. X means "Don't Care".

2. The rising edge of clock is symbolized by ↑.
3. $\overline{WRITE}$ = L means Write operation in WRITE TRUTH TABLE.
   $\overline{WRITE}$ = H means Read operation in WRITE TRUTH TABLE.
4. Operation finally depends on status of asynchronous input pins(ZZ and $\overline{OE}$).

WRITE TRUTH TABLE

$\overline{GW}$	$\overline{BW}$	$\overline{WEa}$	$\overline{WEb}$	$\overline{WEc}$	$\overline{WEd}$	Operation
H	H	X	X	X	X	READ
H	L	H	H	H	H	READ
H	L	L	H	H	H	WRITE BYTE a
H	L	H	L	H	H	WRITE BYTE b
H	L	H	H	L	L	WRITE BYTE c and d
H	L	L	L	L	L	WRITE ALL BYTEs
L	X	X	X	X	X	WRITE ALL BYTEs

NOTE : 1. X means "Don't Care".

2. All inputs in this table must meet setup and hold time around the rising edge of CLK(↑).

ASYNCHRONOUS TRUTH TABLE

(See Notes 1 and 2):

Operation	ZZ	$\overline{OE}$	I/O Status
Sleep Mode	H	X	High-Z
Read	L	L	DQ
	L	H	High-Z
Write	L	X	Din, High-Z
Deselected	L	X	High-Z

NOTE

1. X means "Don't Care".
2. ZZ pin is pulled down internally
3. For write cycles that following read cycles, the output buffers must be disabled with $\overline{OE}$, otherwise data bus contention will occur.
4. Sleep Mode means power down state of which stand-by current does not depend on cycle time.
5. Deselected means power down state of which stand-by current depends on cycle time.

PASS-THROUGH TRUTH TABLE

Previous Cycle		Present Cycle				Next Cycle
Operation	$\overline{WRITE}$	Operation	$\overline{CS_1}$	$\overline{WRITE}$	$\overline{OE}$	
Write Cycle, All bytes Address=An-1, Data=Dn-1	All L	Initiate Read Cycle Address=An Data=Qn-1 for all bytes	L	H	L	Read Cycle Data=Qn
Write Cycle, All bytes Address=An-1, Data=Dn-1	All L	No new cycle Data=Qn-1 for all bytes	H	H	L	No carryover from previous cycle
Write Cycle, All bytes Address=An-1, Data=Dn-1	All L	No new cycle Data=High-Z	H	H	H	No carryover from previous cycle
Write Cycle, One byte Address=An-1, Data=Dn-1	One L	Initiate Read Cycle Address=An Data=Qn-1 for one byte	L	H	L	Read Cycle Data=Qn
Write Cycle, One byte Address=An-1, Data=Dn-1	One L	No new cycle Data=Qn-1 for one byte	H	H	L	No carryover from previous cycle

NOTE : 1. This operation makes written data immediately available at output during a read cycle preceded by a write cycle.

ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Rating	Unit
Voltage on V_{DD} Supply Relative to V_{SS}	V_{DD}	-0.3 to 4.6	V
Voltage on V_{DDQ} Supply Relative to V_{SS}	V_{DDQ}	V_{DD}	V
Voltage on Input Pin Relative to V_{SS}	V_{IN}	-0.3 to 6.0	V
Voltage on I/O Pin Relative to V_{SS}	V_{IO}	-0.3 to V_{DDQ} + 0.5	V
Power Dissipation	P_D	1.2	W
Storage Temperature	T_{STG}	-65 to 150	°C
Operating Temperature	T_{OPR}	0 to 70	°C
Storage Temperature Range Under Bias	T_{BIAS}	-10 to 85	°C

***NOTE** : Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

OPERATING CONDITIONS ($0°C \leq T_A \leq 70°C$)

Parameter	Symbol	Min	Typ.	Max	Unit
Supply Voltage	V_{DD}	3.13	3.3	3.6	V
	V_{DDQ}	3.13	3.3	3.6	V
Ground	V_{SS}	0	0	0	V

CAPACITANCE*(T_A=25°C, f=1MHz)

Parameter	Symbol	Test Condition	Min	Max	Unit
Input Capacitance	C_{IN}	V_{IN}=0V	-	5	pF
Output Capacitance	C_{OUT}	V_{OUT}=0V	-	7	pF

***NOTE** : Sampled not 100% tested.

DC ELECTRICAL CHARACTERISTICS

(V_{DD}=3.3V-5%+10%, T_A=0 to 70°C)

Parameter	Symbol	Test Conditions		Min	Max	Unit
Input Leakage Current(except ZZ)	I_{IL}	V_{DD}= Max, V_{IN}=V_{SS} to V_{DD}		-2	+2	µA
Output Leakage Current	I_{OL}	Output Disabled, V_{OUT}=V_{SSQ} to V_{DDQ}		-2	+2	µA
Operating Current	I_{CC}	Device Selected, I_{OUT}=0mA, ZZ≤V_{IL}, All Inputs=V_{IL} or V_{IH} Cycle Time ≥ t_{CYC} min	-13	-	200	mA
			-15	-	180	
Standby Current	I_{SB}	Device deselected, I_{OUT}=0mA, ZZ≤V_{IL}, f=Max, All Inputs≤0.2V or≥V_{DD}-0.2V		-	40	mA
	I_{SB1}	Device deselected, I_{OUT}=0mA, ZZ≤0.2V, f = 0, All Inputs=fixed (V_{DD}-0.2V or 0.2V)		-	5	mA
			L-Ver.	-	1	mA
	I_{SB2}	Device deselected, I_{OUT}=0mA, ZZ≥V_{DD}-0.2V, f = Max, All Inputs≤V_{IL} or≥V_{IH}		-	5	mA
			L-Ver.	-	500	µA
Output Low Voltage	V_{OL}	I_{OL}=8.0mA		-	0.4	V
Output High Voltage	V_{OH}	I_{OH}=-4.0mA		2.4	-	V
Input Low Voltage	V_{IL}			-0.5*	0.8	V
Input High Voltage	V_{IH}			2.2	5.5**	V

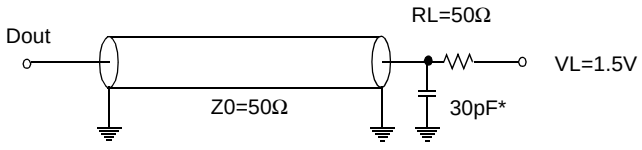
* V_{IL}(Min) = -3.0V(Pulse Width≤20ns)
** In Case of I/O Pins, the Max. V_{IH} = V_{DDQ} + 0.5V

TEST CONDITIONS

(T_A=0 to 70°C, V_{DD}=3.3V-5%/+10%unless otherwise specified)

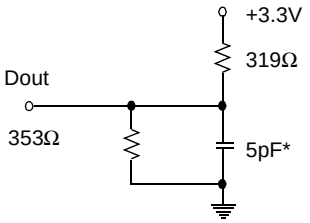
Parameter	Value
Input Pulse Level	0 to 3V
Input Rise and Fall Time(Measured at 0.3V and 2.7V)	2ns
Input and Output Timing Reference Levels	1.5V
Output Load	See Fig. 1

Output Load(A)



* Capacitive Load consists of all components of the test environment.

Output Load(B)
(for t_{LZC}, t_{LZOE}, t_{HZOE} & t_{HZC})



* Including Scope and Jig Capacitance

Fig. 1

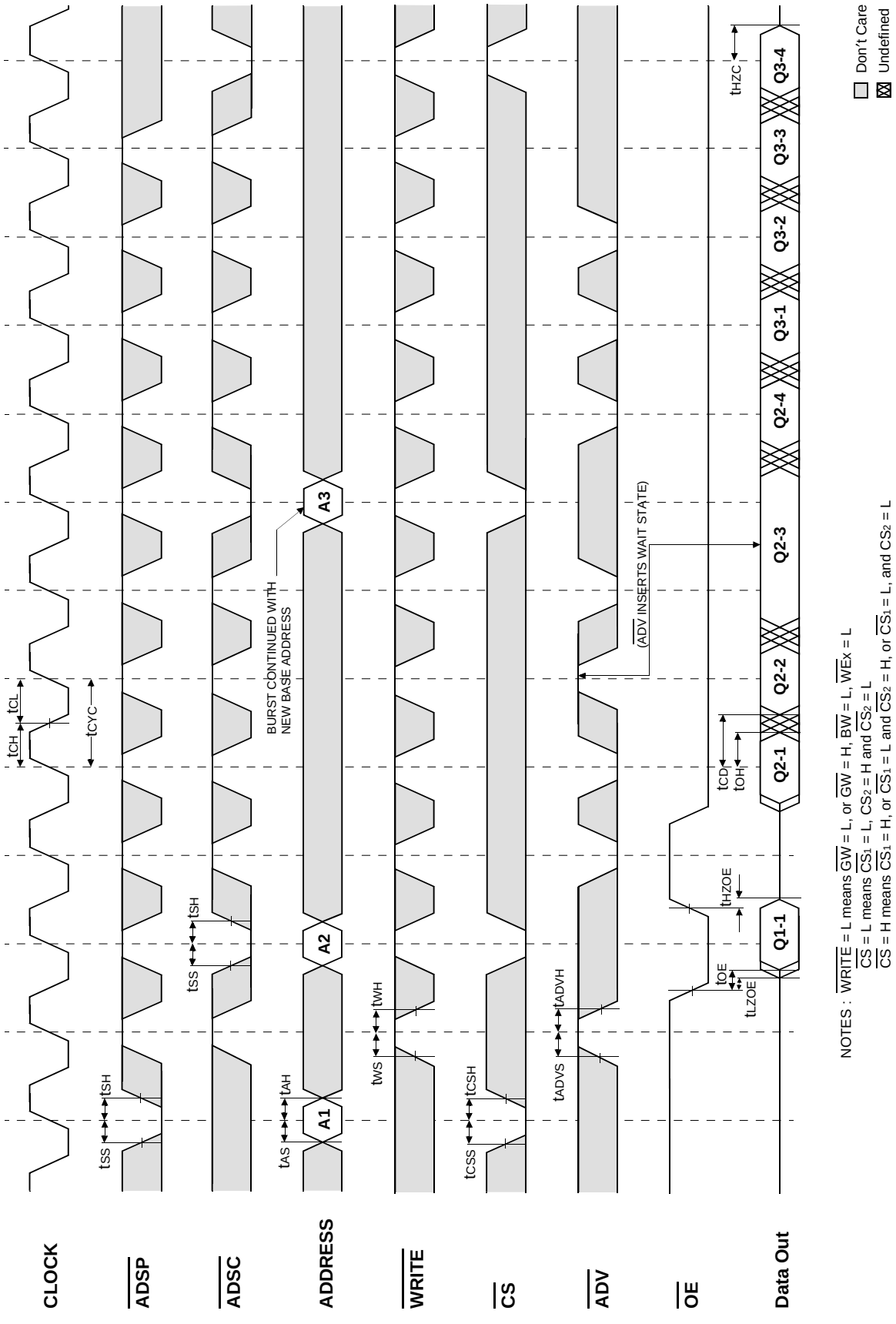
AC TIMING CHARACTERISTICS

(V_{DD}=3.3V-5%/+10%, T_A=0 to 70°C)

Parameter	Symbol	KM732V589A-13		KM732V589A-15		Unit
		Min	Max	Min	Max	
Cycle Time	t_{CYC}	13	-	15	-	ns
Clock Access Time	t_{CD}	-	7.0	-	8.0	ns
Output Enable to Data Valid	t_{OE}	-	6.0	-	7.0	ns
Clock High to Output Low-Z	t_{LZC}	0	-	0	-	ns
Output Hold from Clock High	t_{OH}	2.5	-	2.5	-	ns
Output Enable Low to Output Low-Z	t_{LZOE}	0	-	0	-	ns
Output Enable High to Output High-Z	t_{HZOE}	-	4.0	-	4.0	ns
Clock High to Output High-Z	t_{HZC}	1.5	5.0	2.0	6.0	ns
Clock High Pulse Width	t_{CH}	4.5	-	6.0	-	ns
Clock Low Pulse Width	t_{CL}	4.5	-	6.0	-	ns
Address Setup to Clock High	t_{AS}	2.5	-	2.5	-	ns
Address Status Setup to Clock High	t_{SS}	2.5	-	2.5	-	ns
Data Setup to Clock High	t_{DS}	2.5	-	2.5	-	ns
Write Setup to Clock High($\overline{GW}$, $\overline{BW}$, $\overline{WE_X}$)	t_{WS}	2.5	-	2.5	-	ns
Address Advance Setup to Clock High	t_{ADVS}	2.5	-	2.5	-	ns
Chip Select Setup to Clock High	t_{CSS}	2.5	-	2.5	-	ns
Address Hold from Clock High	t_{AH}	0.5	-	0.5	-	ns
Address Status Hold from Clock High	t_{SH}	0.5	-	0.5	-	ns
Data Hold from Clock High	t_{DH}	0.5	-	0.5	-	ns
Write Hold from Clock High($\overline{GW}$, $\overline{BW}$, $\overline{WE_X}$)	t_{WH}	0.5	-	0.5	-	ns
Address Advance Hold from Clock High	t_{ADVH}	0.5	-	0.5	-	ns
Chip Select Hold from Clock High	t_{CSH}	0.5	-	0.5	-	ns
ZZ High to Power Down	t_{PDS}	2	-	2	-	cycle
ZZ Low to Power Up	t_{PUS}	2	-	2	-	cycle

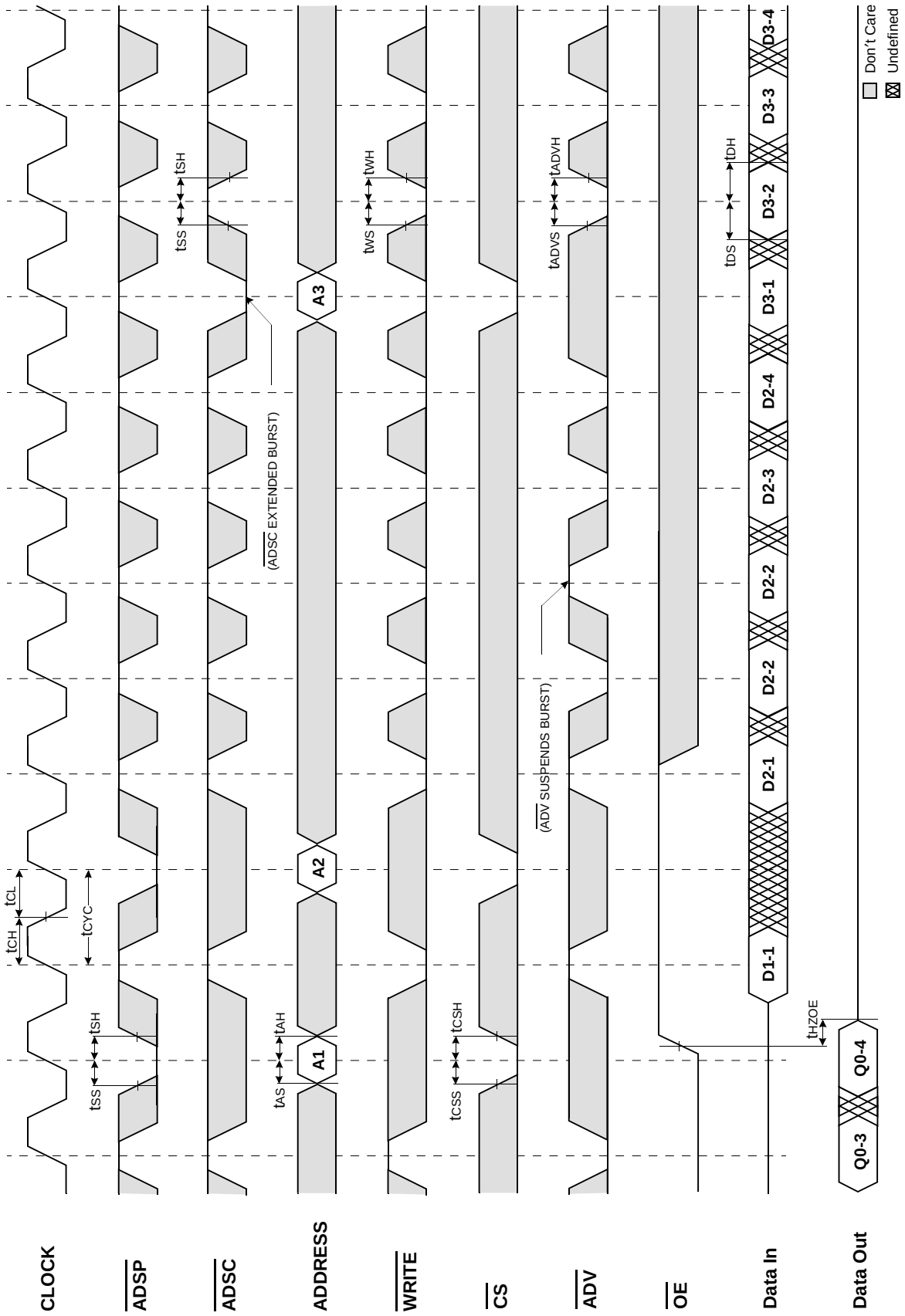
NOTE : 1. All address inputs must meet the specified setup and hold times for all rising clock edges whenever $\overline{ADSC}$ and/or $\overline{ADSP}$ is sampled low and CS is sampled low. All other synchronous inputs must meet the specified setup and hold times whenever this device is chip selected.
2. Both chip selects must be active whenever ADSC or ADSP is sampled low in order for the this device to remain enabled.
3. ADSC or ADSP must not be asserted for at least 2 Clock after leaving ZZ state.

TIMING WAVEFORM OF READ CYCLE

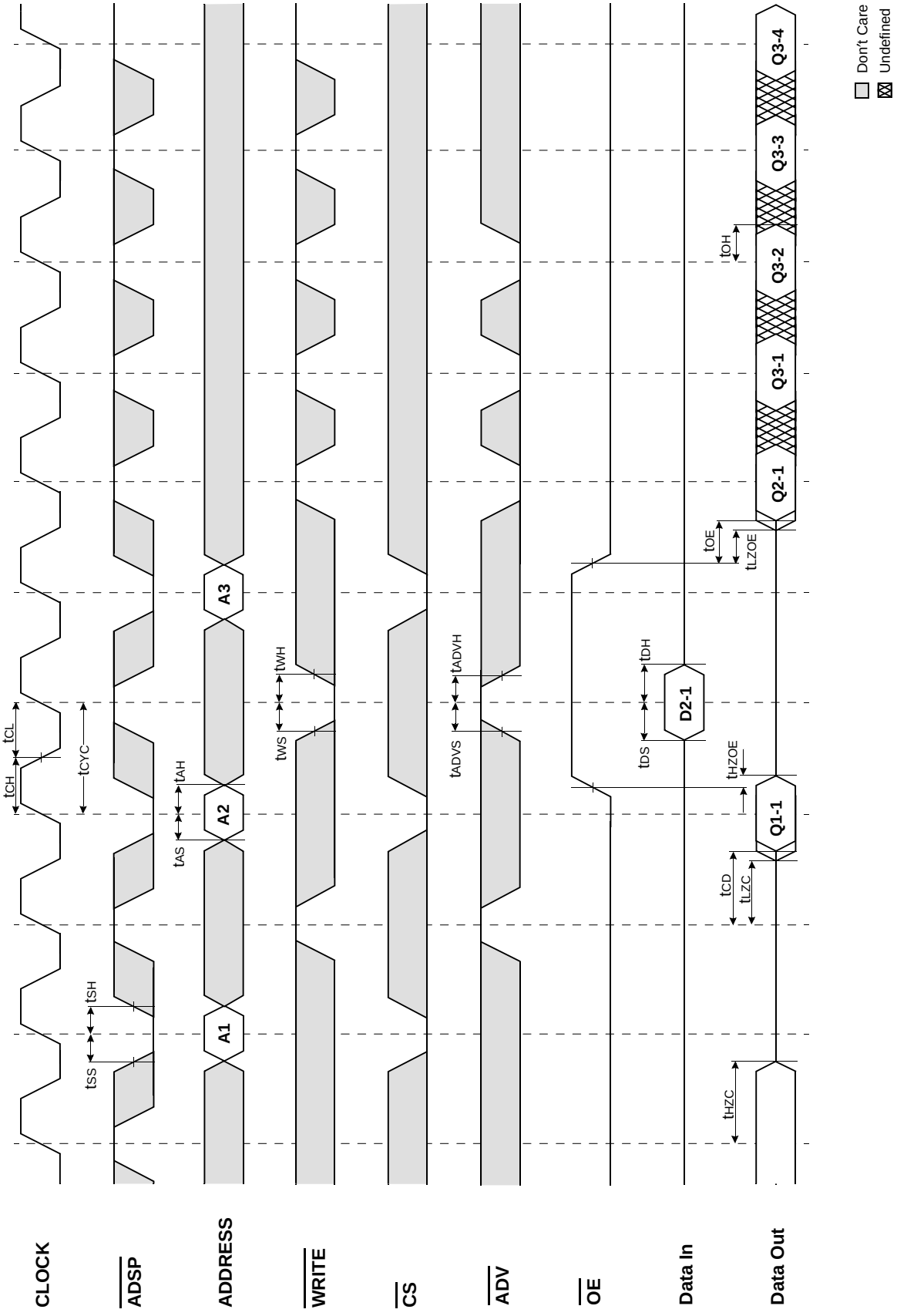


NOTES : $\overline{WRITE}$ = L means $\overline{GW}$ = L, or $\overline{GW}$ = H, $\overline{BW}$ = L, $\overline{WE}$x = L
$\overline{CS}$ = L means $\overline{CS_1}$ = L, CS_2 = H and $\overline{CS_2}$ = L
$\overline{CS}$ = H means $\overline{CS_1}$ = H, or $\overline{CS_1}$ = L and $\overline{CS_2}$ = H, or $\overline{CS_1}$ = L, and CS_2 = L

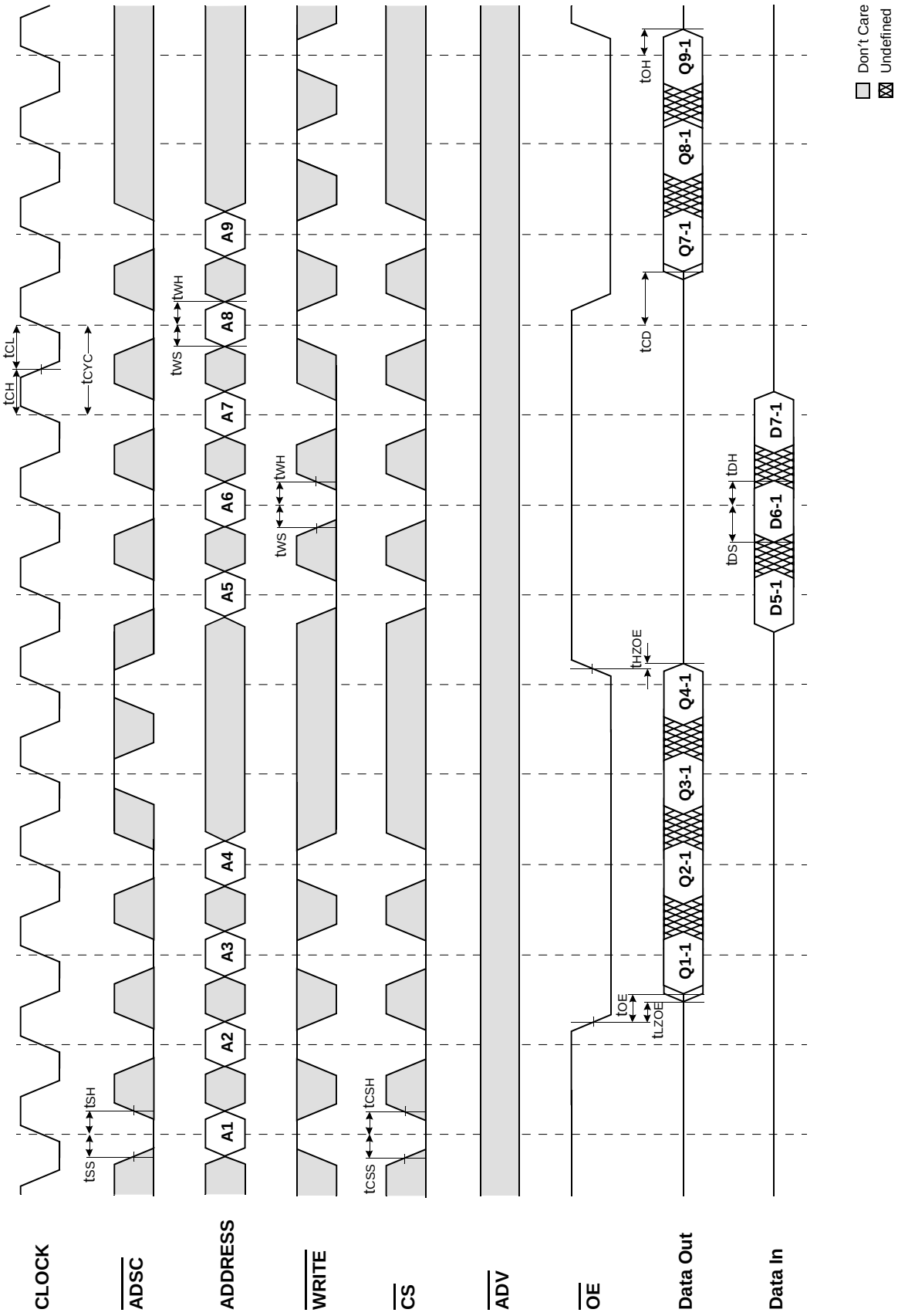
TIMING WAVEFORM OF WRTE CYCLE



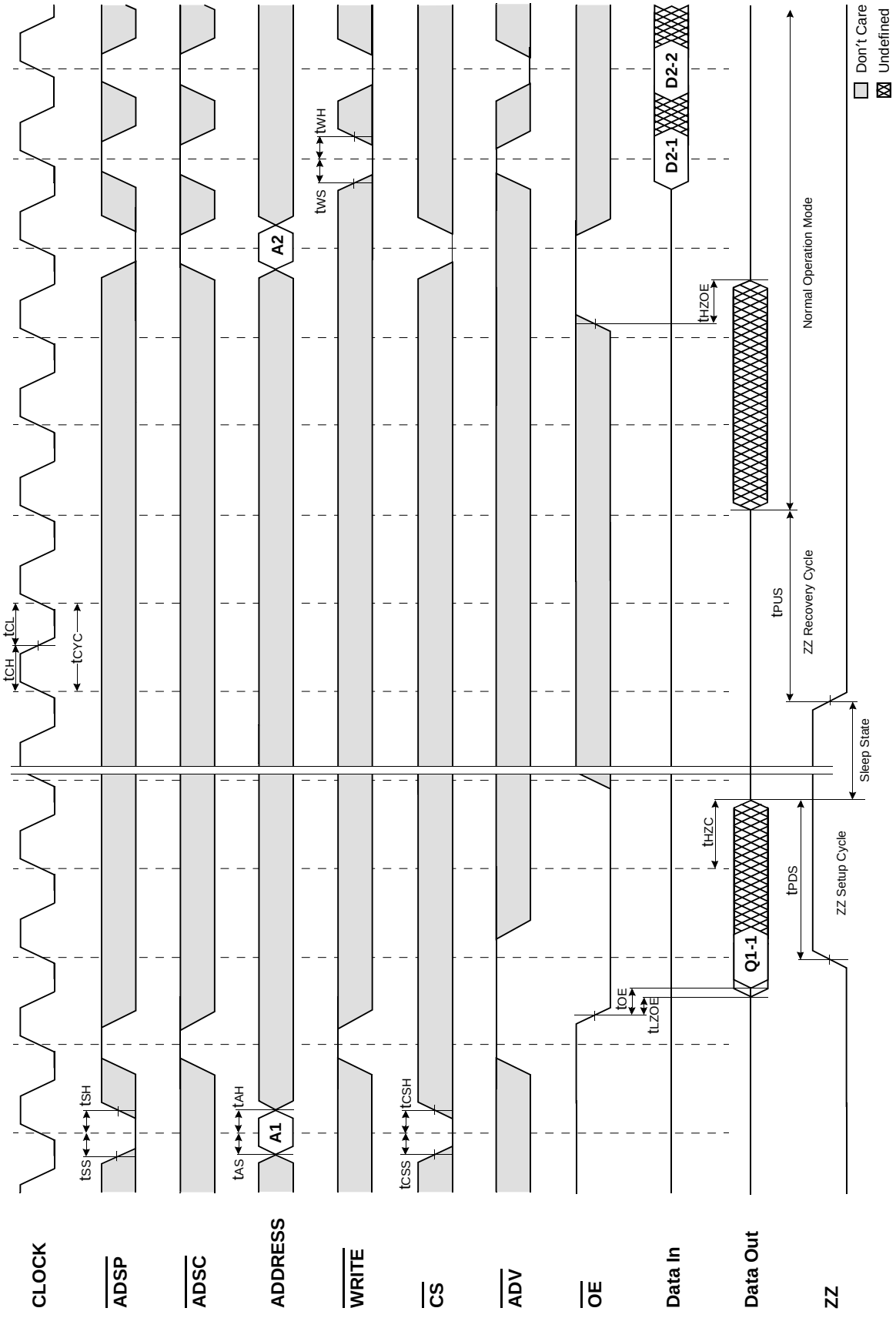
TIMING WAVEFORM OF COMBINATION READ/WRTE CYCLE



TIMING WAVEFORM OF SINGLE READ/WRITE CYCLE



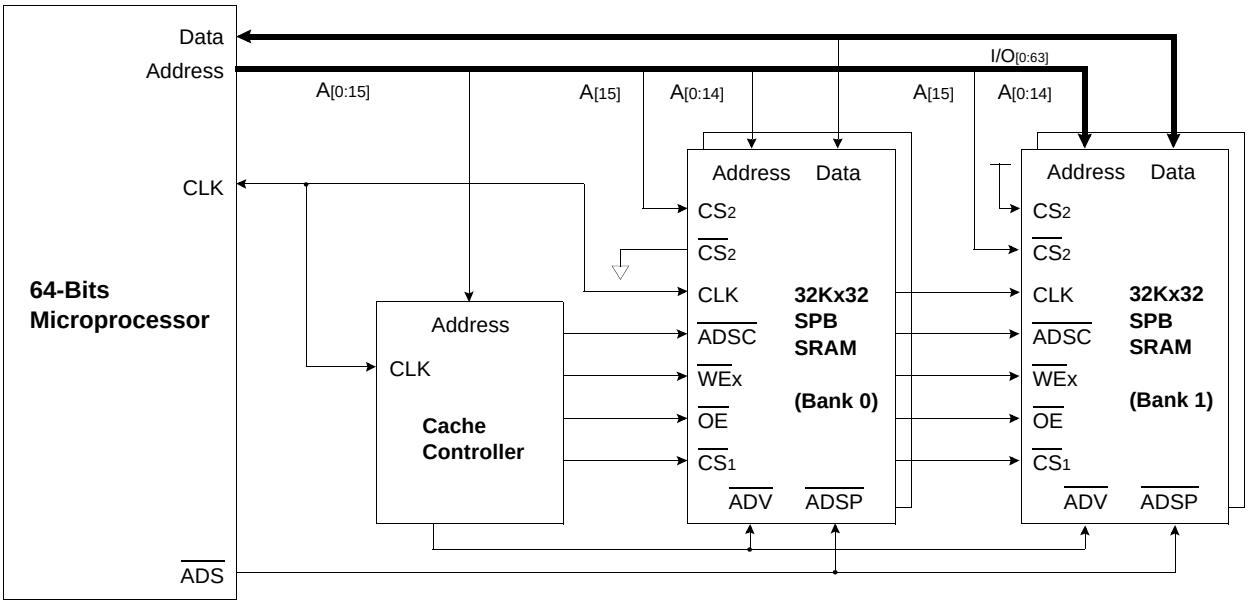
TIMING WAVEFORM OF POWER DOWN CYCLE



APPLICATION INFORMATION

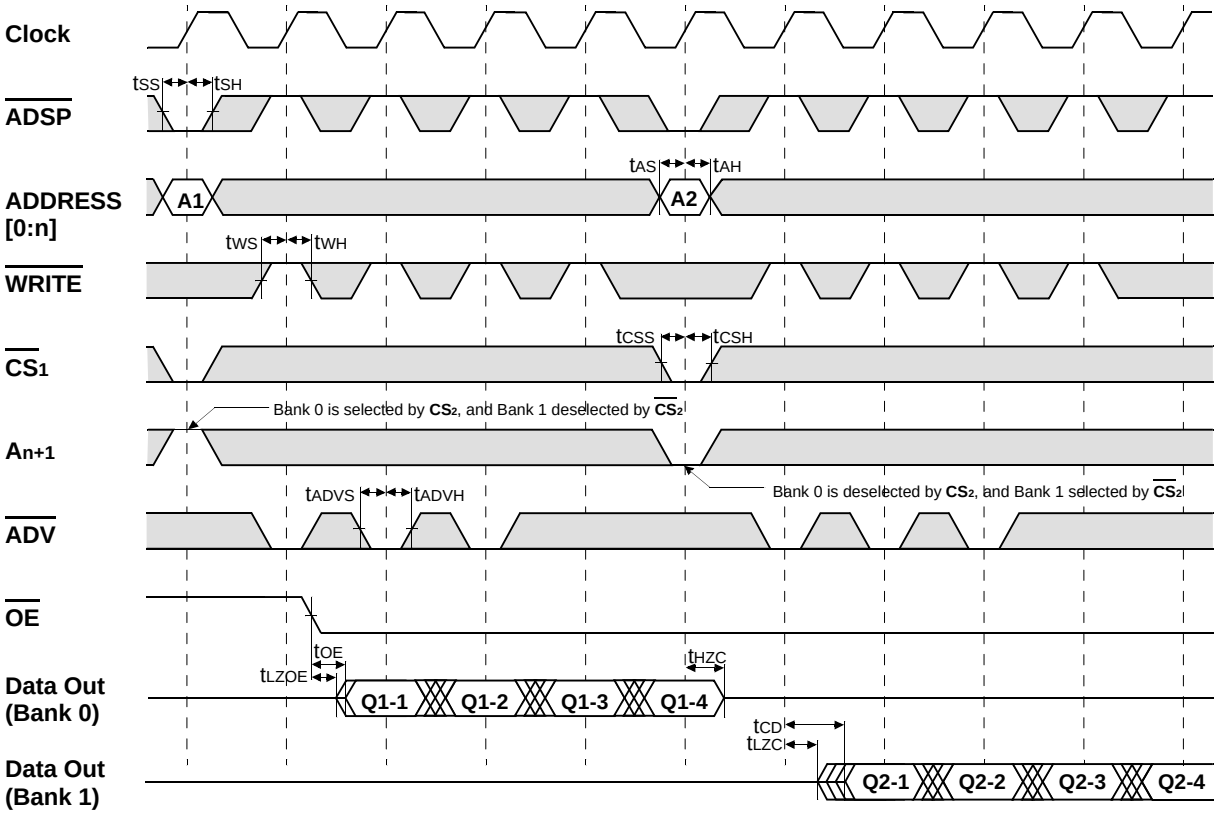
DEPTH EXPANSION

The Samsung 32Kx32 Synchronous Pipelined Burst SRAM has two additional chip selects for simple depth expansion. This permits easy secondary cache upgrades from 32K depth to 64K depth without extra logic.



* Please refer to attached timing diagram 2

INTERLEAVE READ TIMING (Refer to non-interleave write timing for interleave write timing)



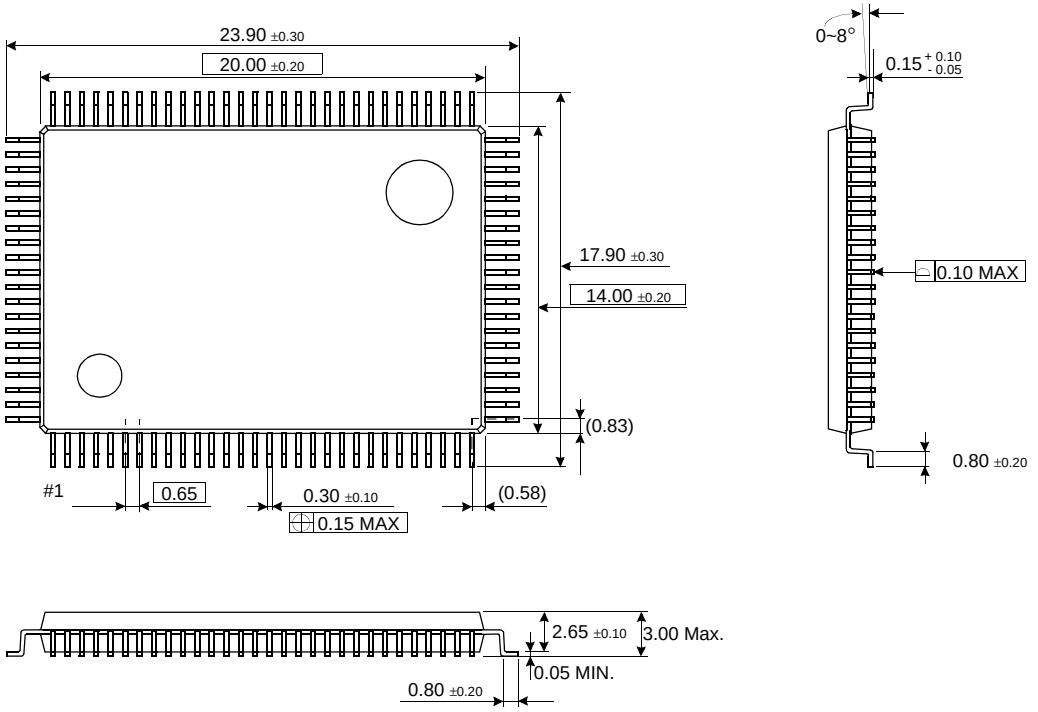
***NOTES** n = 14 32K depth, **15 64K depth, 16 128K depth, 17 256K depth**

Don't Care Undefined

PACKAGE DIMENSIONS

100-QFP-1420C

Units:millimeters/inches



100-TQFP-1420A

Units:millimeters/inches