A Semtech Company

Zero-Power Keyboard Encoder & Power Management IC for Intel StrongARM™ H/PCs

USAR H/PC ICs family
product specifications

Description

The USAR UR5HCSPI-SA01 SPICoder™, a member of USAR's H/PC IC product family, is a keyboard encoder and power management IC designed specifically for Handheld PCs (H/PCs), Web Phones and other systems that run Microsoft® Windows CE® and utilize the Intel StrongARM™processor.

The UR5HCSPI-SA01 offers several features necessary to H/PCs, including low power consumption, real estate-saving size, and special keyboard modes.

The IC operates at Zero-Power™ (less than 2µA @ 3V), providing the the host system both power management and I/O flexibility, with minimal battery drainage. Unlike the UR5HCSPI-SA, the SA01 does not offer Lid function.

Special keyboard modes and built-in power management features allow the USAR SPICoder™ SA01 to operate in harmony with the power management modes of Windows CE®, resulting in greater user flexibility, and longer battery life.

The IC will scan, debounce and encode an 8 x 14 keyboard matrix. It communicates with the Host over the SPI channel, implementing a high-reliability two-way protocol. The UR5HCSPI-SA01 also offers programmable features for wake-up keys and general purpose I/O pins.

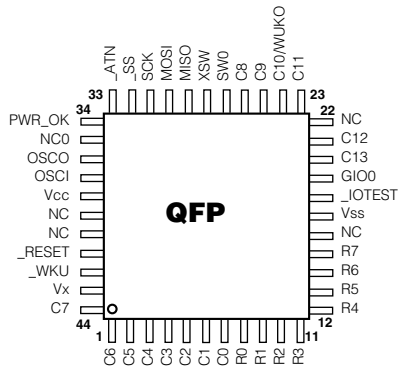
Features

- SPI-compatible keyboard encoder and power management IC; other interfaces available
- Ideal for use with the Intel StrongARM™ processor
- Operates at patented Zero-Power™ — typically consuming less than 2µA, between 3-5V
- Offers overall system power management capabilities
- Available in 10mm by 10mm, 44-pin low profile QFP package; other packaging available
- Implements high-reliability two-way protocol
- Fully compatible to the WinCE® keyboard specification
- Works in harmony with the power management modes of WinCE®
- Provides special modes of operation for H/PCs, including programmable "wake-up" keys
- Scans an 8 x 14 matrix; controls discrete switches and LED indicators
- Compatible with "system-on silicon" CPUs for H/PCs

Applications

- StrongARM™ Handheld PCs
- Windows CE® Platforms
- Web Phones
- Personal Digital Assistants (PDAs)
- Wearable Computers
- Internet Appliance

Pin Assignments

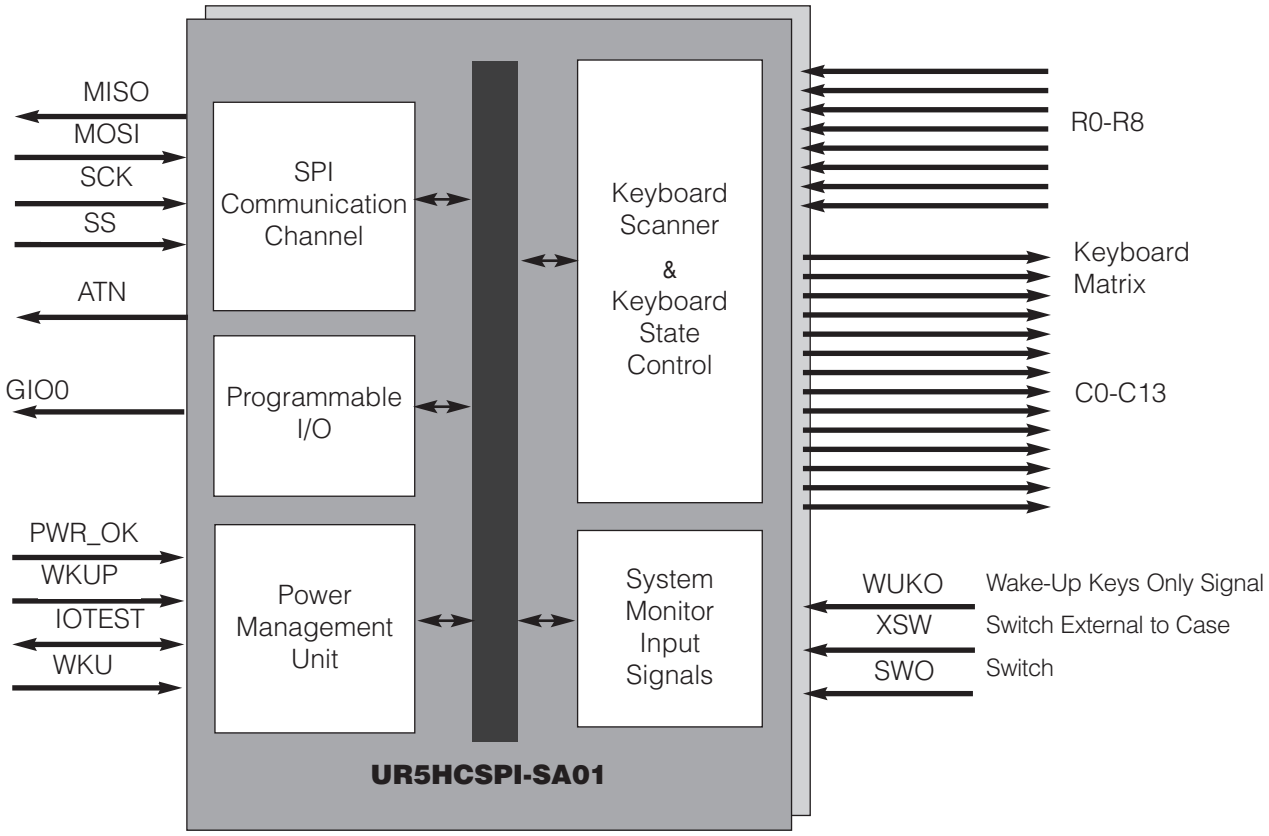


UR5HCSPI-SA01-FB
44-pin QFP
(0.80 mm pitch
(10x10 mm)

Ordering Code

Package options	Pitch In mm's	TA = -40°C to +85°C
44-pin, Plastic PLCC	1.27 mm	UR5CSPI-SA-FN
44-pin, Plastic QFP	0.8 mm	UR5CSPI-SA-FB

Block Diagram



Functional Description

The UR5HCSPI-SA01 consists functionally of five major sections (see the Functional Diagram on page 2). These are the Keyboard Scanner and State control, the Programmable I/O, the SPI Communication Channel, the System Monitor and the Power Management unit. All sections communicate with each other and operate concurrently.

Pin Definitions

Mnemonic	PLCC	QFP		Type	Name and Function
VCC	44	38		I	**Power Supply:** 3-5V
VSS	22	17		I	**Ground**
VX	4	43	-	I	Tie to VCC
OSCI	43	37		I	**Oscillator input**
OSCO	42	36		O	**Oscillator output**
_RESET	1	41		I	**Reset:** apply 0V to provide orderly start-up
MISO	34	29		O	**SPI Interface Signals**
MOSI	35	30		I	
SCK	36	31		I	
_SS	37	32		I	**Slave Select:** If not used tie to VSS
_IOTEST	24	18		O	**Wake-Up Control Signals**
_WKU	2	42		I	
R0-R4	13-17	8-12		I	**Row Data Inputs**
R5-R7	19-21	13-15		I	Port provides internal pull-up resistors
C0-C5	12-7	7-2		O	**Column Select Outputs:**
C6-C7	6-5	1,44		O	
C8-C9	31-30	26-25		O	
C11	28	23		I/O	
C12	27	21		O	
C13	26	20		O	
					Multi-function pins
C10/WUKO	29	24		I/O	C10 & “Wake-Up Keys Only” imput
					Miscellaneous functions
GI00	25	19		I/O	General programmable I/O
XSW	33	28		I	External discrete switch
SWO	32	27		I	Discrete switch
					Power Management Pins
_ATN	38	33		O	CPU Attention Output
_PWR_OK	39	34		I	Power OK Input
NC	3,18 23,40	39-40 16,22			**No Connects**: these pns are unused
NC0	41	35			NC0 should be tied to VSS or GND

Note: An underscore before a pin mnemonic denotes an active low signal.

Pin Descriptions

VCC and VSS

VCC and VSS are the power supply and ground pins. The UR5HCSPI-SA01 will operate from a 3-5 Volt power supply. To prevent noise problems, provide bypass capacitors placed as close as possible to the IC with the power supply. VX, where available, should be tied to Vcc.

OSCI and OSCO

OSCI and OSCO provide the input and output connections for the on-chip oscillator. The oscillator can be driven by any of the following circuits:
- Crystal
- Ceramic Resonator
- External Clock Signal

The frequency of the on-chip oscillator is 2 MHz.

_RESET

A logic zero on the _RESET pin will force the UR5HCSPI-SA01 into a known start-up state. The reset signal can be supplied by any of the following circuits:
- RC
- Voltage monitor
- Master system reset

MOSI, MISO, SCK, _SS, _ATN

These five signals implement the SPI interface. The device acts as a slave on the SPI bus. The _SS (Slave Select) pin must go high between successive characters in an SPI message or it will cause a write collision error. The _ATN pin is asserted low each time the UR5HCSPI-SA01 has a packet ready for delivery. For a more detailed description, refer to the SPI Communication Channel section on page 11 of this document.

_IOTEST and _WKU

The_IOTEST and _WKU pins ("Input Output Test" and "Wake Up") pins control the stop mode exit of the device. The designer can connect any number of active low signals to these two pins through a 15K resistor, in order to force the device to exit the stop mode. A sample circuit is shown on page 17 of this document. All the signals are "wire-anded." When any one of these signals is not active, it should be floating (i.e., these signals should be driven from "open-collector" or "open-drain" outputs). Other configurations are possible; contact the factory.

R0-R7

The R0-R7 pins are connected to the rows of the scanned matrix. Each pin provides an internal pull-up resistor, eliminating the need for external components.

C0 to C9 and C11

Pins C0 to C9 are bi-directional pins and are connected to the columns of the scanned matrix. When a column is selected, the pin outputs an active low signal. When the column is de-selected, the pin turns into high-impedance.

C10/WUKO

The C10/WUKO pin acts alternatively as column scan output and as an input. As an input, the pin detects the "Wake-Up Keys Only" signal, typically provided by the host CPU to indicate that the user has turned the unit off. When the device detects an active high state on this pin, it feeds this information into the "Keyboard State Control" unit, in order to disable the keyboard and enable the programmed wake-up keys.

To achieve maximum power savings, the resistor connected to WUKO can be as large as 1.5 MOhm.

Pin Descriptions, Cont.

C12 and C13

C12 and C13 are used as additional column pins in order to accommodate larger-size keyboards, such as the Fujitsu FKB1406 palmtop keyboard. GIO0 is a programmable input/output switch or LED pin; it can also be used as a wake-up signal. Its programming is explained on page 9 of this document.

XSW

The XSW pin is dedicated to an external switch. This pin is handled differently than the rest of the switch matrix and is intended to be connected to a switch physically located on the outside of the unit.

SW0

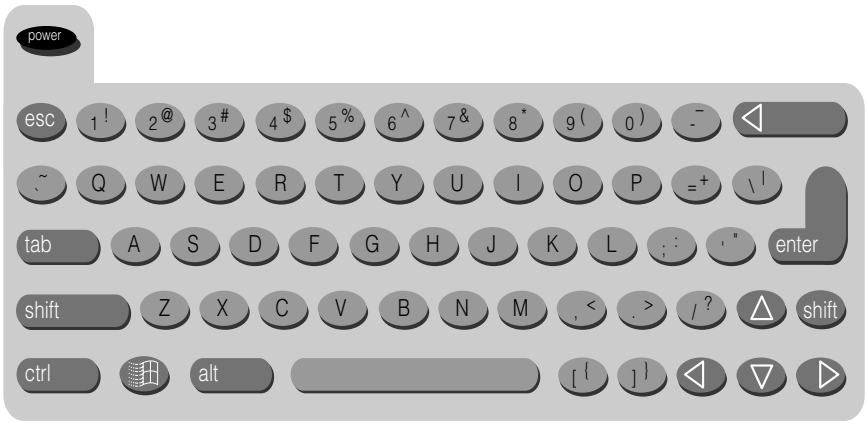
The SW0 pin is a dedicated input pin for a switch.

PWR_OK

The PWR_OK is an active low pin that monitors the battery status of the unit. When the UR5HCSPI-SA01 detects a transition from high to low on this pin, it will immediately enter the STOP mode, turn the LED off and remain in this state until the batteries of the unit are replaced and the signal is deasserted.

The Windows CE® Keyboard

The following illustration shows a typical implementation of a Windows CE® keyboard.



Windows CE® does not support the following keyboard keys typically found on desktop and laptop keyboards:

- INSERT
- SCROLL LOCK
- PAUSE
- NUM LOCK
- Function Keys (F1-F12)
- PRINT SCREEN

If the keyboard implements the Windows key, the following key combinations are supported in the Windows CE® environment:

Key Combination	Result
Windows	Open Start Menu
Windows+K	Open Keyboard Tool
Windows+I	Open Stylus Tool
Windows+C	Open Control Panel
Windows+E	Explore the H/PC
Windows+R	Display the Run Dialog Box
Windows+H	Open Windows CE® Help
Ctrl+Windows+A	Select all on desktop

"Ghost" Keys

In any scanned contact switch matrix, whenever three keys defining a rectangle on the switch matrix are pressed at the same time, a fourth key positioned on the fourth corner of the rectangle is sensed as being pressed. This is known as the "ghost" or "phantom" key problem.

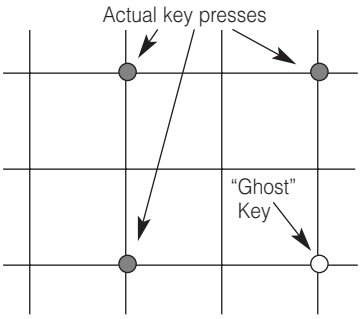


Figure 1: "Ghost" or "Phantom" Key Problem

Although the problem cannot be totally eliminated without using external hardware, there are methods to neutralize its negative effects for most practical applications. Keys that are intended to be used in combinations should be placed in the same row or column of the matrix, whenever possible. Shift Keys (Shift, Alt, Ctrl, Window) should not reside in the same row (or column) as any other keys. The UR5HCSPI-SA01 has built-in mechanisms to detect the presence of "ghost" keys.

Keyboard Scanner

The encoder scans a keyboard organized as an 8 row by 14 column matrix for a maximum of 112 keys. Smaller size matrixes can also be accommodated by simply leaving unused pins open. The UR5HCSPI-SA01 provides internal pull-ups for the Row input pins. When active, the encoder selects one of the column lines (C0-C13) every 512 µS and then reads the row data lines (R0-R7). A key closure is detected as a zero in the corresponding position of the matrix.

A complete scan cycle for the entire keyboard takes approximately 9.2 mS. Each key found pressed is debounced for a period of 20 mS. Once the key is verified, the corresponding key code(s) are loaded into the transmit buffer of the SPI communication channel.

Keyboard Scanning

N-Key Rollover

In this mode, the code(s) corresponding to each key press are transmitted to the host system as soon as that key is debounced, independent of the release of other keys.

When a key is released, the corresponding break code is transmitted to the host system. There is no limitation to the number of keys that can be held pressed at the same time. However, two or more key closures, occurring within a time interval of less than 5mS, will set an error flag and will not be processed. This feature is to protect against the effects of accidental key presses.

Keyboard States

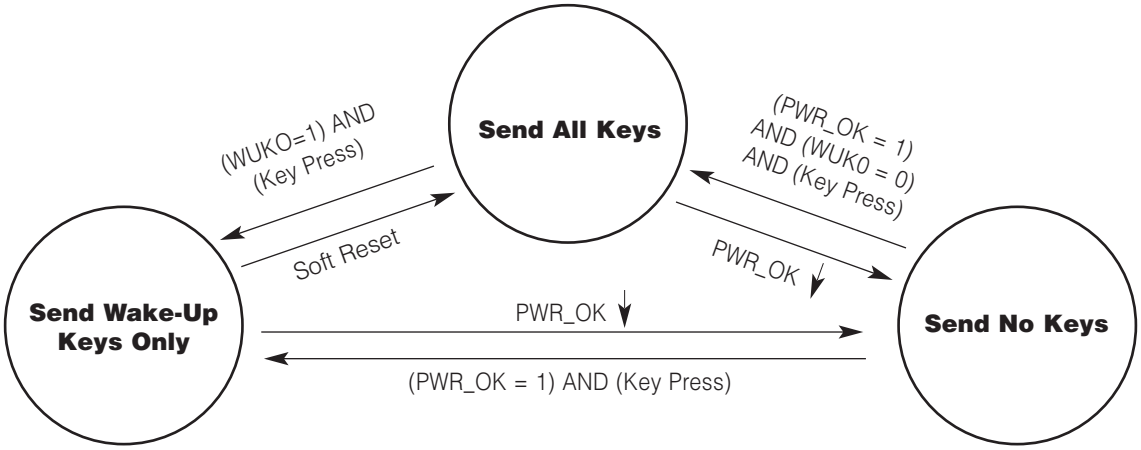


Figure 2: The UR5HCSPI-SA01 implements three modes of keyboard and switch operation.

These states of operation refer only to the keyboard functionality and, although they are related to power states, they are also independent of them.

"Send All Keys"

Entry Conditions: Power on reset, soft reset, PWR_OK =1, {(WUKO=0)}

Exit Conditions: PWR_OK = 0 -> "Send No Keys"(WUKO=1) AND (Key Press) -> "Send Wake-Up Keys Only"(LID = 0) AND (WUKO=0) AND (Key Press) -> "Send XSW Key Only"

Description: This is the UR5HCSPI-SA01's normal state of operation, accepting and transmitting every key press to the system. This state is entered after the user powers on the unit and it is sustained while the unit is being used.

"Send Wake-Up Keys Only"

Entry Conditions: (WUKO=1) AND (Key or Switch press)

Exit Conditions: Soft Reset -> "Send All Keys"PWR_OK = 0 -> "Send No Keys"

Description: This state is entered when the user turns the unit off. A signal line driven by the host will notify the UR5HCSPI-SA01 about this state transition. While in this state, the UR5HCSPI-SA01 will transmit only keys programmed to be wake-up keys to the system. It is not necessary for the UR5HCSPI-SA01 to detect this transition in real time, since it does not affect any operation besides buffering keystrokes.

"Send No Keys"

Entry Conditions: PWR_OK transition from high to low

Exit Conditions: (PWR_OK = 1) AND (Matrix key pressed OR Switch OR _WKUP)

Description: This state is entered when a PWR_OK signal is asserted (transition high to low), indicating a critically low level of battery voltage. The PWR_OK signal will cause an interrupt to the UR5HCSPI-SA01, which guarantees that the transition is performed in real time. While in this state, the UR5HCSPI-SA01 will perform as follows:

1. The LED will be turned off. Nevertheless, its state is saved and will be restored after exiting the disabled state (change of batteries).

2. The UR5HCSPI-SA01 will enter the STOP mode for maximum energy conservation.

3 Stop mode time-out entry will be shortened to further conserve energy.

4. While in this state all interrupts are disabled. The UR5HCSPI-SA01 will exit this state on the next interrupt event that detects the PWR_OK line has been de-asserted.

Key Map for the Fujitsu FKB1406 (UR5HCSPI-SA01)

Rows (R0–R6) \ Columns (C0–C13)	0	1	2	3	4	5	6	7	8	9	10	11	12	13
0	LAlt	`		LCtrl	FN	Esc	1 F1	2 F2	9 F9	0 F10	- NmLk	+ Bk		BkSp
1		\	LSft			Del		T	Y	U Pad 4	I Pad 5	Enter	RShift	↓ PgDn
2		TAB				Q	W	E	R	O Pad 6	P Ins	[Pause		] ScrLk
3		Z				CapLk			K Pad 2	L Pad 3	; PrtScr	‘ SysReq		↑ PgUp
4		A				S	D	F	G	H	J Pad 1	/ /		← Home
5		X				C	V	B Pad 0	N	M	,	.		Spc
6						3 F3	4 F4	5 F5	6 F6	7 F7	8 F8	Prog		→ End

Keyboard Layout for Fujitsu FKB1406

Key Codes

Key codes range from 01H to 73H and are arranged as follows:

Make code = column_number * 8 + row_number + 1

Break code = Make code OR 80H

Discrete Switches transmit the following codes:

XSW = 71H

SW0 = 72H

GIO0 = 73H

GIO0 Pin

The UR5HCSPI-SA01 provides a general purpose pin, GIO0, that can be programmed as Input, Output, Debounced Switch Input or LED Output. The programmable I/O pin can be configured to the desired mode through a command from the system. After the I/O pin is configured, the host system can read or write data to it. If the pin is configured as a Debounced Switch, it will return scan codes.

For Pin GIO0:

I/O Number = 0
LED Number = 0

Input Mode

While in the Input Mode, the GIO0 pin will detect input signals and report the input status to system as required.

Output Mode

In the Output Mode, the UR5HCSPI-SA01 will control the output signal level according to the system command. When the pin is set at Output Mode, the default output is low.

Switch Input Mode

In Switch Input Mode, the UR5HCSPI-SA01 will generate an individual make key code when the switch closes (pin goes low), and a break key code when the switch returns to open (pin goes to high). The switches generate key codes outside of those generated by the key matrix, from 71H - 73H. When the switch closes, the USAR SPICoder™ will not fall asleep.

Pin Configurations

When prototyping, caution should be taken to ensure that programming of the GIO0 pin does not conflict with the circuit implemented. A series protection resistor is recommended for protection from improper programming of the pin.

After a power-on or soft reset, GIO0 defaults to the Input state.

The following drawing illustrates the suggested interface to the general purpose input/output pin.

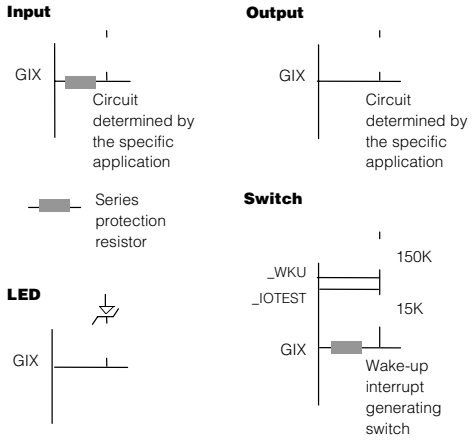


Figure 3: Suggested interface of general purpose input/output pin

LED Modes

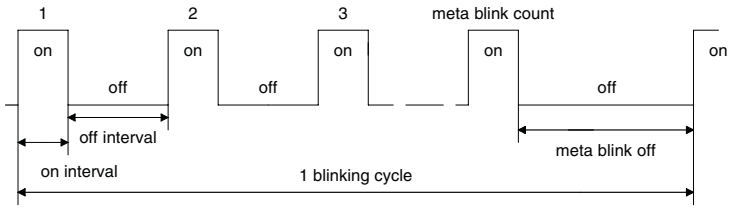


Figure 4: Timing chart: the behavior of an LED using the settings,1: LED on; 0: LED off.

There are three LED modes: off, on, and blinking. The LED can be individually set to one of these modes. In the Blinking Mode, both the on-interval and the off-interval can be individually set. Additionally, a meta blink count and meta blink interval may be specified. This describes an interval of a different length which may be inserted after each specified number of blinks. All the intervals are based on a 1/16th of a second duration. When the LED is on or blinking, the USAR SPICoder™ will not enter the STOP Mode unless the PWR_OK signal is asserted low. In this case, the device will save the status of the LED and turn it off. The default LED mode is off.

The above timing chart describes the behavior of an LED using these settings,1: LED on; 0: LED off.

SPI Communication Channel

SPI data transfers can be performed at a maximum clock rate of 500 KHz. When the UR5HCSPI-SA01 asserts the _ATN signal to the host Master, the data will have already been loaded into the data register waiting for the clocks from the master. One _ATN signal is used per each byte transfer. If the host fails to provide clock signals for successive bytes in the data packet within 120 mS, the transmission will be aborted and a new session will be initiated by asserting a new _ATN signal. In such a case, the whole packet will be re-transmitted.

If the SPI transmission fails 20 times consecutively, the synchronization between the master and slave may be lost. In this case, the UR5HCSPI-SA01 will enter the reset state.

When CPHA = 0, the shift clock is the OR of _SS with SCK; therefore, _SS must go high between successive characters in an SPI message. The master can assert _SS low only when it is getting ready to transmit or receive. After the last bit is shifted out, _SS must go high within 60 µS.

The UR5HCSPI-SA01 implements the SPI communication protocol according to the following diagram:

CPOL = 0 ---------- SCK line idles in low state
CPHA = 0 ---------- SS line is an output enable control

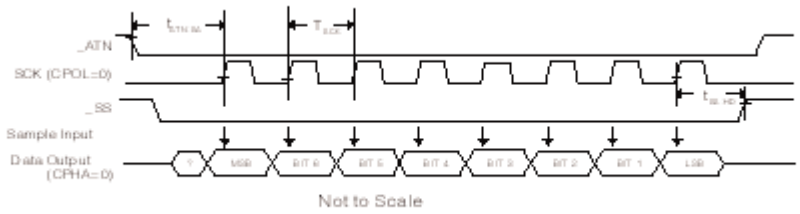


Figure 5: SPI Communication Protocol

When the host sends commands to the keyboard, the UR5HCSPI-SA01 requires that the minimum and maximum

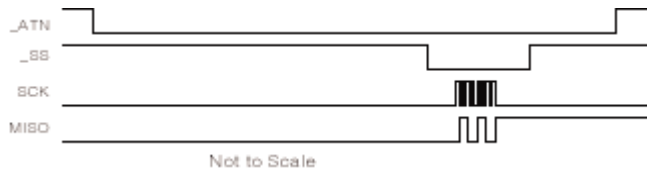


Figure 6: Transmitting Data Waveforms:

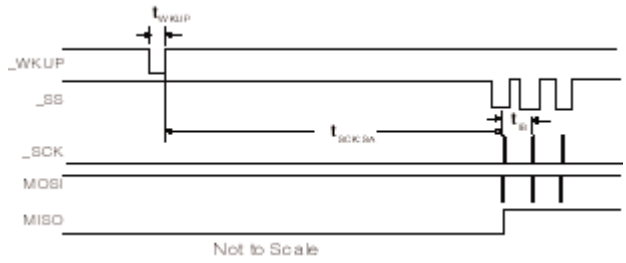


Figure 7: Receiving Data Waveforms

Data/Command Buffer

The UR5HCSPI-SA01 implements a data buffer that contains the key code/command bytes waiting to be transmitted to the host. If the data buffer is full, the whole buffer will be cleared and an "Initialize" command will be sent to the host. At the same time, the keyboard will be disabled until the "Initialize" or "Initialize Complete" command from the host is received.

SPI Communication Table

The following table describes the specific timing referenced in diagrams on page 12.

Signal Name	Description	Min	Max	Units
tATN:SA _	ATN to first clock pulse	-	120	mS
TSCK	Clock period	2	-	µS
tSS:HD	Last clock pulse to _SS de-asertion	-	60	µS
tWKUP	_WKUP pulse width	125	-	nS
tSCK:SA	_WKUP to first clock pulse	5	150	mS
tIB	Inter-byte period	0.2	5	mS

Power Management Unit

The UR5HCSPI-SA01 supports two modes of operation. The following table lists the typical and maximum supply current (no DC loads) for each mode at 3.3 Volts (+/- 10%).

Current	Typical	Max	Unit	Description
RUN	1.5 1	3.0	mA	Entered only while data/commands are in process and if the LEDs are blinking
STOP	2.0	20	µA	Entered after 125 mS of inactivity if LEDs islow

Power consumption of the keyboard sub-system will be determined primarily by the use of the LEDs. While the UR5HCSPI-SA01 is in the STOP mode, an active low Wake-Up Output from the Master must be connected to the edge-sensitive _WKU pin of the UR5HCSPI-SA01. This signal will be used to wake up the UR5HCSPI-SA01 in order to receive data from the Master host. The Master host will have to wait a minimum of 5 mS prior to providing clocks to the UR5HCSPI-SA01. The UR5HCSPI-SA01 will enter the STOP mode after a 125 mS period of keypad and/or host communications inactivity, or anytime the PWR_OK line is asserted low by the host. Note that while one or more keys are held pressed, the UR5HCSPI-SA01 will not enter the STOP mode until every key is released.

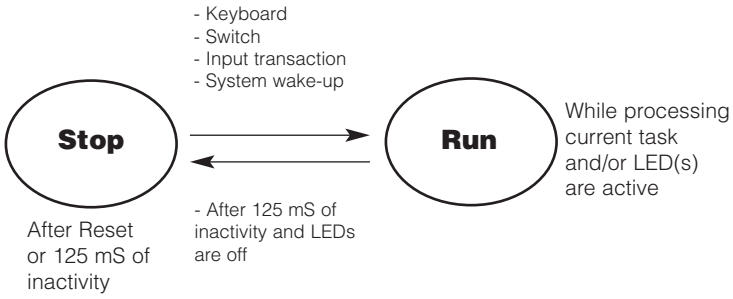


Figure 8: The Power States of the UR5HCSPI-SA01.

Communication Protocol

There are eight commands that may be sent from the UR5HCSPI-SA01 to the host, and ten commands that may be sent from the host to the UR5HCSPI-SA01.

Each command from UR5HCSPI-SA01 to the host is composed of a sequence of codes. All commands start with <CONTROL> code (80H) and end with LRC code (see the description of the LRC calculation on page 14). Command details are listed below.

Commands to the Host - Summary

Command Name	Code	Description
Initialize Request	AOH	Sent to the host when the data buffer is full
Initialize Complete	A1H	Issued upon completion of the “Initialize” command issued by the host
Heartbeat Response	A2H	Response to “Heartbeat Request” issued by the host
Identification Response	F2H	Response to “Identification Request” issued by the host
LED Status Report	A3H	Response to “LED Status Request”
Resend Request	A5H	Issued upon error during the reception of a packet
Input/Output Mode Status Report	A7H	Reports the status of GIO0 pin
Input/Output Data Report	A8H	Response to “I/O Data Request” command from the host

LRC Calculation

The LRC is calculated for the whole packet, including the Command Code and the Command Prefix. The LRC is calculated by first taking the bitwise exclusive OR of all bytes from the message. If the most significant bit (MSB) of the LRC is set, the LRC is modified by clearing the MSB and changing the state of the next most significant bit. Thus, the Packet Check Byte will never consist of a valid LRC with the most significant bit set.

Commands to the Host Analytically

Initialize Request:

<CONTROL>	80H	
<INIT>	A0H	
<LRC>	20H	

The UR5HCSPI-SA01 will send the Initialize Request Command to the host when its data buffer is full.

Initialization Complete

<CONTROL>	80H	
<INIT COMPLETE>	A1H	
<LRC>	21H	

The UR5HCSPI-SA01 wil send the Initialize Complete Report to the host when it finishes the initialization caused by Initialize Command from the host.

Heartbeat Response:

<CONTROL>	80H	
<ONLINE>	A2H	
<LRC>	22H	

The UR5HCSPI-SA01 will send the Heartbeat Response to the host when it receives the Heartbeat Request Command from the host.

Identification Response:

<CONTROL>	80H	
<ID>	F2H	
<Vendor>	02H	--- USAR
<Revision>	08H	--- Rev 0.8A
<Switch>	00H	.
<LRC>	7EH	

The UR5HCSPI-SA01 will send the Identification Response to the host when it receives the Identification Request Command from the host.

LRC Calculation, Cont.

The following C language function is an example of an LRC calculation program. It accepts two arguments: a pointer to a buffer and a buffer length. Its return value is the LRC value for the specified buffer.

```
char Calculate LRC (char  buffer,
size  buffer)
{
char LRC;
size_t index;
/*
* Init the LRC using the first two
message bytes.
*/
LRC = buffer [0] ^ buffer [1];
/*
* Update the LRC using the
remainder of the buffer.
*/
for (index = 2; index < buffer; index
++)
  LRC ^ = buffer[index];
/*
* If the MSB is set then clear the
MSB and change the next most
significant bit
*/
if (LRC & 0x80)
LRC ^ = 0xC0;
/* * Return the LRC value for the
buffer.*/}
```

Commands to the Host from the UR5HCSPI-SA01, Cont.

LED Status Report

<CONTROL>	80H	
<LED>	A3H	
<Status 0>	xxH	LED0 status:(0=OFF; 1=ON; 2=BLINKING; 3=NO LED MODE)
<Status 1>	xxH	LED1 status:(0=OFF; 1=ON; 2=BLINKING; 3=NO LED MODE)
<Status 2>	xxH	LED2 status:(0=OFF; 1=ON; 2=BLINKING; 3=NO LED MODE)
<LRC>	xxH	

The UR5HCSPI-SA01 will send the LED Status Report to the host when it receives the LED Status Request Command from the host.

Resend Request

<CONTROL>	80H	
<RESEND>	A5H	
<LRC>	25H	

The UR5HCSPI-SA01 will send this Resend Request Command to the host when its command buffer is full, or if it detects either a parity error or an unknown command during a system command transmission.

Input/Output Mode Status Report

<CONTROL>	80H	
<MODIO>	A7H	
<IO NUMBER>	xxH	IO number, 0
<IO MODE>	xxH	IO mode: (0=input; 1=output; 2=switch; 3=LED)
<LRC>	xxH	

The UR5HCSPI-SA01 will send the I/O Mode Status Report to the host when it receives the I/O Mode Status Request Command from the host, in order to report the status of the GIO0 pin.

Input/Output Data Report

<CONTROL>	80H	
<MODIO>	A8H	
<IO NUMBER>	xxH	IO number, 0
<IO DATA>	xxH	IO data: (0=low, 1=high)
<LRC>	xxH	

The UR5HCSPI-SA01 will send the I/O Data Report to the host when it receives the I/O Data Request Command from the host.

Commands from the Host to the UR5HCSPI-SA01

Each command to UR5HCSPI-SA01 is composed of a sequence of codes. All commands start with <ESC> code (1BH) and end with the LRC code (bitwise exclusive OR of all bytes).

Commands from the Host - Summary

Command Name	Code	Description
Initialize	AOH	Causes the UR5HCSPI-SA01 to enter the power-on state
Initialization Complete	A1H	Issued as a response to the "Initialize Request"
Heartbeat Request	A2H	The UR5HCSPI-SA01 will respond with "Heartbeat Response"
Identification Request	F2H	The UR5HCSPI-SA01 will respond with "Identification Response"
LED Status Request	A3H	The UR5HCSPI-SA01 will respond with "LED Status Response"
LED Modify	A6H	The UR5HCSPI-SA01 will change the LED accordingly
Resend Request	A5H	Issued upon error during the reception of a packet
Input/Output Mode Modify	A7H	The UR5HCSPI-SA01 will modify or report the status of the GIO0 pin
Output Data to I/O pin	A8H	The UR5HCSPI-SA01 will output a signal to the GIO0 pin
Set Wake-Up Keys	A9H	Defines which keys are "wake-up" keys

Commands from the Host to the UR5HCSPI-SA01 Analytically

Initialize:

<ESC> 1BH
<INIT> A0H
<LRC> 7BH

When the UR5HCSPI-SA01 receives this command, it will clear all buffers and return to the power-on state.

Initialization Complete

<ESC> 1BH
<INIT COMPLETE> A1H
<LRC> 7AH

When the UR5HCSPI-SA01 receives this command, it will enable transmission of keyboard data. Keyboard data transmission is disabled if the TX output buffer is full (32 bytes). Note that if the transmit data buffer gets full the encoder will issue an "Initialize Request" to the host.

Heartbeat Request

<ESC> 1BH
<ONLINE> A2H
<LRC> 79H

When the UR5HCSPI-SA01 receives this command, it will reply with the Heartbeat Response Report.

Identification Request

<ESC> 1BH
<ID> F2H
<LRC> 29H

the UR5HCSPI-SA01 will reply to this command with the Identification Response Report.

LED Status Request

<ESC> 1BH
<LED> A3H
<LRC> 78H

When UR5HCSPI-SA01 receives this command, it will reply with the LED Status Report.

Commands from the Host to the UR5HCSPI-SA01, Cont.

Set Wake-Up Keys:

<ESC>	1BH	
<SETMATRIX>	A9H	
<COL0>	xxH	

(R7 R6 R5 R4 R3 R2 R1 R0
Bitmap: 0-enabled 1-disabled)

<COL1>	xxH	
<COL2>	xxH	
<COL3>	xxH	
<COL4>	xxH	
<COL5>	xxH	
<COL6>	xxH	
<COL7>	xxH	
<COL8>	xxH	
<COL9>	xxH	
<COL10>	xxH	
<COL11>	xxH	
<COL12>*	xxH	
<COL13>*	xxH	
<SWITCHES>	xxH	

(where SWITCHES bit assignments are = x x x x GIO0 SW0 XSW)

<LRC>	xxH	

The "Set Wake-Up Keys" command is used to disable specific keys from waking up the host. Using this command, the host can set only a group of keys to act as "power-on" switches. The host can change the keyboard behavior dynamically according to the system power management requirements. The default after power on is “All Keys Enabled.”

LED Modify

<ESC>	1BH	
<MODLED>	A6H	
<LED NUMBER>	xxH	LED number (0)
<LED STATE>	xxH	(0=LED OFF; 1=LED ON; 2=LED BLINKING)
<ON INTERVAL>	xxH	Time in 1/16ths of a second for LED to be on
<OFF INTERVAL>	xxH	Time in 1/16ths of a second for LED to be off
<META COUNT>	xxH	Number of blinks after which to apply meta blink interval
<META INTERVAL>	xxH	Time in 1/16ths of a second for LED to be off after <META COUNT> blinks
<LRC>	xxH	

When the UR5HCSPI-SA01 receives this command, it will change the LED mode accordingly.

I/O Mode Modify

<ESC>	1BH	
<MODIO>	A7H	
<IO NUMBER>	xxH	IO number: 0
<IO MODE>	xxH	IO mode: (0=input, 1=output, 2=switch, 3=LED, 4=current mode request)
<LRC>	xxH	

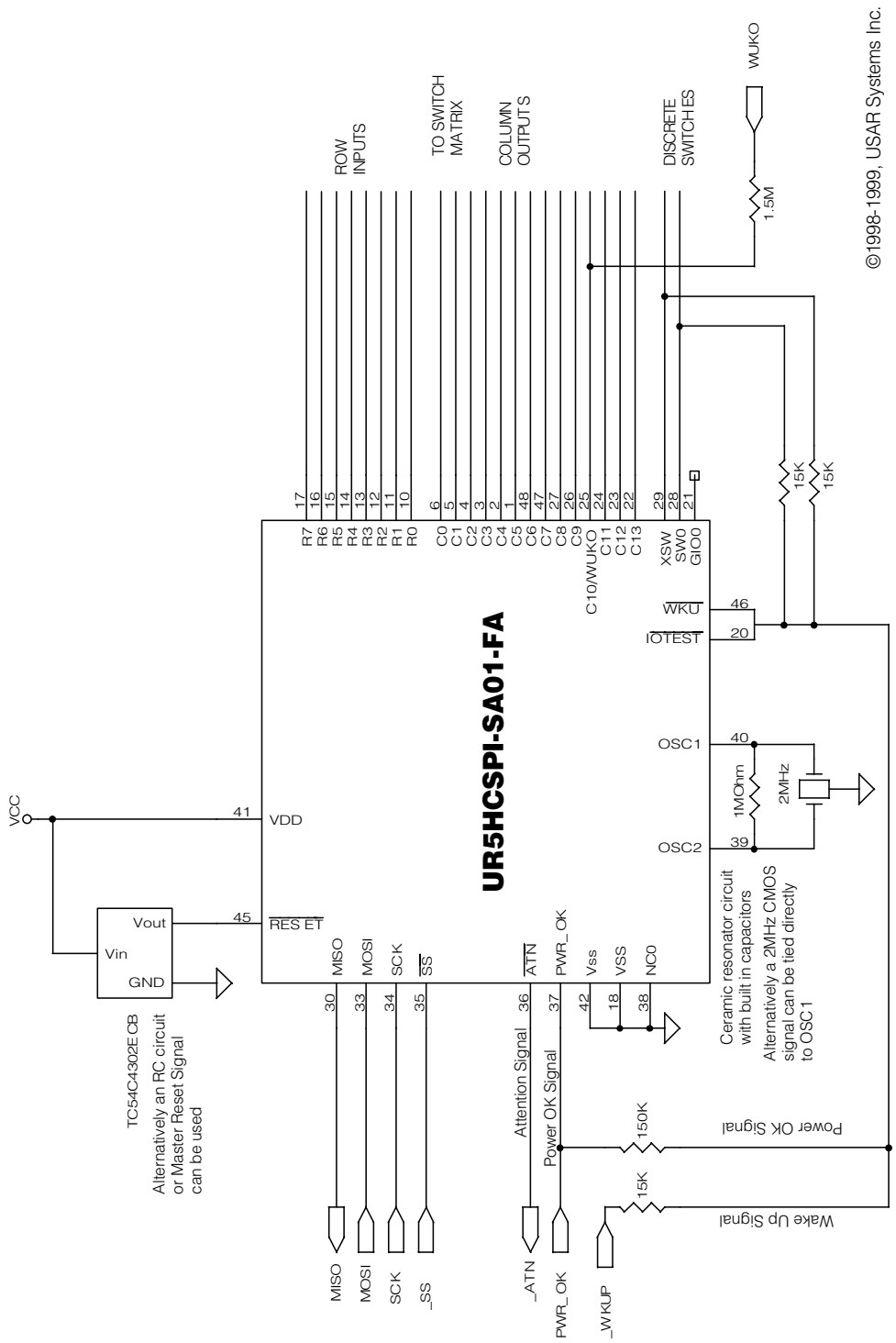
When UR5HCSPI-SA01 receives this command, it will change the I/O pin's mode accordingly. If the <IO MODE> =4, the UR5HCSPI-SA01 will send the I/O Mode Status Report to the host.

Output Data to I/O Pin

<ESC>	1BH	
<MODIO>	A8H	
<IO NUMBER>	xxH	IO number: 0
<IO DATA>	xxH	IO data: (0=low, 1=high, 2=current I/O data request)
<LRC>	xxH	

When UR5HCSPI-SA01 receives this command, it will change the value of the output pin accordingly. If the addressed pin is not configured as an output pin, the command will be ignored. If <IO DATA> =2, the UR5HCSPI-SA01 will respond by issuing the I/O Data Status Report to the host.

Sample Configuration-UR5HCSPI-SA01



Electrical Specifications

Absolute Maximum Ratings

Ratings	Symbol		Value	Unit
Supply Voltage	Vdd		-0.3 to +7.0	V
Input Voltage	Vin		Vss -0.3 to Vdd +0.3	V
Current Drain per Pin (not including Vss or Vdd)	I		25	mA
Operating Temperature UR5HCSPI-SA01	Ta		T low to T high -40 to +85	° C
Storage Temperature Range	Tstg -		65 to +150	° C

Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance	Tja		°C per W
■ Plastic		60	
■ PLCC		70	

DC Electrical Characteristics (Vdd=3.3 Vdc +/-10%, Vss=0 Vdc, Temperature range=T low to T high unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage (I load<10µA)	Vol			0.1	V
	Voh	Vdd–0.1			
Output High Voltage (I load=0.8mA)	Voh	Vdd–0.8			V
Output Low Voltage (I load=1.6mA)	Vol:			0.4	V
Input High Voltage	Vih	0.7xVdd		Vdd	V
Input Low Voltage	Vil	Vss		0.2xVdd	V
User Mode Current	Ipp		5	10	mA
Data Retention Mode (0 to 70°C)	Vrm	2.0			V
Supply Current (Run)	Idd		1.53	3.0	mA
(Wait)			0.711	1.0	mA
(Stop)			2.0	20	µA
I/O Ports Hi-Z Leakage Current	Iil			+/-10	µA
Input Current	Iin			+/- 1	µA
I/O Port Capacitance	Cio		8	12	pF

Control Timing (Vdd=3.3 Vdc +/-10%, Vss=0 Vdc, Temperature range=T low to T high unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
Frequency of Operation	fosc			MHz
■ Crystal Option			2.0	
■ External Clock Option		dc	2.0	
Cycle Time	tcyc	1000		ns
Crystal Oscillator Startup Time	toxov		100	ms
Stop Recovery Startup Time	tilch		100	ms
RESET Pulse Width	trl	8		tcyc
Interrupt Pulse Width Low	tlih	250		ns
Interrupt Pulse Period	tilil	*		tcyc
OSC1 Pulse Width	toh, tol	200		ns

*The minimum period tlil should not be less than the number of cycle times it takes to execute the interrupt service routine plus 21 tcyc.

Bill of Materials for UR5HCSPI-SA01-FA

Quantity	Manufacture	Part#	Description
3	Generic	15K	15K Resistor
1	Generic	150K	150K Resistor
1	Generic	11M	1M Resistor
2	Generic	1.5K	1.5 Resistors
1	TELCOM	TC54VC4302ECB713	IC Volt Detector CMOS 4.3V SOT23, for 5V Operation
		TC54VC4302ECB713	IC Volt Detector CMOS 2.7V SOT23, for 3.3V Operation
1	AVX	PBRC-2.00BR	2.00MHZ Ceramic Resonator with Built in Capacitors, SMT

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