TOPRO

TP6508

Advanced Panel-2 Video Graphic Array

Specification

Version: 2.02
Revision: 2.01a
1999/04/12

Topro Technology Incorporation

Revision History

Revision	Date .	Comment .
2.02	88.04.12	Change for Topro version .

TP6508 Target Spec. List

I. General Description

The TP6508 is an advanced single-chip flat panel VGA controller . It's used for notebook or portable computer system with simple operation and powerful features. Also it contains all of the functions and supports logic required to implement the IBM VGA display standards and enhanced display modes on LCD, PLASMA,EL panel and TV display at register and BIOS level compatiable. A simultaneous display technology is implemented in TP6508 to be used for CRT/Flat panel, LCD/ TV display.

For minimum chip-count or board-space, it is designed to complete a video subsystem with only one 256kx16 DRAM(512K Bytes). This video subsystem can support all panel type without any glue logic or external frame buffer.

Like general VGA graphics chips, the TP6508 includes CRT Controller (CRTC), Attribute Controller (ATRC), Graphic Controller (GFXC), Address Multiplexer (AMUX) , Sequential Controller (SEQC) and adds a Graphics Engine Controller (GEC) to provide VGA display functions and to speed up the system operation. With the deeper CRT FIFO , and the multiple level CPU command FIFO (Write Buffer) / Read Cache , the TP6508 supports higher system performance even in minimum memory configurations.

In order to complete a video subsystem by two chips, VGA controller and DRAM, the TP6508 uses 208pin QFP to integrate Clock Generator(Dual frequency synthesizers), True-color RAMDAC, Display controller, Flat panel controller, Video-in interface, Graphics Engine Controller and Power management controller to minimizes the form factor requirement for VGA subsystem.

In addition to an ISA bus connection, it can be connected directly to PCI standard local bus interface to provide additional graphics performance without any glue logic.

TP6508 can support flat panel display, resolution up to 1024x768 mono, 800x600 hi-color, 640x480 true-color. Unlike on CRT, the pixels on a flat panel display are real,discrete entities of a fixed size. This results in problems when different display modes are mapped onto one panel. The TP6508 provides approach to keep the vertical resolution of the display mode constant but center the active display area vertically on the panel.

The flat panel interface supports Monochrome/Color STN LCD panel, Color TFT LCD panel, PLASMA panel and, EL panel. Providing direct panel interface to (DD) Dual-panel,Dual-drive for color and monochrome and (SS) Single-panel,Single-drive (supports 8,9,12,15,16,18,24-bit data). For Single-panel/Single-drive panel which refresh data rate is not high, the TP6508 can set some of the video memory as the frame buffer for panel display to decrease video memory chip counts to one (a 256kx16DRAM).

When the TP6508 is interfaced to a dual-scan mono STN LCD panel , an additional DRAM isn't needed with the shadow frame buffer technology . This shadow frame buffer build in video memory that is used by the chipset to accelerate panel refresh rate without using high frequency clocks , thus reducing power, and allowing vertical refresh rates from 60 Hz to 160 Hz for improved contrast and freedom from flicker.

The TP6508 serves as a DRAM controller for the display memory,it handle DRAM refresh, display refresh, display memory access by CPU and supply the control signal of DRAM with dual-write or dual-cas.

The TP6508 offers two types DRAM to make various memory configurations including of 512k , 1024k , 2048k memory size for different market. TP6508 support 256k x 4-bit , or 256k x 16-bit DRAM memory to simplify VGA system and implement high resolution display simultaneously. With Random Memory Cycle allocation skill and the multiple level CPU write buffer, the TP6508 provide better system performance and achieve zero wait state during memory write accesses.

When using DRAM 256kx16 by 1 or DRAM 256kx4 by 4, memory size is 512k byte and data width is 16 bits. When using 256kx16 by 2 or 256kx4 by 8, memory size is 1M byte and data size is 32 bits. TP6508 can support the CRT display resolution up to 1024x768 256 color non-interlace, 800x600 hi-color,640x480 true color at 1M byte display memory. When using 256kx16 by 4 , memory size is 2M byte and data size is 32 bits. All display-memory can be linear addressing.

The Video-in interface accept video signal from PC-video.

Providing the power sequential control for flat panel . FPVCC signal is applied to the digital +5V voltage of flat panel, FPVEE signal is applied to the analog Driver's bias voltage of flat panel, and FPBACK signal is applied to the Invertor for the backlight of flat panel, their on/off sequence is programmable. Anotherway TP6508 providing intelligent control by timer to switch power mode (On including Cover-close,standby,suspend,Off) to save the power of TP6508 and Display.

The TP6508 graphics chip has been designed to optimize cost/performance trade-off considerations. The Video clock rate depends upon the mode used, and is up to 135 MHz. The Memory clock input is optional and depends on the display DRAMs access-time . It can be up to 75 MHz.

II. Feature

. 208-pin single chip design
. IBM VGA hardware compatible
. Integrates RAMDAC
- Support 24-bit True-color resolution
- Up to 135 MHz pixel rate
- Low power control
- Implement Monitor-Sense feature

. Integrates Clock Generator
- Programmable dual frequency synthesizer
- Up to 135 MHz clock rate for VCLK synthesier
- Up to 75 MHz clock rate for MCLK synthesier
- External Power-down mode Clock Source optional

. Memory DRAM configuration support
- Support symmetric or asymmetric RAS/CAS address DRAM
- Support dual-CAS or dual-WE addressing DRAM
- 512k Bytes Memory:four 256kx4-bit /one 256kx16-bit
- 1M Bytes Memory:eigh 256kx4-bit /two 256kx16-bit
- 2M Bytes Memory:sixteen 256kx4-bit/four 256kx16-bit

. Bus support
- ISA Bus with Zero-wait state assertion
- 32-bit data width PCI Local Bus

. Provide linear addressing
- Relocation VGA memory address at over 1M-byte address location

. Integrates STN panel support
- Support Dual/single scan mono STN LCD Panel,
  up to 64 simultaneous grays
- Support Dual/single scan color STN LCD Panel
  up to 64k simultaneous colors, and 61^3 visual color
- Provide 8 and 16 bit panel interfaces

. Integrates color TFT panel support
- Support Normal or CRT-like TFT LCD panel
- Support 9/12/15 or 18/24 bit panel interface, and up to 16.8M simultaneous colors

. Support panel resolution up to 800x600 for STN and TFT LCD flat panel
. Simultaneous Display operation
- Simultaneous LCD and CRT display
- Simultaneous PLASMA and CRT display
- Simultaneous EL and CRT display
- Simultaneous LCD and TV display

. VGA BIOS decoding
- Provide 64k-byte or 32k-byte VGA BIOS decoding

. Dual-scan STN Frame Buffer

- Shadow Frame Buffer onto display memory for mono or color LCD panel
- Pseudo Frame Buffer for color LCD panel (no additional DRAMs required)
- External Frame Buffer for color LCD panel (external additional DRAMs required)

. Provide PC Video interface

- Provide VESA Advanced Feature Connector(VAFC) interface
- Provide color-key PC video interface

. High Performance architecture

- Provide 4 stages CPU Write Buffer
- Provide 8 stages Command FIFO for graphics engine access
- Offer 20 stages CRT FIFO and 8 stages Attribute FIFO

. Integrates hardware cursor function

- 64 by 64 pixels (2-bit)
- Offer Color 0,1,inversion and transparency operation

. Windows performance-improvement feature

- Bit block transfer (8/16/24 bit color mode) including of Image read/write
- Color expansion (8/16/24 bit mode)
- Line drawing (8/16/24 bit mode)
- Rectangular clipping (8/16/24 bit mode)
- Rectangular fill and Pattern fill(8/16/24 bit mode)

. Graphics Engine I/O command addressing

- Programmable I/O base command
- Memory mapping I/O command

. Intelligent Power Management

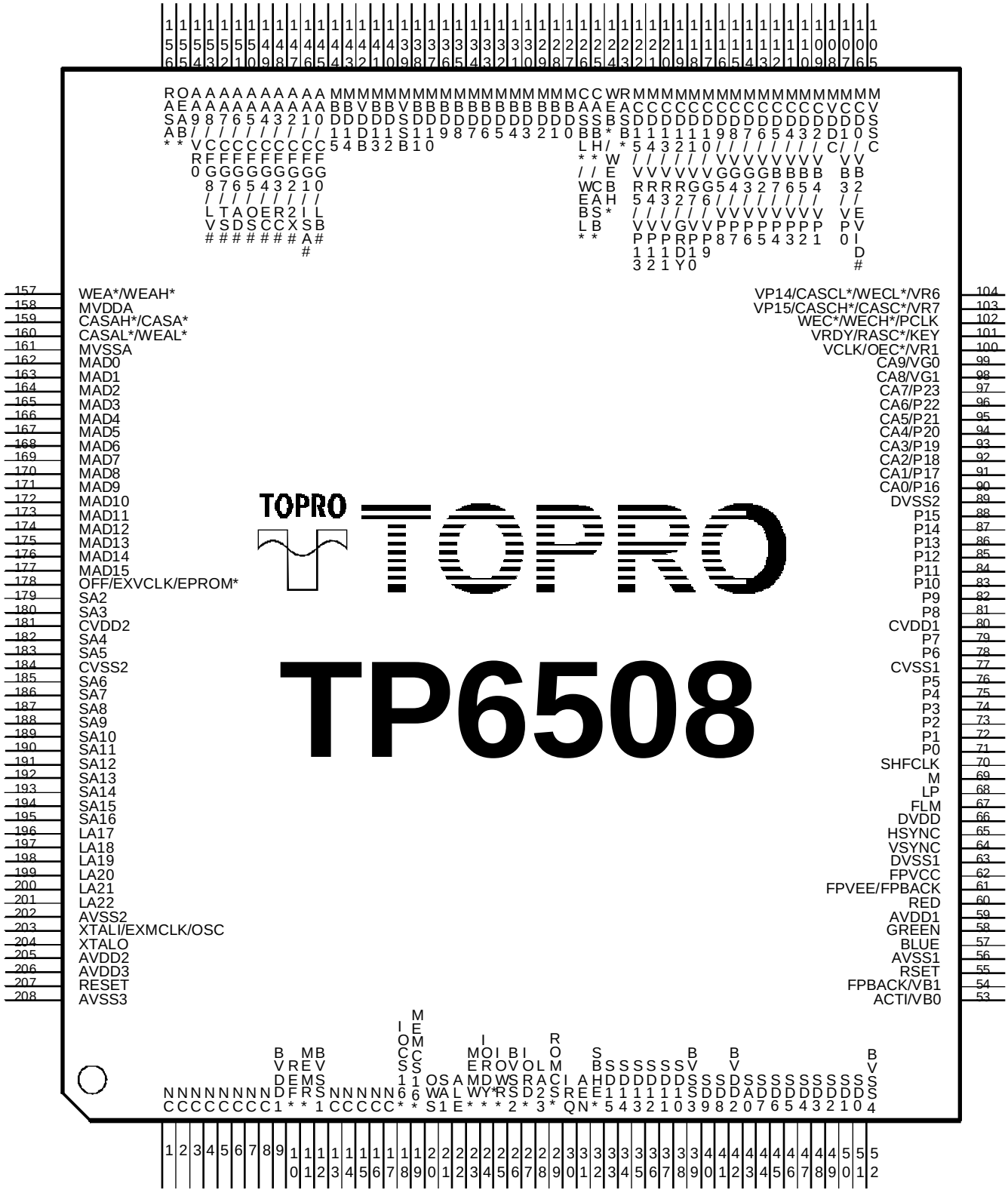
- Built-In Power Management controller
- Multiple level power down modes (On/Standby/Suspend/Off mode)
- Automatic activity monitoring
- Flexible mode transition Control (Pin control/Timer out/Register programming /VGA access and Keyboard request trigger return)
- Automatic flat panel power sequencing
- Programmable slow refresh rate

. Enhanced mode includes:

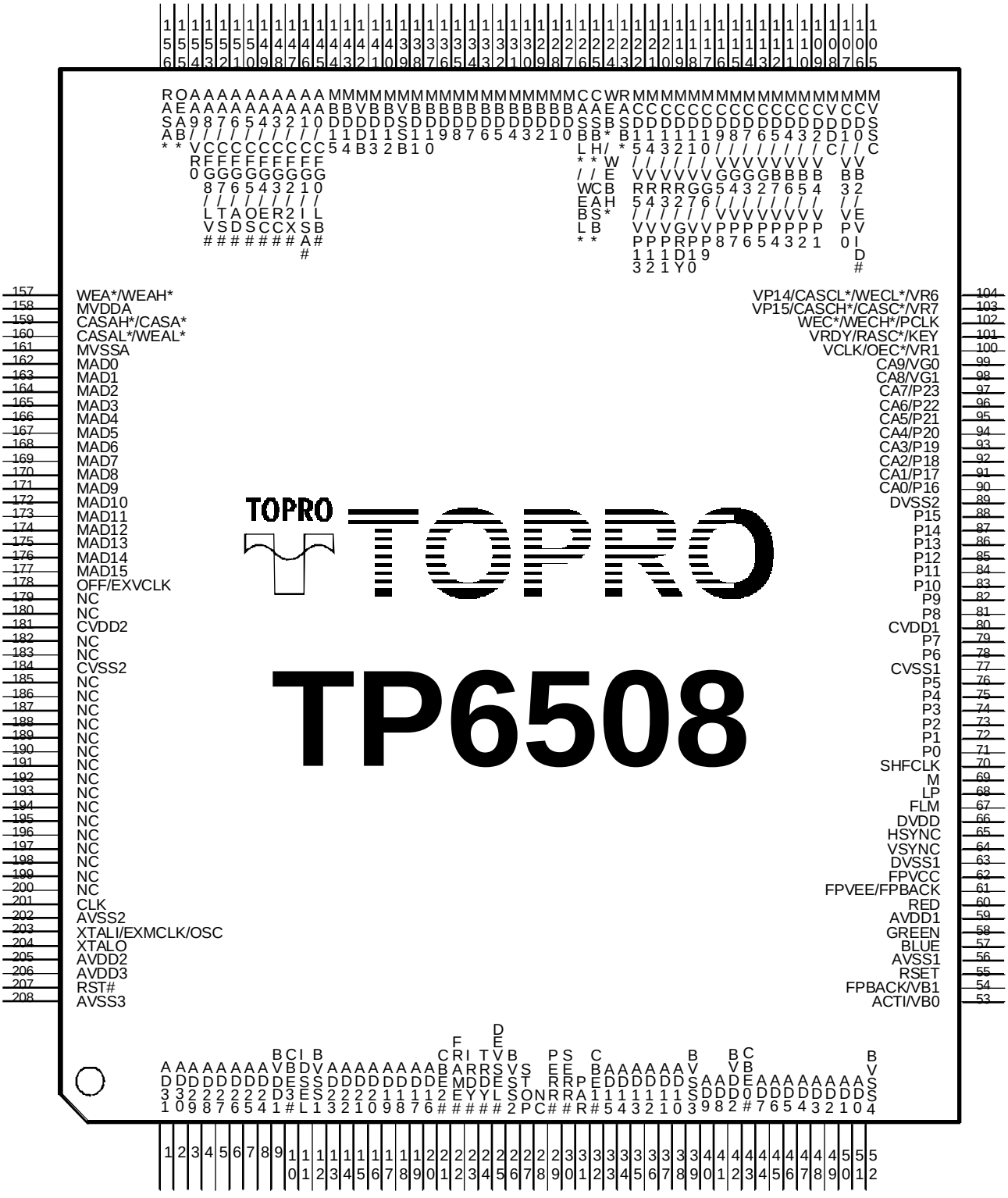
- 132x25 or 132x44 text mode
- 640x480/256 colors (Windows acceleration mode support optional)
- 640x480/65536 colors (Windows acceleration mode support optional)
- 640x480/16.8M colors (Windows acceleration mode support optional)
- 800x600/16 colors
- 800x600/256 colors (Windows acceleration mode support optional)
- 800x600/65536 colors (Windows acceleration mode support optional)
- 800x600/16.8M colors
- 1024x768/16 colors
- 1024x768/256 colors (Windows acceleration mode support optional)
- 1024x768/65536 colors (Windows acceleration mode support optional)
- 1280x1024/16 colors
- 1280x1024/256 colors (Windows acceleration mode support optional)
- 1600x1280/16 colors interlace display mode

III. Pin Configurations

ISA Bus Interface Connections

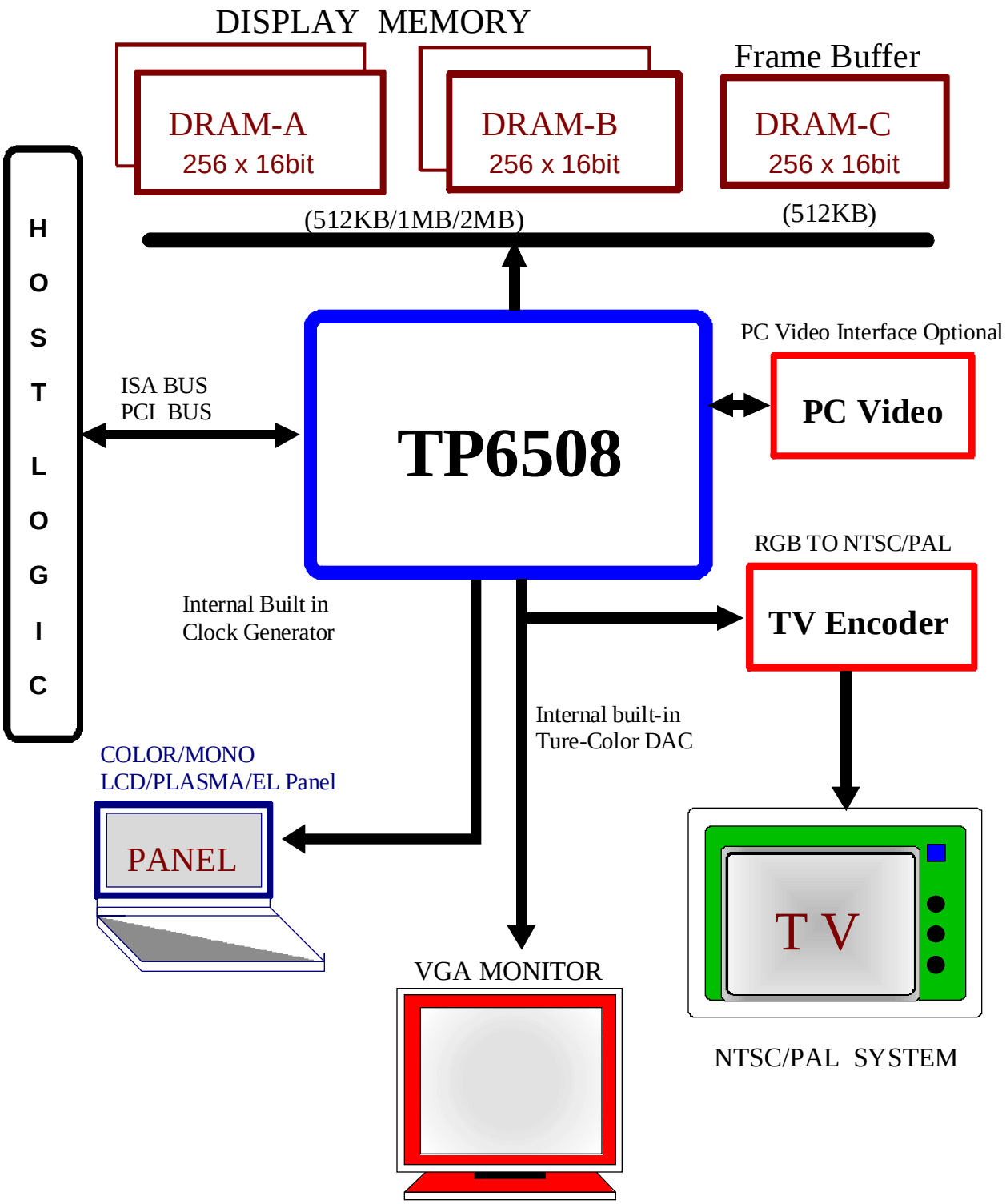


PCI Local Bus Interface Connections



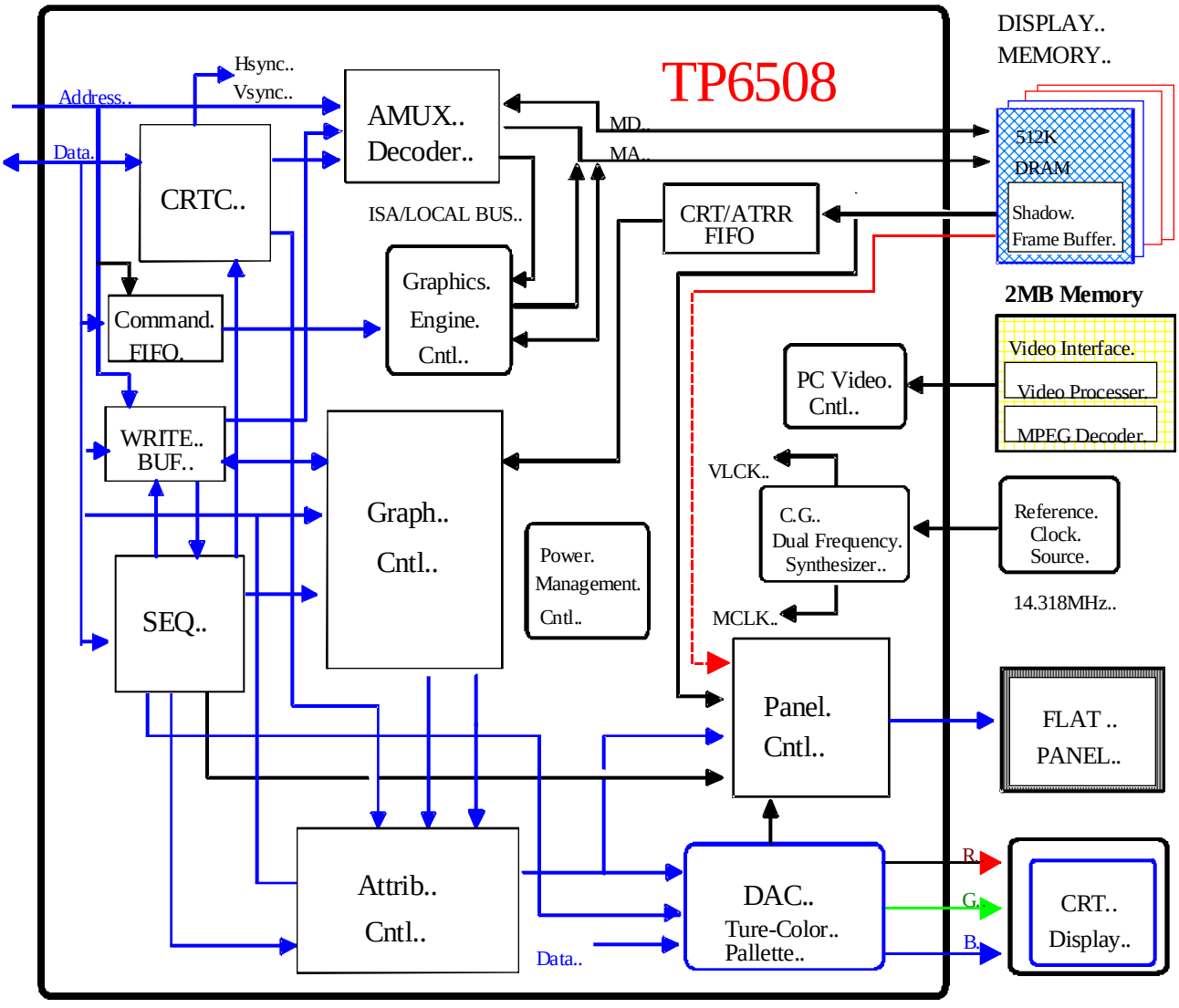
IV. Functional Block Diagram

System Block Diagram



1280 X 1024 / 256 , 800 X600 / 16.8M COLORS FLAT PANEL/CRT DISPLAY SYSTEM

VGA Block Diagram



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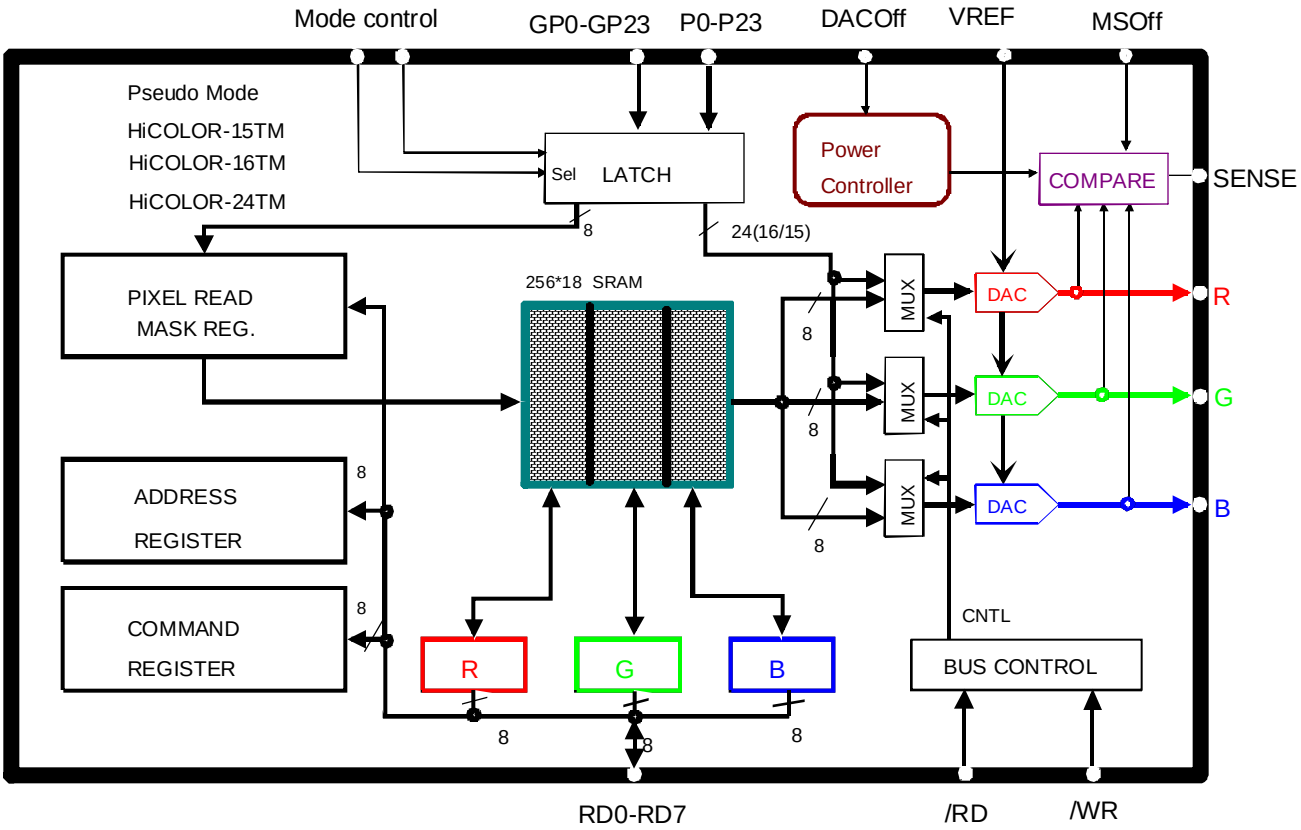
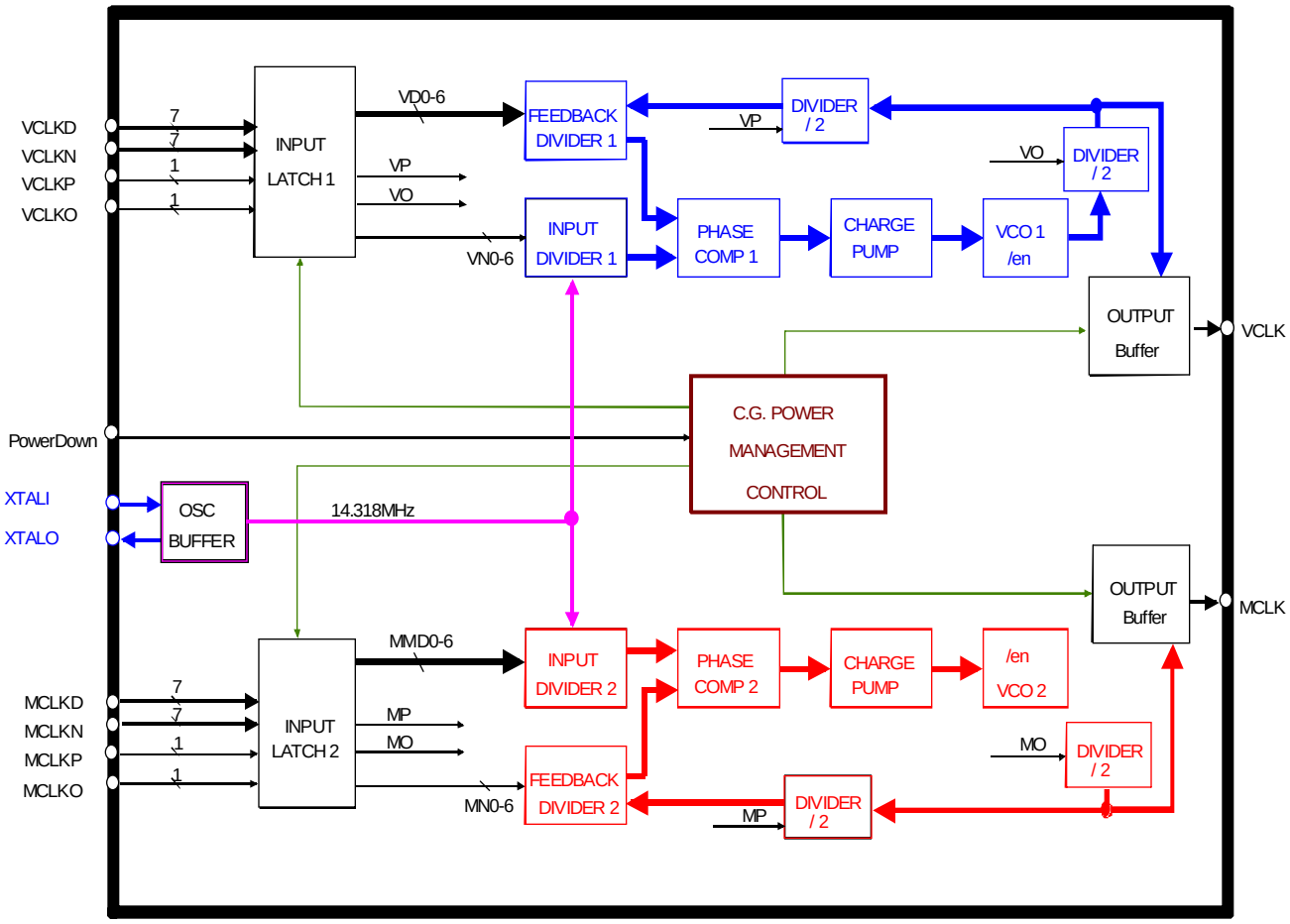
True-Color Palette DAC Block Diagram



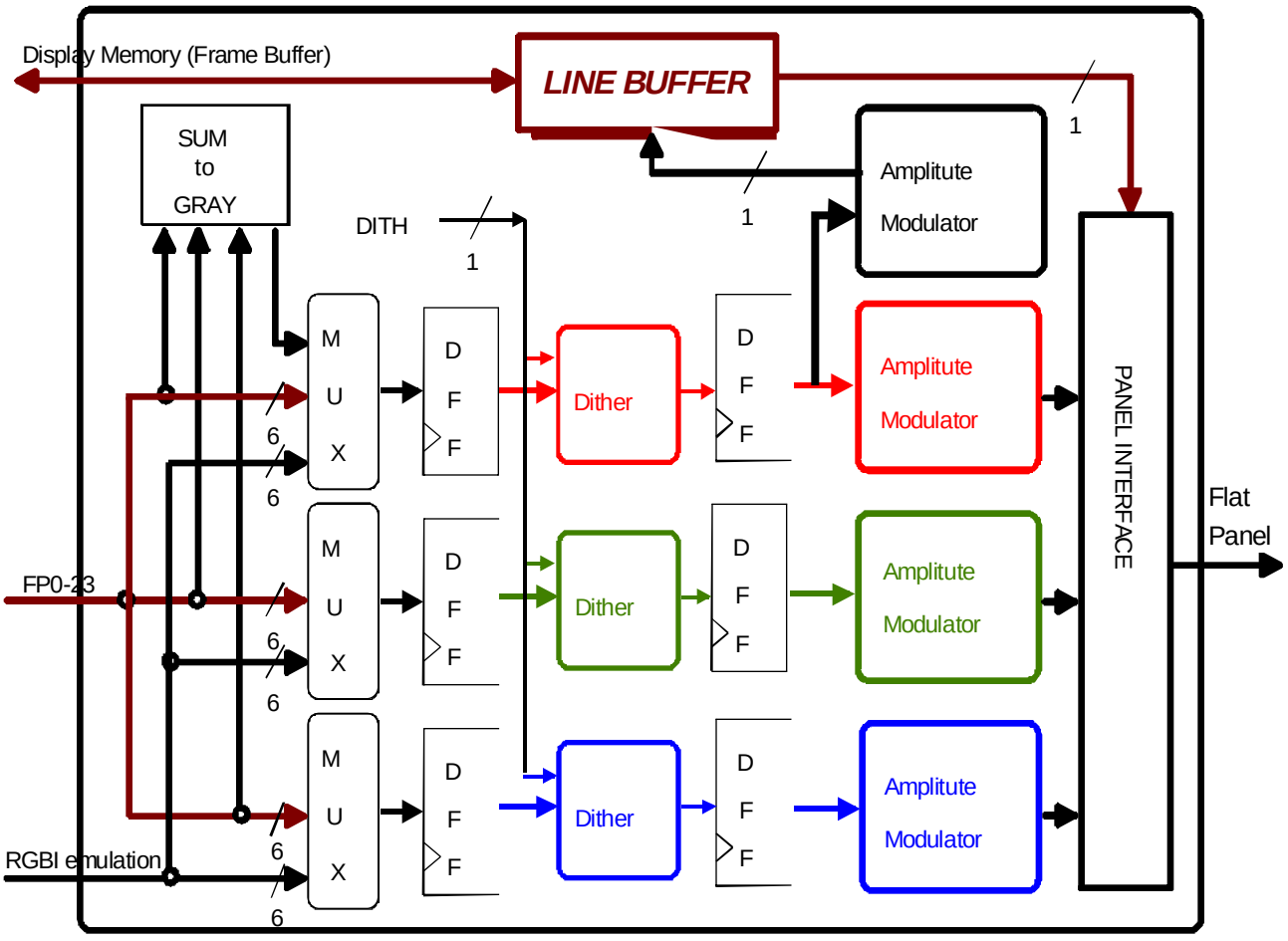
[SP508B02.DS4 85/03/11 L.R.Y.]

Dual Frequency Synthesizer Block Diagram



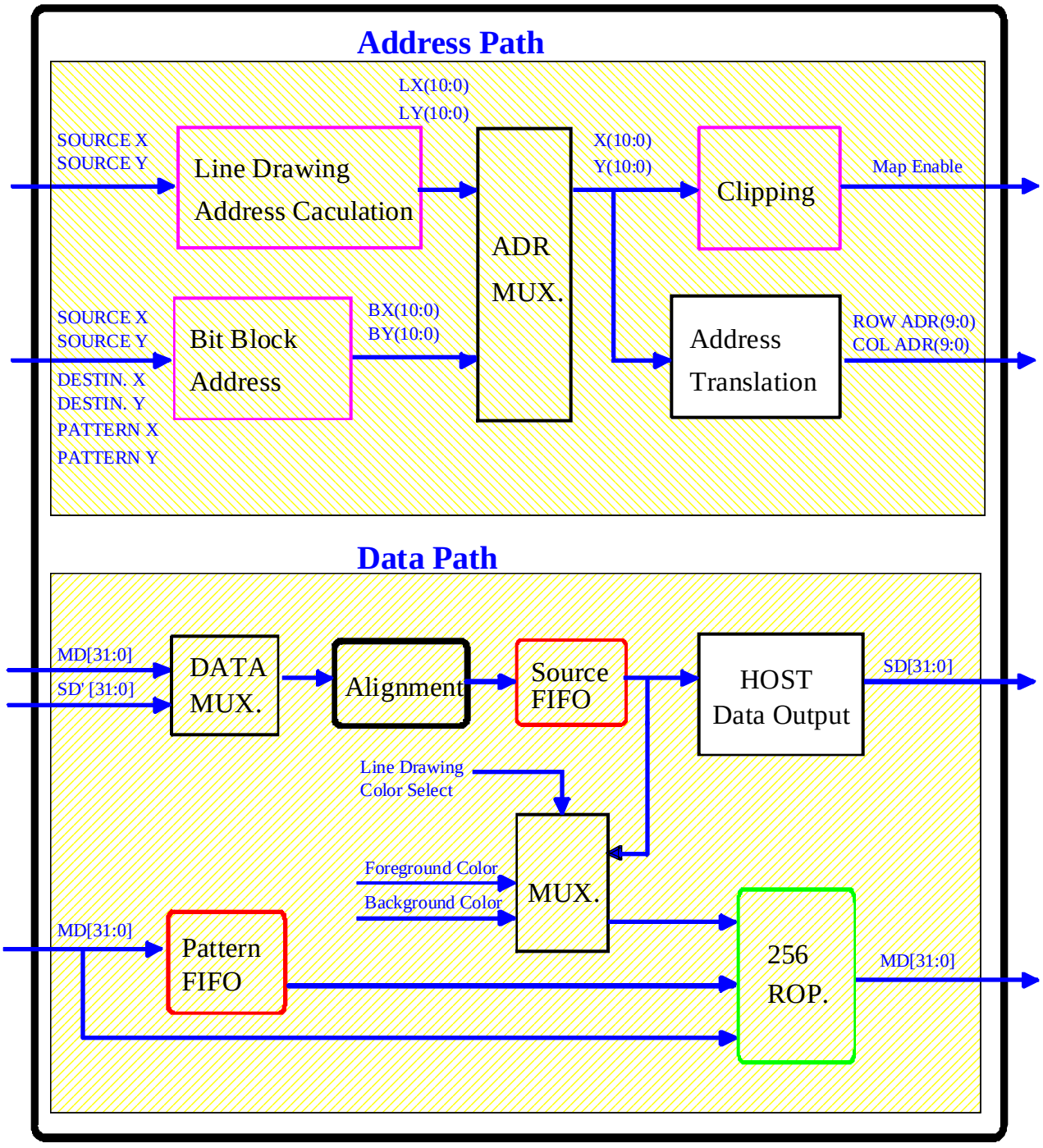
[SP508B03.DS4 85/03/11 L.R.Y.]

Panel Controller Block Diagram



[SP508B04.DS4 85/03/11 L.R.Y.]

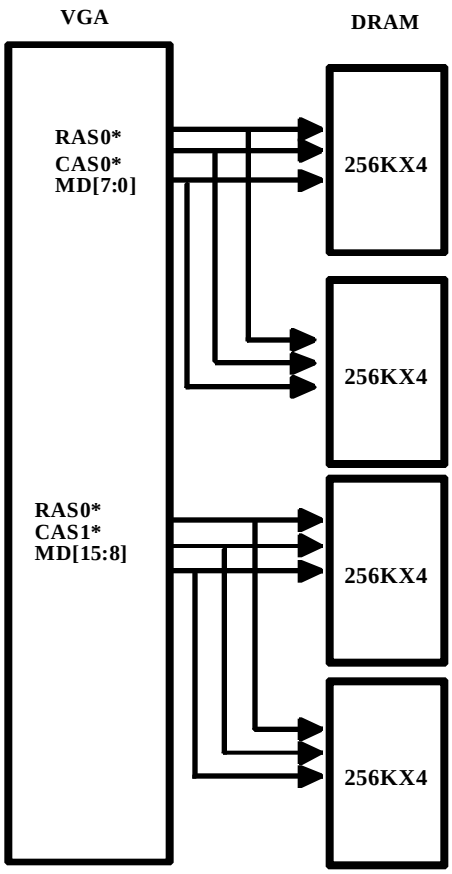
Graphics Engine Diagram



[SP508B12.DS4 85.08.21]

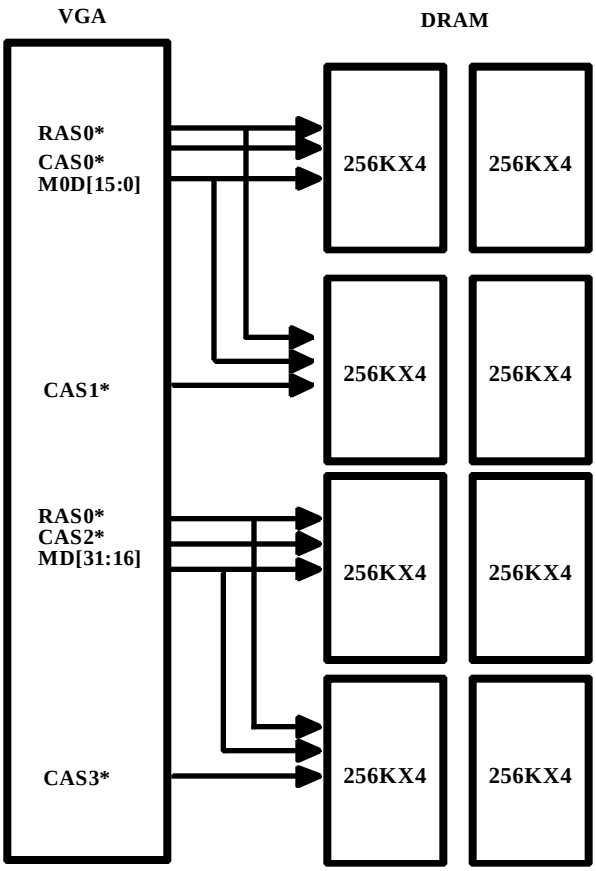
Memory Configuration Block Diagram

512 K MEMORY DRAM(S) CONFIGURATION

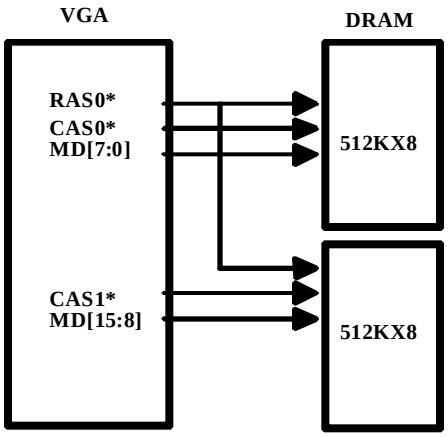


1024K MEMORY DRAM(S) CONFIGURATION

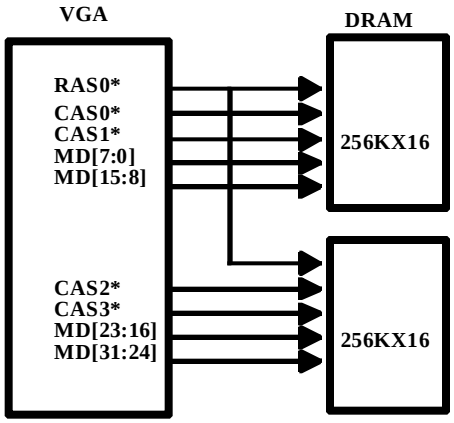
A.



B.



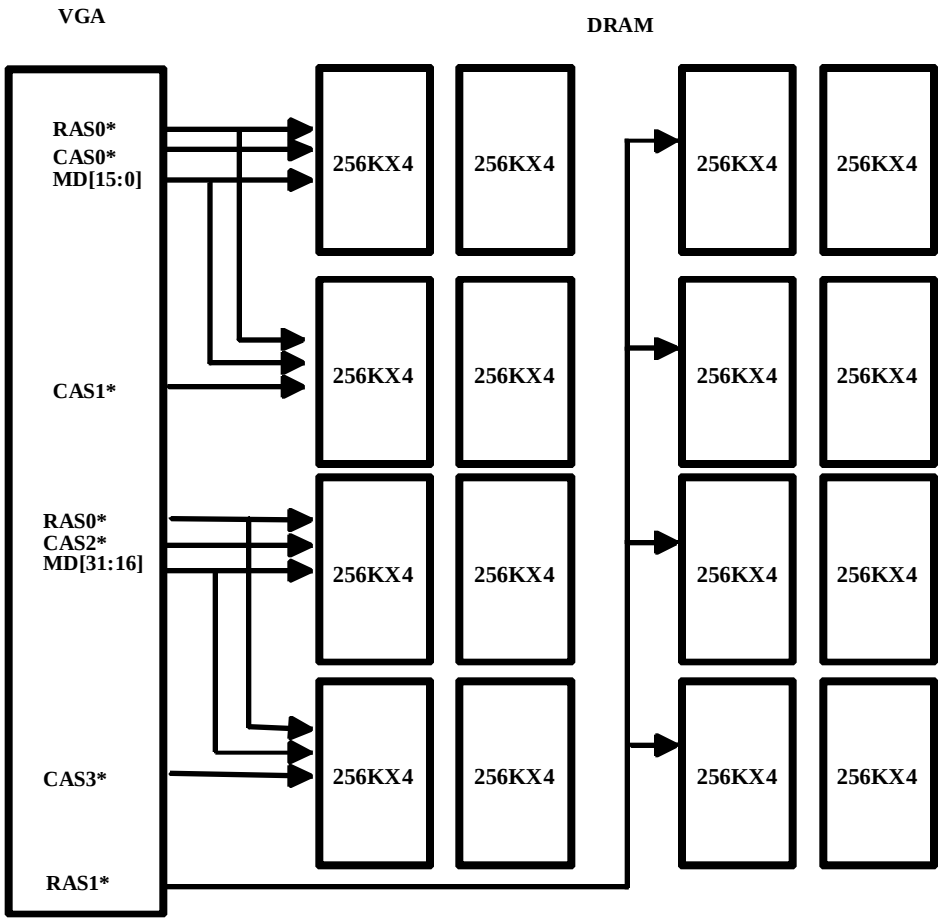
C.



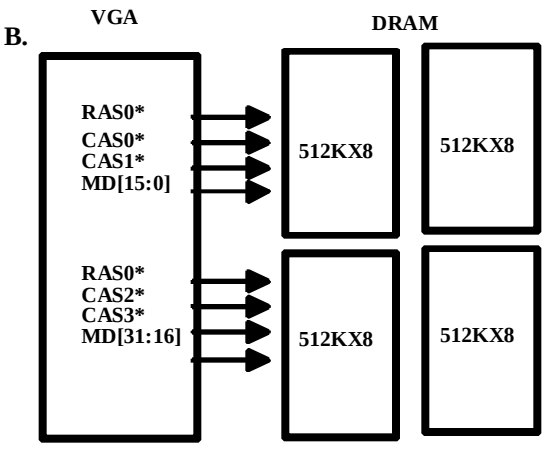
[SP508B06.DS4 84/05/23]

2048K MEMORY DRAM(S) CONFIGURATION

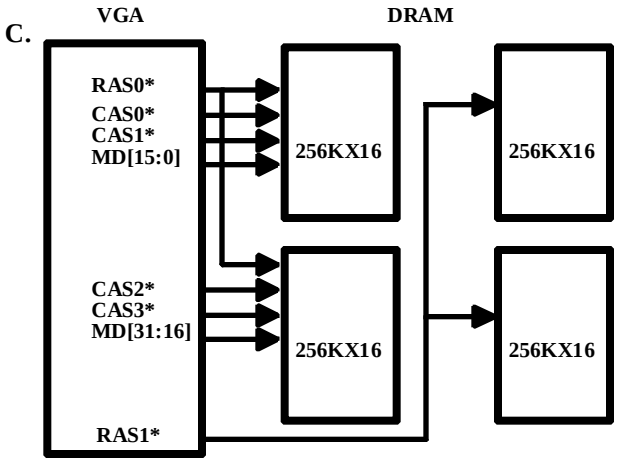
A.



B.



C.



[SP508B06.DS4 84/05/23]

V. Pin Descriptions

* ISA Bus Interface (54 pins)

Symble	Type	Drive	Pin Number	Active	Function
SD[15:0]	I/O	8maR	33,34,35,36,37 38,40,41,44,45 46,47,48,49,50,51	True	These signals provide 16 data bits transfer on ISA bus with system microprocessor.
SA[16:2] SA[1:0]	I (I/O) I	-	195,194,193,192,191, 190,189,188,187,186, 185,183,182,180,179, 21,43	True	Address Bit 16 Through 0 are used to address frame buffer and I/O ports with TP6508.
LA[23:22] A21 A20 LA[19:17]	I I (I/O) I I (I/O)	-	28,201,200,199,198, 197,196	True	Address Bit 23 Through 17 are used to address frame buffer and I/O ports with TP6508. In general ,these signals are not gated address LA[19:17]
AEN	I (I/O)	-	31	High	A high active signal used to detect the TP6508 from the I/O channel to avoid a disturbance from the DMA controller.
ALE	I	-	22	High	This signal is used to latch those ungated address bus.
SBHE*	I	-	32	Low	It indicates and enables transfer of data on the high byte of data bus and is used with A0 to distinguish between high and low byte.
IORD*	I (I/O)	-	27	Low	I/O read signal comes from a host microprocessor to read data from TP6508 control.
IOWR*	I (I/O)	-	25	Low	I/O write signal comes from a host microprocessor to read data from TP6508 control registers.
MEMR*	I	-	11	Low	Memory read signal comes from a host microprocessor to read data from video memory.
MEMW*	I	-	23	Low	Memory write signal comes from a host microprocessor to read data from video memory.
IORDY*	OT	12maR	24	Low	This signal is driven low by TP6508 to lengthen the memory or I/O accessed cycle.
IOCS16*	OT (I/O)	12maR	18	Low	This signal is driven low to indicate that the TP6508 can execute an I/O operation at the address currently on the 16-bit bus mode.
MEMCS16*	OT (I/O)	12maR	19	Low	This signal drives a 16-bit memory cycle for 16-bit bus data transfer.
RESET*	I/S	-	207	Low	This pin is connected to the signal that was inverted from the system board to reset the TP6508.
IRQ	OT (I/O)	8maR	30	Low	The vertical retrace interrupt.
REF*	I	-	10	Low	This signal is driven by system mother board logic and is used to indicate a memory refresh cycle is in operation.
OWS*	OT (I/O)	8maR	20	Low	This signal is driven by TP6508 to short the memory accessed cycle for improving system performance.

* PCI Local Bus Interface (48 pins)

Symble	Type	Drive	Pin Number	Active	Function
AD[31:0]	I/O	8maR	1,2,3,4,5, 6,7,8,13,14, 15,16,17,18,19,20, 33,34,35,36,37 38,40,41,44,45 46,47,48,49,50,51	True	Address and Data are multiplexed on the same PCI Bus interface. A Bus transaction consists of an address phase followed by one or more data phase.
C/BE[3:0]#	I	-	10,21,32,43	True	Bus Command and Byte Enable are multiplexed on the same PCI Bus interface. During the address phase of a transaction, they define the Bus Command. During the data phase , they are used as Byte Enable.
PAR	OT (I/O)	4maR	31	True	Parity is even part across AD[31:0] and C/BE[3:0]#. Parity generation is required by all PCI agents.
FRAME#	I	-	22	Low	This input signal is used to indicate the beginning and duration of an access.
TRDY#	OT	12maR	24	Low	This signal is driven to indicate TP6508's ability to complete the current data phase. It is used in conjunction with IRDY#.
IRDY#	I	-	23	Low	This input signal is to indicate Bus master's ability to complete the current data phase. It is used in conjunction with TRDY#.
IDSEL	I	-	11	High	This signal is used as a chip select during configuration read and write access.
RESET#	I/S	-	207	Low	This signal is used to reset the TP6508 video device into initial state.
CLK	I	-	201	True	This is the timing reference for TP6508 when connected to PCI Local Bus.
DEVSEL#	OT (I/O)	12maR	25	Low	This signal is driven to indicate that TP6508 video device has been selected . So TP6508 has decoded its address as the target of the current access.
STOP#	OT (I/O)	4maR	27	Low	This signal is output to indicate that TP6508 is requesting the master to stop the current transaction.
PERR#	O/T (I/O)	8maR	29	Low	This signal is used for the reporting of data parity erros. PERR# will be driven high for one clock before being tristated as with all sustained tristate signals.
SERR#	O/T (I/O)	8maR	30	Low	This signal is used for the reporting of system erros.

* Display Memory Interface (82 pins)

Symble	Type	Drive	Pin Number	Active	Function
AA9 AA[8:0]	I/O I/O/U	4maR 4maR	154,153,152,151,150, 149,148,147,146,145	True	Display memory address bit 9 to 0 for DRAMs A and B. A pull-high mechanism gives a default high value in those configuration data.
CA[9:8] CA[7:0]	I/O O	4maR 4maR	99,98,97,96,95, 94,93,92,91,90	True	Display memory address bit 9 to 0 for DRAMs C.
MAD[15:0]	I/O/U	4maR	177,176,175,174,173, 172,171,170,169,168, 167,166,165,164,163 162	True	These pins are used to transfer data between the TP6508 and display memory, DRAM A. A pull-high mechanism gives a default high value in those configuration data.
MBD[15:0]	I/O	4maR	144,143,141,140,138, 137,136,135,134,133, 132,131,130,129,128, 127	True	These pins are used to transfer data between the TP6508 and display memory, DRAM B.
MCD[15:0]	I/O	4maR	122,121,120,119,118, 117,116,115,114,113, 112,111,110,109,107, 106	True	These pins are used to transfer data between the TP6508 and frame buffer memory, DRAM C. When a frame buffer DRAM isn't requireed, this bus may optionall be used to input up to 24 bits of RGB data from the external PC-Video subsystem(device).
RASA*	O	4maR	156	Low	Row address strobe for latching 10-bit row address signal into display memory, DRAM A..
RASB*	O	4maR	123	Low	Row address strobe for latching 10-bit row address signal into display memory, DRAM B..
RASC*	I/O	4maR	101	Low	Row address strobe for latching 10-bit row address signal into display memory, DRAM C..
CASAL*/WEAL*	O	4maR	160	Low	Column address strobe for DRAM A lower byte in dual-CAS application. In dual-WE application, it is used as write enable signal for DRAM A lower byte.
CASAH*/CASA*	O	4maR	159	Low	Column address strobe for DRAM A upper bytein dual-CAS application.
CASBL*/WEBL*	O	4maR	126	Low	Column address strobe for DRAM B lower bytein dual-CAS application.
CASBH*/CASB*	O	4maR	125	Low	Column address strobe for DRAM B upper byte.in dual-CAS application.
CASCL*/WEAL*I/O	4maR		104	Low	Column address strobe for DRAM C lower bytein dual-CAS application.
CASCH*/CASC*	I/O	4maR	103	Low	Column address strobe for DRAM C upper bytein dual-CAS application.
WEA*/WEAH*	O	4maR	157	Low	Write enable signal for DRAM A in dual-CAS application. In dual-WE application, it is used as write enable signal for DRAM A upper byte.
WEB*/WEBH*	O	4maR	124	Low	Write enable signal for DRAM Bin dual-CAS application.
WEC*/WECH*	O	4maR	102	Low	Write enable signal for DRAM Cin dual-CAS application.
OEAB*	O	8maR	155	Low	Data output enable signal for DRAM A and DRAM B.
OEC*	I/O	4maR	100	Low	Data output enable signal for DRAM C.

* CRT Output interface (6 pins)

Symble	Type	Drive	Pin Number	Active	Function
RED	Analog Output	20ma	60	-	These three analog outputs are generated by TP6508's internal build-in DAC and it supplies current corresponding to the red , green , blue value of pixel being displayed.
GREEN	Analog Output	20ma	58		
BLUE	Analog Output	20ma	57		
RSET	Analog Output	10ma	55	-	This pin input is used as the internal build-in RAMDAC voltage reference. A setting resister is required between this pin and AVSS1 determines the full-scale output of each DAC.
VSYNC	O	12maR	64	True	Vertical retrace synchronization signal drives the CRT monitor.
HSYNC	O	12maR	65	True	Horizontal retrace synchronization signal drives the CRT monitor.

* Clock Input Interface (4 pins)

XTALI	I	-	203	True	The pin serves as the crystal input.
EXMCLK	I	-		True	External memory clock input.
OSC	I	-		True	It requires an input frequency of 14.318MHz with a duty cycle of 50+/-5%.This input pin supplies the reference frequency for the Dual-frequency Synthesizer .
XTALO	O	-	204	True	The pin serves as the crystal output .
EXVCLK	I (I/O)	-	178	True	External video clock input It is a optional input from STANBY pin.
32KHZ	I (I/O)	-	154	True	Refresh clock input for DRAMs under into OFF mode (VESA DPMS).

* MISC. Pins (2 pins)

ROMCS*	O (I/O)	8maR	29	Low	VGA BIOS ROM enable signal for ISA bus, it generated by HM86509 when the 32k-byte memory location from C0000 to C7fff or the 64k-byte memory domain setting by extended registers is selected.
TEST	I/O	4maR	178	True	This pin is intended for testing. It can be redefined as other useful function pin at the combination switch type of description in extended register Hex CC .

* Flat Panel Interface (28 pins)

Symble	Type	Drive	Pin Number	Active	Function
SHFCLK(CL2)	O	12maR	70	True	This signal is used to driver the flat panel shift clock .
LP(CL1) PHSYNC DE	OT	8maR	68	High True High	This signal is used to drive the flat panel line clock for LCD panels or the horizontal sync for PLASMA/EL panels and some TFT panels. It can also do as the display enable signal (DE) for flat panel.
FLM PVSYNC	OT	8maR	67	High True	This signal is used to start a new frame on flat panels for LCD panels or the vertical sync for PLASMA/EL panels and some TFT panels.
M DE	O	8maR	69	True High	This signal is used to provide the AC inversion for flat panels to prevent a chemical damage. It can also do as the display enable signal (DE) for flat panel.
P[23:16]	O	4maR	97,96,95,94,93,	True	These signals contain RED/GREEN/BLUE color data for 9/12/18/24 bit interface TFT-color LCD panels.
P[15:0]	O	8maR	92,91,90 88,87,86,85,84, 83,82,81,79,78, 76,75,74,73,72,71		
SLD[7:0]	O	8maR	75,76,78,79,85, 86,87,88	True	These signals contain the lower data for color STN LCD panels .
SUD[7:0]	O	8maR	71,72,73,74,81, 82,83,84	True	These signals contain the upper data for color STN LCD panels .
LD[3:0]/ED[3:0]	O	8maR	75,76,78,79	True True	These signals contain the lower data for gray dual-scan LCD panels . These signals contain the even data for gray PLASMA/EL panels .
UD[3:0]/OD[3:0]	O	8maR	71,72,73,74	True True	These signals contain the upper data for gray dual-scan LCD panels . These signals contain the odd data for gray PLASMA/EL panels .

* Power Management Pins (5 pins)

ACTI	I (I/O)	-	53	High	The ACTI output is an active high signal that is driven high every time a valid VGA access (memory or I/O read/write).
FPVCC	O	8maR	62	High	This signal is part of the flat panel power-down sequencing and should be connected to the flat panel LOGIC power enable . (default = 1)
FPVEE	O	8maR	61	High	This signal is part of the flat panel power-down sequencing and should be connected to the flat panel BIAS power enable . (default = 1)
FPBACK	O	8maR	54	High	This signal is part of the flat panel power-down sequencing and should be connected to the flat panel BACKLIGH enable . (default = 0)
OFF	I/O	4maR	178	High	This input is used to force TP6508 into Off mode enable. This pin can also redefined as an output to indicate the active status . It may be also configed as other function- by extended register.

Flat Panel Interface Table

Pin Number	Pin Name	Mono LCD	Color LCD	Color LCD*	Color LCD	Color LCD	Color LCD	Gray	Gray
		Dual-scan STN	Single-scan STN	Dual-scan STN	Dual-scan STN	TFT	TFT	PLASM	EL
		8-bit	16-bit	8-bit	16-bit	9/12/16-bit	18/24-bit	8-bit	8-bit
70	**SHFCLK**	SCLK	CL2	CL2	CL2	DCLK	DCLK	CLK	VCLK
68	**LP**	LCLK	CL1	CL1	CL1	LP/HS	LP/HS	HSYNC	HS
67	**FLM**	FLM	FLM	FLM	FLM	FLM/VS	FLM/VS	VSYNC	VS
69	**M**	MDL	M	M	M	DE	DE	DISPTMG	DE
71	**P0**	UD3	SUD7	SUD7	SUD7	B0	B0		
72	**P1**	UD2	SUD6	SUD6	SUD6	B1	B1		
73	**P2**	UD1	SUD5	SUD5	SUD5	B2	B2		
74	**P3**	UD0	SUD4	SUD4	SUD4	B3	B3		
75	**P4**	LD3	SUD3	SUD3	SLD7	B4	B4		
76	**P5**	LD2	SUD2	SUD2	SLD6	G0	B5		
78	**P6**	LD1	SUD1	SUD1	SLD5	G1	B6		
79	**P7**	LD0	SUD0	SUD0	SLD4	G2	B7		
81	**P8**		SLD7		SUD3	G3	G0	OD3	OD3
82	**P9**		SLD6		SUD2	G4	G1	OD2	OD2
83	**P10**		SLD5		SUD1	G5	G2	OD1	OD1
84	**P11**		SLD4		SUD0	R0	G3	OD0	OD0
85	**P12**		SLD3		SLD3	R1	G4	ED3	ED3
86	**P13**		SLD2		SLD2	R2	G5	ED2	ED2
87	**P14**		SLD1		SLD1	R3	G6	ED1	ED1
88	**P15**		SLD0		SLD0	R4	G7	ED0	ED0
90	**P16**						R0		
91	**P17**						R1		
92	**P18**						R2		
93	**P19**						R3		
94	**P20**						R4		
95	**P21**						R5		
96	**P22**						R6		
97	**P23**						R7		

* : Color Dual-scan STN LCD Panel with external frame buffer

[84.05.29 508PNL.TBL]

Symble	Type	Drive	Pin Number	Active	Function

* Video Interface (26 pins)

VR[7:0]	I/O	4maR	103,104,122,121,120, 119,100,154	True	Red data for the Video-In input by external PC-Video system.
VG[7:0]	I/O	4maR	118,117,116,115,114, 113,98,99	True	Green data for the Video-In input by external PC-Video system.
VB[7:0]	I/O	4maR	112,111,110,109,107, 106,54,53	True	Blue data for the Video-In input by external PC-Video system.
KEY	I/O	4maR	101	True	Color key signal for the Video-In input by external PC-Video system.
PCLK	O	4maR	102	True	Pixel clock input of the Video-In interface by external PC-Video system.
VP[15:0]	I/O	4maR	103,104,122,121,120, 118,117,116,115,114, 113,112,111,110,109, 107	True	VAFC interface video pixel data output.
VRDY	I	-	101	High	VAFC interface video system ready signal.
GRDY	O	4maR	119	High	VAFC interface graphics system ready signal.
EVID#	I	-	106	Low	VAFC interface enable video signal.
VCLK	I	-	100	True	VAFC interface video input clock.

* Power Pins (25 pins)

AVDD1	59	+5V	Internal DAC analog power.
AVDD2	205	+5V	Internal MCLK frequency Synthesizer power.
AVDD3	206	+5V	Internal VCLK frequency Synthesizer power.
BVDD[1:2]	9,42	+5V	Host bus interface power.
CVDD[1:2]	80,181	+5V	Core logical power.
DVDD	66	+5V	Digital pads output power.
MVDDA	158	+5V	Memory bus A interface power.
MVDDB	142	+5V	Memory bus B interface power.
MVDDC	108	+5V	Memory bus C interface power.
AVSS1	56	Ground	Internal DAC analog ground.
AVSS2	202	Ground Ground	Internal MCLK frequency Synthesizer analog ground.
AVSS3	208	Ground Ground	Internal VCLK frequency Synthesizer analog ground.
BVSS[1:4]	12,26,39,52	Ground	Host bus interface ground.
CVSS[1:2]	77,184	Ground	Core logical ground.
DVSS[1:2]	63,89	Ground	Digital pads output ground.
MVSSA	161	Ground	Memory bus A interface ground.
MVSSB	139		Memory bus B interface ground.
MVSSC	105		Memory bus C interface ground.

*** Descript of Type term

O : Output
I : Input
I/O : Birdirectional
OT : Output Tri-state
I/S : Schmitt-trigger Input
U : Internal passive pull-up

* Host Bus Interface Table

Pin Type	Pin Number	Pin Drive	ISA Bus	PCI 32-Bit Local Bus
I/O	-	8maR	SD[15:0]	AD[15:0]
I/O	20	8maR	OWS	AD16
I/O	19	8maR	MEMCS16*	AD17
I/O	18	8maR	IOCS16*	AD18
I/O	-	8maR		AD[31:19]
Input	43		SA0	CBE0#
Input	32		SBHE*	CBE1#
Input	21		SA1	CBE2#
Input	10		REF*	CBE3#
I/O	-	4maR	SA[19:2]	ROMA[17:0]
Input	-		SA20	
I/O	-	4maR	SA21	ROMOE*
Input	201		SA22	CLK
Input	28		SA23	
I/O	29	8maR	ROMCS*	PERR#
I/O	30	8maR	IRQ	SERR#
I/O	53	8maR	(ACTI)	(ACTI)
I/O	54	8maR	(FPBACK)	(FPBACK)
Input	207		RESET	RST#
Input	22		ALE	FRAME#
I/O	31	4maR	AEN	PAR
Input	11		MEMR*	IDSEL
Input	23		MEMW*	IRDY#
OT	24	12maR	IORDY*	TRDY#
I/O	25	12maR	IOWR*	DEVSEL#
I/O	27	4maR	IORD*	STOP#

[86.04.15 508BUS.TBL]

* Pin List

Pin #	Pin Drive	Pin Type	Pin Name	Other Name(s) (ISA Bus)
1	8maR	I/O	AD31	
2	8maR	I/O	AD30	
3	8maR	I/O	AD29	
4	8maR	I/O	AD28	
5	8maR	I/O	AD27	
6	8maR	I/O	AD26	
7	8maR	I/O	AD25	
8	8maR	I/O	AD24	
9		Power	BVDD1	
10		I	CBE3#	REF*
11		I	IDSEL	MEMR*
12		Ground	BVSS1	
13	8maR	I/O	AD23	
14	8maR	I/O	AD22	
15	8maR	I/O	AD21	
16	8maR	I/O	AD20	
17	8maR	I/O	AD19	
18	8maR	I/O	AD18	IOCS16*
19	8maR	I/O	AD17	MEMCS16*
20	8maR	I/O	AD16	OWS
21		I	CBE2#	SA1
22		I	FRAME#	ALE
23		I	IRDY#	MEMW*
24	12maR	OT	TRDY#	IORDY*
25	12maR	I/O	DEVSEL	IOWR*
26		Ground	BVSS2	
27	12maR	I/O	STOP	IORD*
28		I		LA23
29	8maR	I/O	PERR#	ROMCS*
30	8maR	I/O	SERR#	IRQ
31	4maR	I/O	PAR	AEN
32		I	CBE1#	SBHE*
33	8maR	I/O	AD15	SD15
34	8maR	I/O	AD14	SD14
35	8maR	I/O	AD13	SD13
36	8maR	I/O	AD12	SD1
37	8maR	I/O	AD11	SD11
38	8maR	I/O	AD10	SD10
39		Ground	BVSS3	
40	8maR	I/O	AD9	SD9
41	8maR	I/O	AD8	SD8
42		Power	BVDD2	
43		I	CBE0#	SA0
44	8maR	I/O	AD7	SD7
45	8maR	I/O	AD6	SD6
46	8maR	I/O	AD5	SD5
47	8maR	I/O	AD4	SD4
48	8maR	I/O	AD3	SD3
49	8maR	I/O	AD2	SD2
50	8maR	I/O	AD1	SD1
51	8maR	I/O	AD0	SD0
52		Ground	BVSS4	

Pin #	Pin Drive	Pin Type	Pin Name	Other Name(s)
53	8maR	I/O	ACTI	VB0,SDA,CSYNC
54	8maR	I/O	FPBACK	VB1,SCL,CSYNC
55	10ma	Analog Output	RSET	
56		Ground	AVSS1	
57	20ma	Analog Output	BLUE	
58	20ma	Analog Output	GREEN	
59		Power	AVDD1	
60	20ma	Analog Output	RED	
61	20ma	O	FPVEE	FPBACK
62	20ma	O	FPVCC	
63		Ground	DVSS1	
64	12maR	O	VSYNC	
65	12maR	O	HSYNC	CSYNC
66		Power	DVDD	
67	8maR	OT	FLM	
68	8maR	OT	LP	
69	8maR	O	M	
70	12maR	O	SHFCLK	
71	8maR	O	P0	
72	8maR	O	P1	
73	8maR	O	P2	
74	8maR	O	P3	
75	8maR	O	P4	
76	8maR	O	P5	
77		Ground	CVSS1	
78	8maR	O	P6	
79	8maR	O	P7	
80		Power	CVDD1	
81	8maR	O	P8	
82	8maR	O	P9	
83	8maR	O	P10	
84	8maR	O	P11	
85	8maR	O	P12	
86	8maR	O	P13	
87	8maR	O	P14	
88	8maR	O	P15	
89		Ground	DVSS2	
90	4maR	O	P16	CA0
91	4maR	O	P17	CA1
92	4maR	O	P18	CA2
93	4maR	O	P19	CA3
94	4maR	O	P20	CA4
95	4maR	O	P21	CA5
96	4maR	O	P22	CA6
97	4maR	O	P23	CA7
98	4maR	I/O	VG1	CA8
99	4maR	I/O	VG0	CA9
100	4maR	I/O	VR1	VCLK,OEC*
101	4maR	I/O	KEY	VRDY,RASC*
102	4maR	O	PCLK	WEC*,WECH*
103	4maR	I/O	VR7	VP15,CASCL*,WECL*
104	4maR	I/O	VR6	VP15,CASCH*,CASC*

Pin #	Pin Drive	Pin Type	Pin Name	Other Name(s)
105		Ground	MVSSC	
106	4maR	I/O	VB2	EVID#,MCD0
107	4maR	I/O	VB3	VP0,MCD1
108		Power	MVDDC	
109	4maR	I/O	VB4	VP1,MCD2
110	4maR	I/O	VB5	VP2,MCD3
111	4maR	I/O	VB6	VP3,MCD4
112	4maR	I/O	VB7	VP4,MCD5
113	4maR	I/O	VG2	VP5,MCD6
114	4maR	I/O	VG3	VP6,MCD7
115	4maR	I/O	VG4	VP7,MCD8
116	4maR	I/O	VG5	VP8,MCD9
117	4maR	I/O	VG6	VP9,MCD10
118	4maR	I/O	VG7	VP10,MCD11
119	4maR	I/O	VR2	GRDY,MCD12
120	4maR	I/O	VR3	VP11,MCD13
121	4maR	I/O	VR4	VP12,MCD14
122	4maR	I/O	VR5	VP13,MCD15
123	4maR	O	RASB*	
124	4maR	O	WEB*	WEBH*,AA9
125	4maR	O	CASBH	CASB*
126	4maR	O	CASBL*	WEBL*
127	4maR	I/O	MBD0	
128	4maR	I/O	MBD1	
129	4maR	I/O	MBD2	
130	4maR	I/O	MBD3	
131	4maR	I/O	MBD4	
132	4maR	I/O	MBD5	
133	4maR	I/O	MBD6	
134	4maR	I/O	MBD7	
135	4maR	I/O	MBD8	
136	4maR	I/O	MBD9	
137	4maR	I/O	MBD10	
138	4maR	I/O	MBD11	
139		Ground	MVSSB	
140	4maR	I/O	MBD12	
141	4maR	I/O	MBD13	
142		Power	MVDDB	
143	4maR	I/O	MBD14	
144	4maR	I/O	MBD15	
145	4maR	I/O/U	AA0	CFG0
146	4maR	I/O/U	AA1	CFG1
147	4maR	I/O/U	AA2	CFG2
148	4maR	I/O/U	AA3	CFG3
149	4maR	I/O/U	AA4	CFG4
150	4maR	I/O/U	AA5	CFG5
151	4maR	I/O/U	AA6	CFG6
152	4maR	I/O/U	AA7	CFG7
153	4maR	I/O/U	AA8	CFG8
154	4maR	I/O	VR0	32KHZ
155	8maR	O	OEAB*	
156	4maR	O	RASA*	

Pin #	Pin Drive	Pin Type	Pin Name	Other Name(s)
157	4maR	O	WEA*	WEAH*
158		Power	MVDDA	
159	4maR	O	CASAH*	CASA*
160	4maR	O	CASAL*	WEAL*
161		Ground	MVSSA	
162	4maR	I/O/U	MAD0	
163	4maR	I/O/U	MAD1	
164	4maR	I/O/U	MAD2	
165	4maR	I/O/U	MAD3	
166	4maR	I/O/U	MAD4	
167	4maR	I/O/U	MAD5	
168	4maR	I/O/U	MAD6	
169	4maR	I/O/U	MAD7	
170	4maR	I/O/U	MAD8	
171	4maR	I/O/U	MAD9	
172	4maR	I/O/U	MAD10	
173	4maR	I/O/U	MAD11	
174	4maR	I/O/U	MAD12	
175	4maR	I/O/U	MAD13	
176	4maR	I/O/U	MAD14	
177	4maR	I/O/U	MAD15	
178	4maR	I/O	OFF	EXVCLK
179	4maR	I/O	ROMA0	SA2
180	4maR	I/O	ROMA1	SA3
181		Power	CVDD2	
182	4maR	I/O	ROMA2	SA4
183	4maR	I/O	ROMA3	,SA5
184		Ground	CVSS2	
185	4maR	I/O	ROMA4	SA6
186	4maR	I/O	ROMA10	SA7
187	4maR	I/O	ROMA5	SA8
188	4maR	I/O	ROMA11	SA9
189	4maR	I/O	ROMA6	SA10
190	4maR	I/O	ROMA9	SA11
191	4maR	I/O	ROMA7	SA12
192	4maR	I/O	ROMA8	SA13
193	4maR	I/O	ROMA12	SA14
194	4maR	I/O	ROMA13	SA15
195	4maR	I/O	ROMA14	SA16
196	4maR	I/O	ROMA15	LA17
197	4maR	I/O	ROMA16	LA18
198	4maR	I/O	ROMA17	LA19
199		I		LA20
200	4maR	I/O	ROMOE	LA21
201		I	CLK	LA22
202		Ground	AVSS2	
203		I	XTALI	EXMCLK,OSC
204	-	O	XTALO	
205		Power	AVDD2	
206		Power	AVDD3	
207		I/S	RST#	RESET
208		Ground	AVSS3	

VI. Function Descriptions

The TP6508 contains seventeen major functional modules. There are; Host bus interface , Sequencer Control , CRT Controller, Attribute Controller , Graphics Controller , Address Multiplexer , CRT FIFO , Attribute FIFO , Write Buffer , Command FIFO ,Dual frequency Synthesizer , True-Color Palette , Graphics Engine Controller , PC Video Controller , LCD line buffer , Panel Controller , Power Management controller. The main difference between standard VGA and TP6508 is Graphics Engine Controller. We will introduce detail description on this part of the whole function.

The following is an overview of the major elements of the TP6508.

Host Bus Interface

In addition to an ISA bus connection , it can be connected directly to PCI standard local bus interface to provide additional graphics performance without any glue logic .

* ISA Bus

TP6508 supports 16-bit ISA Bus with a high integrated bus interface that no additional logical is require . The TP6508 executes either 8-bit or 16-bit I/O and memory accesses .

* PCI Local Bus

TP6508 can directly connect to 32-bit PCI local bus without any additional logic to support its multiplexed address and data pins, at speeds of up to 33MHz. The TP6508 supports 32-bit data width accesses with memory burst mode , fast back-to-back , byte merge function . It also provides 256k BIOS ROM support and transfers ROM data through VGA to PCI bus .

Sequencer Controller (SEQC)

The Sequencer Controller includes a timing generator. The timing generator produces the basic timing sequence control for the CRTC , ATC, GFXC. It manages the display memory and provides an arbitration for CRT, CPU and Refresh requests. With a deeper CRT FIFO design, the TP6508 performs fast-page mode to fetch display data quickly into CRT FIFO. When CPU accesses the frame memory, it inserts a CPU cycle via the arbitrating state machine to CPU access.

CRT Controller (CRTC)

The CRT Controller includes a cursor control logic, a horizontal logic, a vertical control logic , and the compatible IBM CRTC registers to generate horizontal synchronous and vertical synchronous signals for external raster-scan CRT monitor. It also provides split-screen capability and smooth scrolling. It generates the blank signals that are sent to RAMDAC (True-color palette DAC) to inhibit pixel display on the screen of monitor.

It provides a linear memory address logic and a raster address logic to produce memory address signals for fetching display informations from VGA frame memory.

Attribute Controller (ATC)

The Attribute Controller provides flexible high-speed display shifting and attribute processing. It is designed for both text and graphics VGA display applications.

In text modes, the Attribute Controller takes in eight bits of character code data and eight bits of attribute data via the Graphics Controller. The character code is used to lookup into a character font table that is located in the Map3 of the display memory. The character font data is loaded into a parallel-to-serial shift register. The serial output from the shift register is used to select a foreground or a background color that is assigned in the attribute data byte. Text blinking, underline and cursor are also the responsibility of the Attribute Controller.

In graphic mode, the display data are converted into pixel color data in groups of 16, 8, 2,or 1 adjacent bits, passed through an internal color palette table, and sent out serially to the RAMDAC. In the 256-color mode, the display data is latched twice to form an 8-bit pixel data.

Graphics Controller (GFXC)

The Graphics Controller is the interface between CRT FIFO and both the Attribute Controller during active display and the system microprocessor during display memory reads or writes.

During display, memory data is latched from CRT FIFO and sent to the Attribute Controller. In graphic mode, the parallel memory data is converted to serial bit-plane data before being sent out. In text mode, the parallel attribute data is sent to Attribute Controller directly.

During a system microprocessor writes or reads to display memory, the graphics controller can perform logical operations on the memory data before it reaches display memory or the system micro-processor data bus, respectively. These logical operations consisted of four logical write modes and two logical read modes.

Address Multiplexer (AMUX)

The Address Multiplexer controls the address bus that is sent to the display memory. It includes RAS* , CAS* , WE* , and OE* timing. During the CRT cycle it sent the display memory address that comes from CRT Controller to the display memory for fetching the display information. When a system microprocessor writes or reads the display memory, the Address Multiplexer connects the system microprocessor address bus to the display memory.

When the write buffer function is enabled, a system microprocessor write operation is done first to the Write Buffer logic, then the system address and data signals are latched in the logic. The Sequencer Controller inserts a CPU cycle to perform a write operation by a request coming from Write Buffer logic. At this time, the Address Multiplexer logic connects the address latched by Write Buffer to display memory.

CRT FIFO (Display FIFO)

The CRT FIFO logic is the interface between display memory and the Graphics controller during the CRT cycle. The Sequencer Controller takes an arbitration between CRT, CPU and Refresh cycle. Because the CRT cycle has the highest priority, the Sequencer Controller can perform a vast fast-page mode to fetch the display data and latch those data into the CRT FIFO. During display , the Graphics Controller takes the display data from the CRT FIFO by the display sequence.

Two threshold registers is defined as a high and a low indicator of the CRT FIFO. These registers data are then compared with the number of available display data in the CRT FIFO. The compare outputs are sent to the Sequencer Controller for arbitrating operation. When the contents in the CRT FIFO are under the low threshold, the CRT FIFO issues a request to the Sequencer Controller for more CRT cycles. When the contents in the CRT FIFO leaps over the high threshold or reaches full of the FIFO, the CPU gains the highest priority. With this CRT FIFO logic, the TP6508 optimizes system performance.

Attribute FIFO

The dynamic memory cycle allocation architecture is used in TP6508. Specially , in text mode we integrate 12 levels attribute FIFO storing the attribute information latches the text attribute , ASCII data and cursor state in order to improve performance.

The Attribute FIFO logic is the interface between display memory and CRT FIFO during the CRT attribute-accessed cycle in text mode. Two threshold registers is defined as a high and a low indicator of the Attribute FIFO, these registers data compare with the number of available text attribute data in the Attribute FIFO. The content-data are sent to CRT FIFO for arbitrating operation. With the Attribute FIFO logic, the TP6508 optimizes system performance in text mode only .

Write Buffer

When the write buffer function is enabled, a system microprocessor writes to the Write Buffer logic instead of writing directly to the display memory or accessing I/O-write command. A four-stage buffer latches the address, data and other status and maintains a zero wait state write cycle to improve the system performance. If the content of the buffer is not empty, the Write Buffer logic requests the Sequencer Controller to insert a CPU cycle.

For compatibility issue, when the content of the buffer is not empty, the Sequencer Controller holds attempts to read display memory and write I/O register until the TP6508 completes processing all items in the Write Buffer logic.

Dual Frequency Synthesizer

The Dual frequency Synthesizer generates the memory clock (MCLK) and the display clock (VCLK) from a single reference frequency - 14.318MHz . . The frequency of each clock is programmable by setting divisor value in the extended regs. that contains field for PLL (Phase Lock Loop), VOC (Volt-

age Controlled Oscillator and Post divide control.

The PLL parameters for dot /pixel clock (VCLK) are programed VCLK0 or VCLK1 set regs. in SREG C3,C4,C5,C6 and for memory clock (MCLK) are programmed MCLK set regs. in SREG C9,CA. These registers uses to be in conjunction with Denominator and Post Scalar Value Register, is used to determine the frequency of VGA dot clock. These 7 bits numerator (N), 7 bits denominator (D), and 1 bit post scalar (P), for each clock (MCLK or VCLK) determines its frequency according to the following expression:

$$\text{MCLK, VCLK(MHz)} = \frac{\text{OSC} \times [N+1] \times [2P+2]}{[D+1]}$$

OSC = reference frequency / 14.318 MHz

The reference frequency can be generated with an internal crystal controlled oscillator. Alternatively, it can be supplied from an external TTL source by XTAL1 Pin input. A optional feature is implemented that directs TP6508 to provide the memory clock and the display clock from MCLK and VCLK pin.

True-Color Palette DAC (TDAC)

The True-Color Palette DAC block contains the true color Palettes and three 6-bit or 8-bit digital-to-analog converters. It contains three 256x8 color LUT RAMs for all color mode with the capability to display up to 16.8 million colors simultaneously in both RGB and BGR HiCOLOR-24™ formats. It also support both the popular HiCOLOR-15™ format which uses 5 bits/primary color and the HiCOLOR-16™ color format which uses 5 bits for red , 6 bits for the green , and 5 bit for the blue primary color. The total colors available using the HiCOLOR-15™ format are 32768 while the HiCOLOR-16™ format provides 65536 colors.

When the True-Color (16.8M) and Hi-Color (32k/64k) mode isn't activated , it behaves exactly as Pseudo Color format compatible RAMDAC. The color palette, with 256x18-bit entries, converts a color code that specifies the color of pixel into three 6-bit values, one each for red, green, and blue.

It also provides a Monitor Sense logic to output a signal to Input Status #0 Register for determining the presence of the CRT monitor. This output is a logical 0 if one or more of the Red, Green, Blue outputs have exceeded the internal voltage reference level by being connected a loaded or unloaded RGB line. After the VGA BIOS programed the palettes and determined the color/mono or no CRT monitor, we can disable the Monitor Sense logic for saving power consumption.

Graphics Engine Controller (GEC)

The Graphics Engine controller generates the control signals for BITBLT (screen-to-screen, host-to-screen) , Color Expansion (1-bit-per-pixel , font-painting) , Line Drawing , Rectangular Clipping , Rectangular Fill, Pattern Fill, Transparence, and Raster operations. They are specifically designed to speed up applications running under GUI environments such as Windows 3.x , Windows applications , X-windows , Autocad , and other CAD/CAM packages.

It maintains memory address to locate data in display memory and combines the Source data

,Destination data ,and Pattern data to perform writing the result back to the destination area under the control of parameters programmed into the chip. The Destination data and Pattern data must reside in the display memory. The Source data and Color expansion pixel data may reside in display memory or be supplied by the CPU during a graphics accelerated operation.

Optionally, we support the base addressing and the memory map I/O addressing to access those GEC. registers with 16-bit/32-bit data width. It is more convenient to implement the GUI acceleration function in order to improve the software level performance.

All of the accelerated functions are integrated by TP6508 for 8-bit , 16-bit , 24-bit color modes. The encoding of these 256 ROPs is 100% compatible with Microsoft Windows driver interface specification. See Appendix C for a list of Raster Operation.

* Line Drawing

The Graphic Engine implement line drawing function based on the Bresenham's Algorithm . It can draw solid line or dash line by programming the line drawing pattern registers . In the case of drawing dash line , there is one selection to determine whether to keep background data unchanged (transparence) or using the color in "Background Color Registers" as the background color .

The pattern format are one pixel mapped to one bit and the first pixel mapped the MSb of the join 32-bits pattern in registers . For the line drawing pattern , one selection is useful for actual screen display that is only used the lower 8-bits of line drawing pattern and one bit mapped four or three pixels . When we draw a more vertical line , the GEC can produce three pixels per mapped bit . When we draw a more horizontal line , the GEC can produce four pixels per mapped bit .

Another selection is to determine whether is to draw the last pixel of this drawing line or not .

* Bit Block Transfer

Bit block transfer can copy a rectangular image from a source region to a destination region on display memory with raster operation in 256 ROPs code described in appendix C.

* Color Expansion

Color expansion function can expand monochrome image which one bit represent one pixel to two-color image . All the "1" bits in monochrome image expand to the color in Foreground Color Registers . All the "0" bits expand to the color in Background Color Registers or keep the background data unchanged if 'Background transparency enable' bit is enabled .

A useful case of color expansion is filling text in graphic mode . The monochrome data are the character font bitmap data and transfer to TP6508 by writing to "Host to Display Data Transfer Register" .

Some additional notes for 'Color Expansion' need to care is described detail in that description of 'Image Write'.

* Image Write

Image write can transfer color image from host system memory to display memory . The color image data transfer to TP6508 by writing to "Host to Display Data Transfer Register" . The display pixels order of color image is from left to right and from top to bottom if both 'X direction' bit and 'Y direction' bit are programmed to "0" .

Some additional notes for 'Image Write' need to care in programming sequence . The first , if Width-X isn't a double-word alignment number for 'Image Write', we muse add a , two or three dummy bytes to fill the last transfer to a double word at the end of each horizontal line . The second , we usually need to check the 'Command FIFO' status in "Graphics Command FIFO Status Register" at the start of any horizontal line . If one horizontal line needs 32 bytes or less to transfer , then the whole line can be written to TP6508 directly . If one horizontal line needs to transfer more than 32 bytes , it must be done after every 32 bytes have been written to TP6508 that we need to check the 'Command FIFO' status .

* Image Read

Image read can transfer color image from display memory to host system memory . The color image data transfer from TP6508 by reading from "Host to Display Data Transfer Register" . The display pixels order is as same as Image Write .

Also , for 'Image Read' the additional cares about 'Image Write' need to take care .

* Rectangular Fill & Pattern Fill

Rectangular fill can fill a any size rectangular region on display memory using the color in "Foreground Color Registers" . Also, the pattern fill can use a 8-pixel by 8-pixel image that is storied on display memory as pattern source to fill a any size rectangular region on display memory if pattern is selected by 'Raster operation'.

* Rectangular Clipping

Rectangular clipping define a rectangular region where the image data can be written or cannot . If rectangular clipping is enabled , all the graphic engine functions including of 'Line Drawing' , 'BitBlt' , 'Color Expansion' , 'Image Write' , 'Image Read' , and 'Rectangular Fill & Pattern Fill' can only write these pixels that inside the clipping region or on the boundary if the 'Rectangular clipping polarity' bit is set to "0" . Any pixel outside the rectangular region would not be changes .

A another option , GEC can write those pixels that outside clipping region (not including of on the boundary) if the 'Rectangular clipping polarity' bit is set to "1" .

* Color Transparency

Color transparency function can partition the destination pixels into two groups base on its color information . Pixels transfer through GEC with the same color as the "Transparency Color Registers" can not be modified if 'transparency polarity' bit is "0" . Pixels transfer

through GEC with the different color as the "Transparency Color Register" can not be modified if 'transparency polarity' bit is "1" .

In addition , there is a "Transparency Mask Registers" . If the mask bit is "1" , then the color bit of destination pixel is not used in color compare and passes through . These is a example in enhanced 256 color mode . If "Transparency color Registers" is written hex 36 and "Transparency Mask Registers" is written hex 28 and 'transparency polarity' bit is "0" , the destination pixels with color 16h , 36h , 1Eh or 3Eh would not be modified .

Command FIFO

When the Graphics Engine is in operation , we will transfer the necessary parameters (X/Y direction ,source/destination select, major movement , foreground/background color, ... etc..) to TP6508 by through the Command FIFO and write a graphics accelerate function command (Bit block transfer , Color expansion , Line drawing , ... etc..) in the last.

A eight-stage FIFO latches the command data including of graphics accelerate function command and it's parameters and maintains a zero wait state write cycle to improve the system performance. If the content of the FIFO is full , the Command FIFO logic requests the Sequencer Controller to assert the wait cycle until to the FIFO isn't full. A better recommendation was to monitor the 'Graphics Command Status Register' in the group of Graphics Engine Control Register before you write graphics engine command to TP6508.

Hardware Cursor Controller

The Hardware cursor controller supports a 32x32 or 64x64 hardware cursor in 256-color,32k/64k-color and 16.8M-color graphics mode. It supports the two-bit plane cursor data structure which provides two colors plus Transparent and Inverted background color by following the Microsoft Windows driver interface specification. In addition, a Auxiliary Color data function can replace the Inverted background color function optionally . The pattern's data format of any pixel (two-bit) is :

Data bit-1	Data bit-0	Definition
0	0	Hardware cursor Primary color
0	1	Hardware cursor Secondary color
1	0	Transparent
1	1	Inversion or hardware cursor auxiliary color (decided by GAREG 2A bit-15 selection)

Usually , the cursor pattern is stored in the off-screen display memory . The structure of cursor pattern is 16-bytes by 64-line . All the 16-bytes join together from low address to high address and from LSb to MSb to form a 64x2-bit bit-string . The screen display order of cursor pattern from left to right is mapped to bit string from LSb to MSb per two-bits . To write the cursor pattern to display memory can use Image Write or VGA memory write access directly . The cursor pattern start must address at boundary of double-word .

Hardware cursor screen position, type, color selection, and pattern address of the cursor are to be controlled by programming these registers in the group of Graphics engine control registers. The hardware cursor data are allowed of multiple patterns to be storied in display memory and rapidly to be selected one of the patterns as the active cursor's pattern by application program.

The hardware cursor replaces the software mouse cursor and eliminates to store and restore the screen data as changed the mouse position. Typically, the application software initializes the cursor once and only needs to update the screen position by setting registers. So we can provide a smooth-moving mouse pointer by compared with a software mouse.

PC Video Controller

TP6508 allows up to 24-bit of external RGB video data to be input and merged with the internal VGA data stream. The TP6508 can support two forms of video window: 1) color key input and 2) X-Y window keying. The X-Y window key input can be used to position the live video window coordinates.

LCD Line Buffer

For dual-scan STN LCD panels, those panels require the upper and lower panels to refresh simultaneously so that we need additional buffer and logic to implement. The additional buffer is called "LCD frame buffer" storing the STN LCD's refresh data which are half of a whole LCD panel's. In TP6508 we have three frame-buffer technique; shadow frame buffer, external frame buffer, pseudo frame buffer, to accelerate LCD display refresh.

For shadow frame buffer, we can share the off-screen display memory as the LCD frame buffer by programming the upper display memory region. TP6508 also implements a LCD Line buffer to process and store a line of the LCD refresh data at the start of every CRT horizontal raster. The operation sequence of LCD line buffer is executed by the following steps:

1. Read a line of LCD frame data which are used for the present display frame from shadow frame buffer during the horizontal blank cycle.
2. Write a line of LCD frame data which are used for the next display frame to shadow frame buffer by following the step-1 during the horizontal blank cycle.
3. Output to panel controller from LCD line buffer, a set of frame information of pixels which are read from shadow frame buffer are used to display one of the half LCD panel.
4. Generate and store into LCD line buffer from panel controller, a set of the frame information of pixels which will write to shadow frame buffer are used to display another of the half LCD panel for next frame.
5. Continuously, process the step-3 and step-4 until ending a line of LCD frame data during the horizontal display period.
6. Restart from step-1 for next horizontal raster display and repeat for whole frame display refresh.

VGA has the memory bandwidth limitation, but CRT refresh rate higher than memory fetch speed. By external frame buffer technique, we can add another external 256Kx16-bit DRAM-C as a LCD frame buffer. The video-in and pin[8:15] of Panel is also by DRAM-C interface.

In addition, the another solution for dual-scan STN LCD panel display is used the pseudo frame buffer technique. It is no additional memory required, but it gets rather lower LCD display contrast than others. It is designed to optimize cost and quality trade-off considerations.

Panel Controller

The Panel Controller redefines data format from Attribute Controller in LCD/PLASMA/EL display modes. The TP6508 can directly drive various flat panels, including dual-scan/single-scan monochrome, color STN, and color TFT.

For monochrome LCD/PLASMA/EL panels, it converts FP0-FP7 to gray level and goes through a special functional operation, sum_to_gray, which is called Gray Scaling. For color LCD panels, it converts FP0-FP23 to R.G.B. color level and goes through two special functional operation, which are called Dithering and Amplitude modulation .

The VGA standard defines how colors are mapped to 64 gray scale values on monochrome monitors. The mapping is based on the following weighting equation:

$$I=0.30R+ 0.59G+ 0.11B$$

This formula follows the NTSC conversion standard and is confirmed to display the original color information.

Basically, monochrome flat panels do not actually show shades of gray, but only black and white. To build a gray scale, some pixels stay white proportionally longer than they are dark, depending on the shade of gray being built up. Gray scaling (pattern modulation) techniques determine which pixels are white or dark for corresponding gray level. If not done well, “Flicker” and “ripples” will occur.

Others, the gray scaling techniques also can be using for color flat panel display. Of course it will be occurred on color STN LCD panels that those problems are talking in previous paragraph. The TP6508 controller support both 8 and 16 bit interfaces to STN panels; 9-bit /12-bit/15-bit or 18-bit/ 24-bit interface TFT color LCD panels.

In addition, 65536 simultaneous colors are supported for color STN LCD panels, and up to 226,981 visual colors are supported by color dithering techniques. For color TFT LCD panels, TP6508 can support 16.8M simultaneous colors on 24-bit interface. Further more, 512 simultaneous colors are supported for 9-bit interface color TFT LCD panels, and up to 185,193 visual colors are supported by amplitude modulation techniques.

To avoid flicker and ripple phenomenon. There are three approaches:

(1) increase frame rate:

The higher the switching rate, the better the display quality.

(2) adequate modulation sequences:

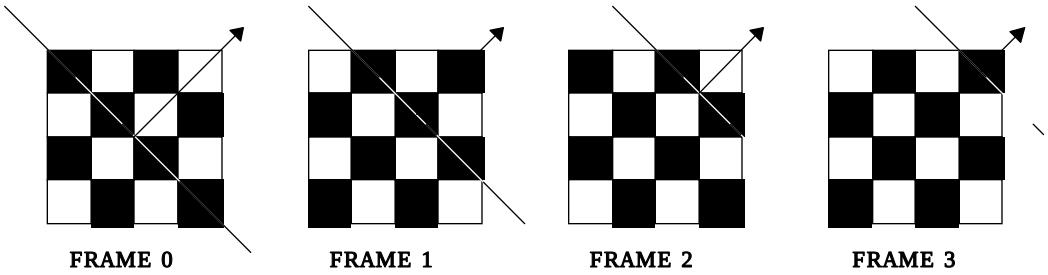
Spread pixels frame ON time on continuous “timing”.

(3) dispersion modulation:

Enhance modulation task from time spreading to spatial spreading each pixel on/off ratio does not change, but has “time shift for neighboring pixels.

* Gray Scaling

Gray scaling is the continuous frame ON/OFF ratio according to the corresponding gray level. We can do 2/4 gray level for pixels as follow:



But notice how the dark pixels line up in diagonal columns. These rows of diagonal columns create regular striations marching across the gray region cycle by cycle.

Alternating the pixels other ways doesn't solve the problem but only creates vertical or other diagonal columns. If not designed correctly, a controller will exhibit diagonal columns jitter or scrambled movement across gray regions, greatly degrading display quality.

How to eliminate the stripping wave become the key point of the panel VGA design. Basically, manufactures obey the following rules:

(1) Pixels On/Off ratio are proportional to gray level.

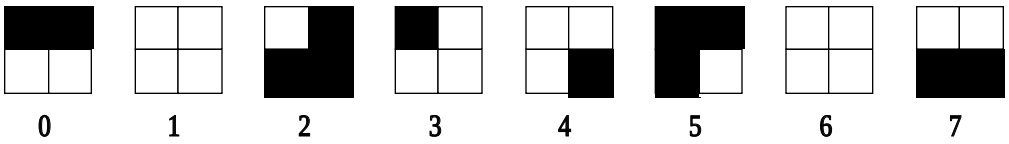
(2) The modulation sequence of neighboring pixels are uncorrelative to reduce stippling wave.

$S^{0}_{3/8}$	$S^{1}_{3/8}$
$S^{2}_{3/8}$	$S^{3}_{3/8}$

Frame / Seq.	0	1	2	3	4	5	6	7
$S^{0}_{3/8}$	*1*	*0*	*0*	*1*	*0*	*1*	*0*	*0*
$S^{1}_{3/8}$	*1*	*0*	*1*	*0*	*0*	*1*	*0*	*0*
$S^{2}_{3/8}$	*0*	*0*	*1*	*0*	*0*	*1*	*0*	*1*
$S^{3}_{3/8}$	*0*	*0*	*1*	*0*	*1*	*0*	*0*	*1*

NOTE : 1 = ON , 0 = OFF

We can see the following situation:



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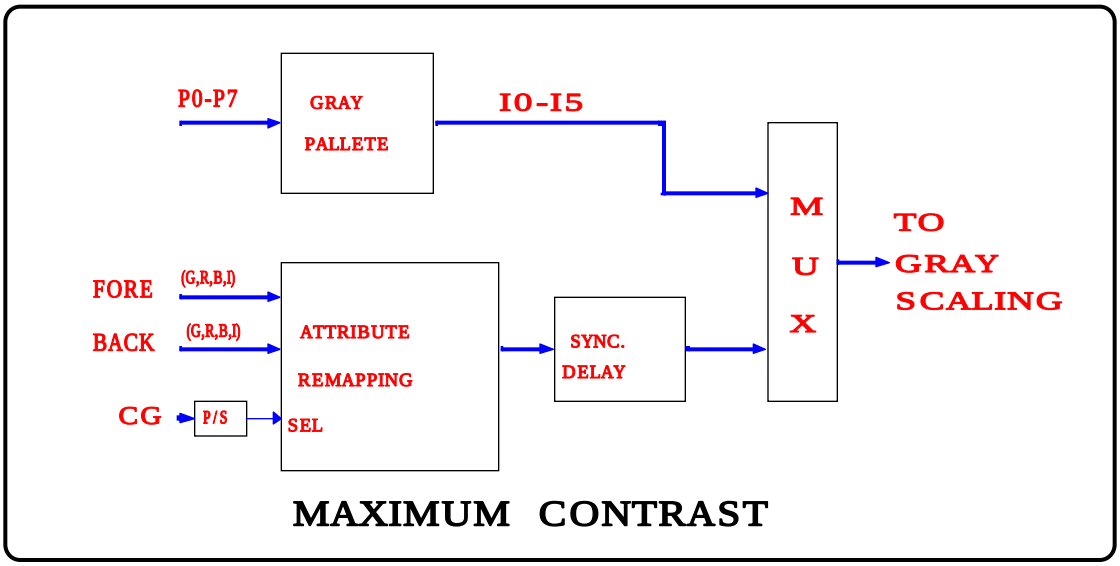
According to the above rules, we can see the ambiguous stippling wave. It is clear that we find a method to eliminate wave phenomenon. But now another problem appear, how to find the best modulation sequence for all gray levels, so the adequate trade-off are needed.

* Maximum Contrast and Attribute Emulation

When color text converts to mono LCD panel mode, remapping gray levels between foreground and background are probably to the same gray level. It is difficult to recognize text forms on the screen. We provide user 'maximum contrast' option to enhance LCD display contrast. The operation as following:



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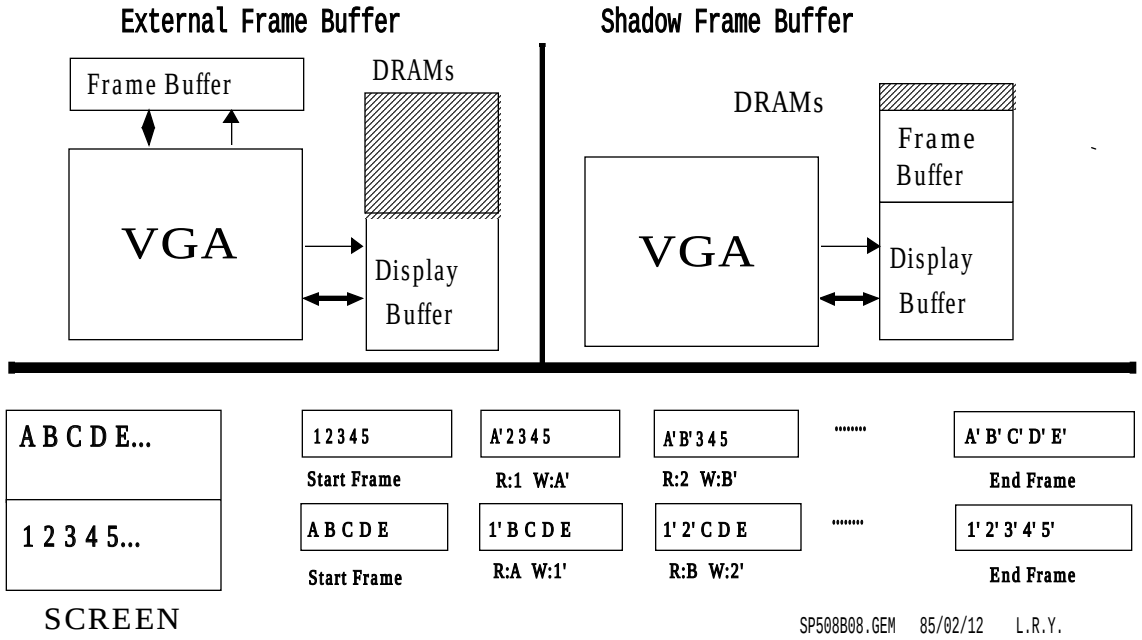
When foreground attribute (G0,R0,B0,I0) is larger than background attribute (G1,R1,B1,I1), we set (G0,R0,B0,I0) = (1,1,1,1) = 63 gray level, (G1,R1,B1,I1) = (0,0,0,0) = 0 gray level.When (G0,R0,B0,I0) = (G1,R1,B1,I1), we reverse the original attribute gray level.

There is another option called attribute emulation. The user enable the 'attribute emulation' function. Attribute Remapping does eight clear contrast automatically, so user can get the best looking in the text mode.

* Frame Buffer

For dual-scan STN LCD panel , we must use "acceleration mode ". We can use the shadow frame buffer technique to fixed it . In the others, VGA has the memory bandwidth limitation , but CRT refresh rate higher than memory fetch speed. How to solve this series problem , we can add another external 256Kx16-bit DRAM as a LCD frame buffer.



When VGA scans upper panel, frame buffer stores the pixel data of lower panel . Every pixel needs only one bit to present on/off information . We provide following figures to show operating procedure:

Left diagram appears actual screen circumstance . A,B,C,D.. AND 1,2,3,4 are the continuous pixels of upper/lower panel. Right rectangles present the interior data of screen buffer . VGA does read-modify-write to the frame buffer consecutively . Upper buffer presents continuous process of scanning VGA upper panel, so does lower panel .

* Color Dithering

For color STN LCD panel , TP6508 can add visual colors by color dithering techniques . The dithering technique uses a group of dithering pattern in 4 by 4 pixel-block and gray modulation to generate the gray shades for each of R,G,B . The dithering patterns for each shades is designed so that it creates minimum flicker and stripping wave on the panel screen.

In the extended indexed register CREG A9 , we can select the various dither algorithm and types to increase colors of the panels .

* Amplitude Modulation

For color TFT LCD panel, TP6508 can add visual colors except the 24-bit true color panel by

color amplitude modulation techniques. The red, green, blue color data that directly come from the palette RAM provide the code for each color. The amplitude modulation technique uses a group of weighting codes and frame (time) modulation to generate the shading information for each of R,G,B.

In the extended indexed register CREG A8 , we can select the various amplitude modulation types to increase colors of the panels .

* Display Combination

The new generation of LCD VGA provides a simultaneous CRT/LCD or CRT/PLASMA display function . This adds a new dimension to the promotional application of portable computers by offering a more versatile visual demonstration . TP6508 also provides this function to extend added value to portable computer. In order to accommodate the limited minimum signal width of CRT VGA, the working frequency of the LCD VGA should at least be 6MHz . The TP6508 will provide a Frame Rate of about 120Hz at this working frequency.

In spite of the above, the CRT VGA still has its draw backs when used for commercial demonstration because of its limited size . With the arrival of low priced TV's (60" to 120"), why not harness the big TV screen to reproduce the portable computer LCD display? To achieve this function, TP6508 has integrated the TV interface synchronization signal circuit . It needs only one analog IC to externally convert the RGB and synchronization signal to RS-170 standard signal for TV . The RS-170 signal is then transmitted through AV terminal to TV . TP6508 has overcome the technical problem of interlaced scan on LCD . This makes the simultaneous display of TV/LCD come true. Presently, TP6508 supports NTSC and PAL TV standard. The SECOM standard support will be available in the future.

* TV Interface

The simultaneous display on both TV and LCD panel is rather an unique design of TP6508. There are many add-on cards or devices on the market which can convert VGA signal to TV display signal, but they can not accomplish a simultaneous display on LCD . The reason is that it is not as easy to perform a interlaced scan on LCD as on CRT . This problem has to be resolved from the internal logic design of VGA.

On the other hand, TP6508 can generate synchronization signal that completely matches with the standard of RS-170. With an external NTSC encoder (A example , MC1377 , is set in Application Circuit chapter) , TP6508 can transmit image to TV through A/V terminal . In order to preclude flickering on TV display, TP6508 uses a non-interlaced scan to stabilize the Frame Rate at 60Hz . Under this Frame Rate, all display modes of IBM VGA are supported. The optimum resolution is 640x480 with 256 colors.

Under TV display mode, the HSYNC signal which is originally sent to VGA are converted to composite sync signal . This composite signal combines the horizontal sync, vertical sync and the equalization pulse . It is necessary of the 3.58 MHz crystal to generate a reference frequency for color burst signal. This frequency is used as the color calibration signal if adjusted by variable capacitor . Due to the limitation of TV's resolution and Frame Rate, the displayed image may not be as good as that of VGA display, but its display of big fonts and graphics as in a commercial demonstration and presentation, is distinctively sharp .

Power Management Controller (P.M.C.)

The TP6508 has a special function which is a power management unit to generate the power control signals for Dual frequency synthesizer , RAMDAC, other block devices of TP6508, and Montor output timing . It's implemented with the VESA DPMS(Display Power Management Signaling) standard and designed to provide power management for Green PC systems . The TP6508 provides trigger pins and timers to determine when the system is idle . When idle, the TP6508 can remove power from unused internal block devices . The TP6508 also supports slow refresh DRAM for power saving.

The TP6508 has four main operating modes: Active mode, Standby mode , Suspend mode , and Off mode. The I/O read/write (register programming/keyboard request) , external trigger pins, and the time-out control the transition between each mode . TP6508 supports one external trigger pins , OFF pin .

DPMS States:

State	HSYNC	VSYNC	CRT	Flat Panel	Power Saving
On(Active)	Pulses	Pulses	Active	Active	None
Standby	No Pulses	Pulses	Blanked	Blanked	Minimal
Suspend	Pulses	No Pulses	Blanked	Blanked	Substantial
Off	No Pulses	No Pulses	Blanked	Blanked	Maximum
Cover-Close	Pulses	Pulses	Active	Blanked	Minimal

* DPMS Operating Modes:

1. On(Active) Mode

This is the start-up or wake-up mode of the system. The CPU is operating at maximum speed . Fixed disks and floppy are working with normal situation and the VGA is active normal .

2. Standby Mode

Standby mode is the first power saving mode . The standby mode is entered from the active mode when the time specified by the P.M.C. time-out register, or user I/O register programming . Resume may be initiated by I/O register programming, or keyboard request . There are no CRT cycle on in this mode and turns off internal DAC . But video memory and register access allowed.

3. Suspend Mode

Suspend mode is the lower power saving mode . It is as same as the standby mode to TP6508's internal power saver except the output of HSYNC and VSYNC signal for various power saving mode monitor by VESA DMPS standard. The different display sync output between Standy mode and Suspend mode is descripted on previous 'DMPS States' table . Suspend may be initiated by the P.M.C. time-out register, or user I/O register programming . Resume may be initiated by I/O register programming , keyboard request.

4. Off Mode

Off mode is the lowest power mode . It may be initiated by the P.M.C. time-out register, user I/O register programming or OFF/SUSPEND pin input . Resume may be initiated by the OFF pin external trigger input. In this mode, system will turn off CPU cycle, CRT cycle, screen buffer, display signal, internal dual frequency synthesizer and internal DAC , meanwhile, does DRAMs slow refresh. Display memory and register accessing isn't allowed .

5. COVER-CLOSE MODE

Cover-close mode is the special power mode using for laptop PC. or Notebook PC. system on closing the machine-cover . Specially, this mode replace OFF mode when the user programmed the extended register 3c4/3c5 index D2h bit 7 to logical 1 . It may be initiated by the OFF pin. Resume may be initiated by external trigger input . In cover-close mode, system will turn off panel backlight, and down saving internal partial panel block device power . Then the CRT display is normal.

1->2
* I/O Register Programming
* Standby timer time-out

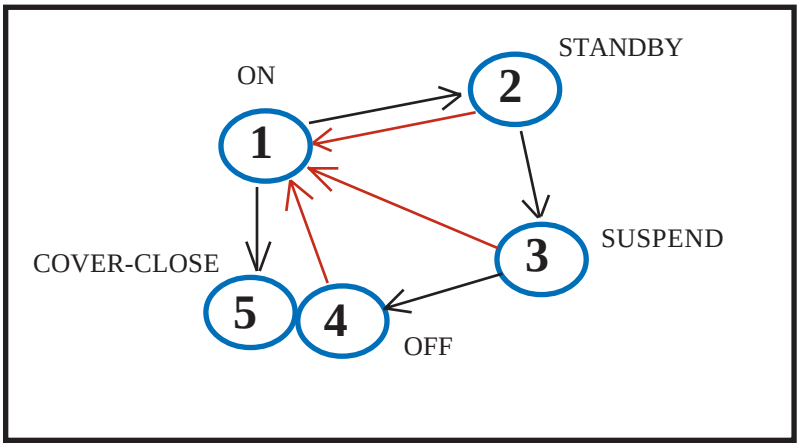
2->3
* I/O Register Programming
* Suspend timer time-out

3->4
* I/O Register Programming
* Off timer time-out
* OFF pin active

2->1
* Keyboard request
* VGA access

3->1
* Keyboard request
* VGA access

4->1
* Keyboard request
* VGA access
* OFF pin not active

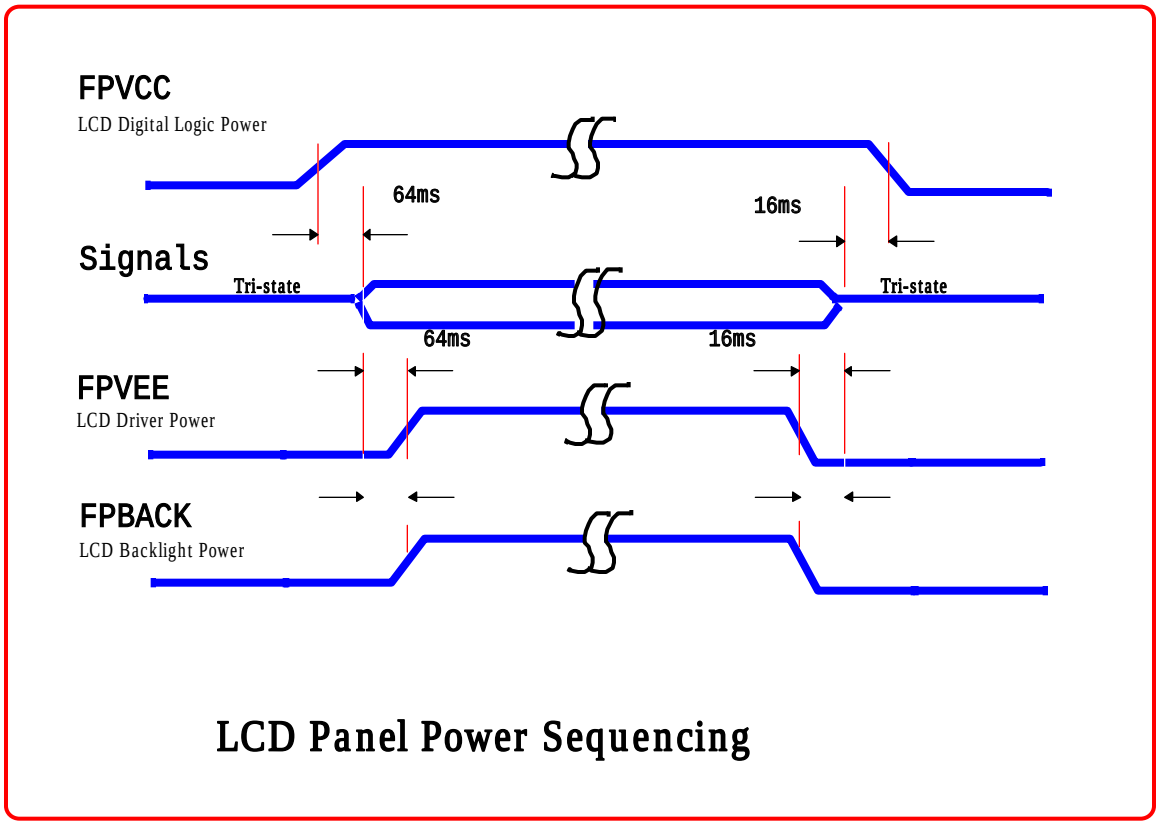


* Flat Panel Power sequencing

The TP6508's power supply management design is very flexible . The following Figure shows the timing diagram and the control signals related to power supply management . It is a very helpful reference for VGA designing with portable or notebook computers .

It is worth mentioning that the FPVCC, FPVEE, and FPBACK signals can effectively resolve problems of LCD power sequencing . The FPVCC signal is used to turn On/OFF the digital power(+5 Volt) for the digital logic of the LCD panel . The FPVEE signal is sent to bias voltage generator of the LCD panel driver for control signal ON/OFF application . The FPBACK signal can be sent to the back-light voltage generator to administer ON/OFF control .

There must be a 64ms skew between the FPVCC's and FPVEE's timing during power on(into On mode) sequence and be a 16ms skew during power off (into Standby/Suspend/Off/Cover-Close mode) sequence . The sequence is reversed between Power On and Power Off. For the convenience of design, the length of skew is fixed and not adjustable, but Topro is confident that this skew will satisfy the requirement of most panels .



LCD Panel Power Sequencing

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VII. Registers

TP6508 contain seven groups of registers . These are IBM Standard Register Backward Compatible Register , Extended Sequencer Register , Extended CRTC Register , Panel Control Register , PCI Local Bus Configuration Register, Graphics Engine Register.

IBM Standard Register

There are five sets of registers in the video subsystem. All but the system microprocessor data latches and the attribute address flip-flop are readable. The following figure lists the registers and the I/O address where they are located. The figure also lists whether or not they are read/write, read-only, or write-only.

* General Registers

Misc. Output Register (MISCREG: R/3CCH, W/3C2H)

D0 I/O address select (0/3BXH, 1/3DXH)
D1 Enable video RAM (active high, no effect on display refresh)
D2 Clock select 0 (00/25MHz, 01/28MHz)
D3 Clock selcet 1 (10/auxi., 11/45MHz)
D4 Reserved
D5 Odd/Even page select (for diagonostic use)
D6 Horizontal sync. polarity select (0/positive, 1/negative)
D7 Vertical sync. polarity select (0/positive, 1/negative)

Input Status Register 0 (INSTREG0 : R/3C2H)

D0-3 Reserved
D4 Switch sense bit (match with clock select 0/1)
D5-6 Reserved (0)
D7 CRT interrupt (0/cleared, 1/pending)

Input Status Register 1 (INSTREG1 : R/3?AH)

D0 Display enable (active low)
D1-2 Reserved
D3 Vertical retrace (VGA) /CG out (Herculus)
D4 Color plane register check 0 (P0, P4, P1, P6)
D5 Color plane register check 1 (P2, P5, P3, P7)
D6-7 Reserved

Feature Control registe (FEATREG: R/3CAH, W/3?AH)

D0-7 Reserved

VGA DAC I/O Ports

3C6H Pixel mask register
3C7H DAC state register (read only, VGA support D0-D1)
3C7H Look-up table read index (write only, RAMDAC support)
3C8H Look-up table write index
3C9H Look-up table data register

* Sequencer Registers

Sequencer Address Register (SEQIDREG : RW/3C4H)

D0-7 SEQUENTIAL ADDRESS BITS (00-FF)

Reset Register (SR00 : RW/3C5H)

D0 Asynchrous reset (active low)
D1 Synchrous reset (active low)
D2-7 Reserved

Clocking Mode Register (SR01 : RW/3C5H)

D0 8/9 dot clocks select (0/9, 1/8)
D1 Reserved
D2 Shift load (0/normal, 1/divide 2)
D3 Dot clock (0/normal, 1/divide 2)
D4 Shift 4 (0/D2, 1/divide 4)
D5 Screen off (active high)
D6-7 Reserved

Map Mask Register (SR02 : RW/3C5H)

D0-3 Enable map 0-3 (active high)
D4-7 Reserved

Character Map Select Register (SR03 : RW/3C5H)

D0 Character generator table select B
D1 Character generator table select B
D2 Character generator table select A
D3 Character generator table select A
D4 Character generator table select B (MSB)
D5 Character generator table select A (MSB)
D6 Reserved

Memory Mode Register (SR04 : RW/3C5H)

D0 Reserved
D1 Extended memory (0/64k, 1/256k)
D2 Odd/Even (active low)
D3 Chain 4 (256 colors only, active high)
D4-7 Reserved

* CRT Registers

CRT Address Register (CRTIDREG : RW/3?4H)

D0-4 Sequential address bits
D5-7 Reserved

Horizontal Total Register (CR00 : RW/3?5H)

D0-7 Horizontal total (-5)

Horizontal Display Enable End Register (CR01 : RW/3?5H)

D0-7 Horizontal display enable end (-1)

Start Horizontal Blanking Register (CR02 : RW/3?5H)

D0-7 Start Horizontal Blanking (-1)

End Horizontal Blanking Register (CR03 : RW/3?5H)

D0-4 End horizontal blanking bit 0-4
D5-6 Display enable skew bit 0-1
D7 Test (1)

Start Horizontal Retrace Pulse Register (CR04 : RW/3?5H)

D0-7 Start horizontal retrace pulse bit 0-7

End Horizontal Retrace Register (CR05 : RW/3?5H)

D0-4 End horizontal retrace bit 0-4
D5-6 Horizontal retrace skew bit 0-1
D7 End horizontal blanking bit 5

Vertecal Total Register (CR06 : RW/3?5H)

D0-7 Veratical Total bit 0-7 (-2)

CRTC Overflow Register (CR07 : RW/3?5H)

D0 Vertical total bit 8
D1 Vertical display enable end bit 8
D2 Vertical retrace start bit 8
D3 Start vertical blank bit 8
D4 Line compare bit 8
D5 Vertical total bit 9
D6 Vertical display enable end bit 9
D7 Vertical retrace start bit 9

Preset Row Scan Register (CR08 : RW/3?5H)

D0-4 Preset row scan (pexil scrolling)
D5-6 Byte panning control bit 0-1
D7 Reserved

Maximum Scan Line Register (CR09 : RW/3?5H)

D0-4 Maximum scan line bit 0-4
D5 Start vertical blank bit 9
D6 Line compare bit 9
D7 200—>400 line conversion

Cursor Start Register (CR0A : RW/3?5H)

D0-4 Row Scan cursor start bit 0-4
D5 Cursor off (active high)
D6-7 Reserved

Cursor End Register (CR0B : RW/3?5H)

D0-4 Row Scan cursor end bit 0-4
D5-6 Cursor skew bit 0-1
D7 Reserved

Start Address High Register (CR0C : RW/3?5H)

D0-7 High order start address bit 0-7

Start Address Low Register (CR0D : RW/3?5H)

D0-7 Low order start address bit 0-7

Cursor Location High Register (CR0E : RW/3?5H)

D0-7 High order cursor location bit 0-7

Cursor Location Low Register (CR0F : RW/3?5H)

D0-7 Low order cursor location bit 0-7

Vertical Retrace Start Register (CR10 : RW/3?5H)

D0-7 Low order vertical start bit 0-7 (10 bits total)

Vertical Retrace End Register (CR11 : RW/3?5H)

D0-3 Vert. retrace end bit 0-3
D4 Clear vert. interrupt
D5 Enable vert. interrupt
D6 Select refresh cycles (0/3 cycle, 1/5 cycle)
D7 Protect CR00-CR07

Vertical Display Enable End Register (CR12 : RW/3?5H)

D0-7 Low order vert. display enable end bit 0-7 (-1) (10 bit total)

Offset Register (CR13 : RW/3?5H)

D0-7 Logical line width of the screen bit 0-7

Underline Location Register (CR14 : RW/3?5H)

D0-4 Underline location bit 0-4
D5 Count by 4
D6 Doubleword Mode
D7 Reserved

Start Vertical Blanking Register (CR15 : RW/3?5H)

D0-7 Low order vertical blanking bit 0-7 (-1) (10 bits total)

End Vertical Blanking Register (CR16 : RW/3?5H)

D0-7 End vertical blanking bit 0-7

CRT Mode Control Register (CR17 : RW/3?5H)

D0 RA0 replace MA13 (active low)
D1 RA1 replace MA14 (active low)
D2 Hor.retrace select (0/normal, 1/double scan)
D3 Memory address count by 2 (0/byte refresh, 1/word refresh)
D4 Reserved
D5 Address wrape (0/MA13:64k, 1/MA15: 256k)
D6 Word/Byte mode (0/normal, 1/MA13 or MA15 replace MA0)
D7 Hardware reset (active low , reset VR and HR)

Line Compare Register (CR18 : RW/3?5H)

D0-7 Low order compare line number bit 0-7 (10 bits total)

* Graphics Registe

Graphics address Register (GFXIDREG : RW/3CEH)

D0-4 Graphics address bit 0-4
D5-7 Reserved

Set/Reset Register (GR00 : RW/3CFH)

D0-3 Set/Reset map bit 0-3
D4-7 Reserved

Enable Set/Reset Register (GR01 : RW/3CFH)

D0-3 Enable Set/Reset map bit 0-3
D4-7 Reserved

Color Compare Register (GR02 : RW/3CFH)

D0-3 Colore Compare map bit 0-3
D4-7 Reserved

Data Rotate Register (GR03 : RW/3CFH)

D0-2 Rotate count bit 0-2
D3 Function select bit 0 (00/unmodified, 01/ANDed)
D4 Function select bit 1 (10/ORed, 11/XORed)
D5-7 Reserved

Read Map Select Register (GR04 : RW/3CFH)

D0 Map select bit 0 (00/Map 0 , 01/Map 1)
D1 Map select bit 1 (10/Map 2 , 11/Map 3)
D2-7 Reserved

Graphics Mode Register (GR05 : RW/3CFH)

D0 Write mode bit 0 (00/dirct write, 01/latch write)
D1 Write mode bit 1 (10/packed write, 11/SR write)
D2 Reserved
D3 Read type (0/map select read, 1/color compare read)
D4 Odd/Even (active high, for Text mode)
D5 Shift register ode (for CGA mode 4,5)
D6 256 color mode (active high)
D7 Reserved

Graphics Misc. Register (GR06 : RW/3CFH)

D0 Graphics enable (active high)
D1 Chain odd and even maps
D2 Memory address select (00/A0000-BFFFF, 01/A0000-AFFFF)
D3 Memory address select (10/B0000-B7FFF, 11/B8000-BFFFF)
D4-7 Reserved

Color Don’t Care Register (GR07 : RW/3CFH)

D0-3 Plan 0-3 Color Don’t care
D4-7 Reserved

Bit Mask Register (GR08 : RW/3CFH)

D0-7 Mask data bit 0-7

* Attribute Registers

Attribute Address Register (ATRIDREG : RW/3C0H)

D0-4 Graphics address bit 0-4
D5 Palette address source (0/CPU, 1/CRTC)
D6-7 Reserved

Pallete Register (AR00-AR0F : R/3C1H, W/3C0H)

D0-5 P0-5
D6-7 Reserved

Attribute Mode Control Register (AR10 : R/3C1H, W/3C0H)

D0 Graphics/Text mode select (0/text, 1/graphics)
D1 Color/mono emulation (0/color , 1/mono)
D2 Enable line graphics characters (ACSII C0-DF, active high)
D3 Attribute code (0/select ackground, 1/enable blink)
D4 Reserved
D5 PEL panning compatiblity with the line compare (active high)
D6 PEL width (0/normal, 1/256 colors)
D7 P5/p4 select source (0/normal, 1/color select reg.)

Over-scan Color Register (AR11 : R/3C1H, W/3C0H)

D0-7 Over scan color bit 0-7

Color Plan Enable Register (AR12 : R/3C1H, W/3C0H)

D0-3 Enable plan 0-3
D4 Video status MUX bit 0 (00/P2-P0, 01/P5-P4)
D5 Videl status MUX bit 1 (10/P3-P1, 11/P7-P6)
D6-7 Reserved

Horizontal PEL Panning Register (AR13 : R/3C1H, W/3C0H)

D0 Horizontal PEL panning bit 0-3
D4-7 Reserved

Color Select Register (AR14 : R/3C1H, W/3C0H)

D0-3 Select color 4-7
D4-7 Reserved

Backward Compatible Register Description

The following registers are TP6508 backward compatible registers. These registers are accessed by first writing the index of the desired register to the Sequencer Index register, i.e. address Hex 3C4 and then accessing the register using the address Hex 3C5. Specially , these are not protected by password/Identification register (Extended Index Register Hex 05) .

Extended Indexed Register CREG 05 : Password/Identification Register

This is a read/write register. Port address is Hex 3C5.
Default value after hardware reset is Hex 00.

Write operation (=> Hex 86) :

D0-7 Password

Read operation (=> Hex 0B for correct password or Hex F4 for incorrect passward):

D0-4 Identification Code

D5-7 Chip Version Code

With the password register, the TP6508 protects the extended register to avoid incorrectly application programming. When user wants to access the extended registers, he must first write Hex 86 to this register to unlock the protection. When user reads the content of this register, he can get a value of Hex 0B that is used to distinguish the TP6508. To enable the protection operation by writing other values into the register , and you can read back a value of Hex F4.

Extended Indexed Register SREG 06 : Extended Memory Bank MISC. Register

This is a read/write register. Port address is Hex 3C5.
Default value after hardware reset is Hex 00.

D0 Enable Bank C and Bank D
D1 Disable dual Bank (window) operation for Bank C and D
D2 Enable read/write bank operation
D3-7 Reserved

Bit 0 For compatibility with the HM86305 that has only three bit bank select for up to 512K- byte display memory, a logical 0 directs the bank selection from Bank A , Bank B or both. When this bit is set to a logical 1, the TP6508 enables both Bank C & D and Bank A & B.

Bit 1 Refer the SREG 09 bit 0-5 description. This bit is used to select the BANK D location address from hex. A0000 to hex. AFFFF or from Hex B0000 to Hex BFFFF . A logical 0 selects BANK D addressing in hex. B0000 to hex. BFFFF.

Bit 2 A logical 1 forces BANK C in write access operation and BANK D in read access operation only. Bank C & D are both location at address hex. A0000 to AFFFF . A logical 0 doesn't enable it.

Bit-2	Bit-1	Bit-0	Memory bank & segment selection
0	0	0	BANK A&B R/W access by segment address A000&B000
0	0	1	BANK C&D R/W access by segment address A000&B000
0	1	0	BANK A R/W access by segment address A000 only
0	1	1	BANK C R/W access by segment address A000 only
1	X	X	BANK C Write access & BANK D Read access by segment address A000

Bit 3-7 Reserved.

Extended Indexed Register SREG 07 : CPU Start address Register

This is a read/write register. Port address is Hex 3C5.
Default value after hardware reset is Hex 00.

D0-3 CPU start address bit 0 to 3
D4-7 Reserved

Bit 0-3 These bit are used to set the CPU start address that specifies the offset from original address point to the first byte of BANK 0. It can solve the Bank(Window) boundary problem. The unit size of CPU start address is in 4 KB, so we can adjust the offset address domain from 0 to 60 KB.

Bit 4-7 Reserved.

Extended Indexed Register SREG 08 : Extended Memory Bank C Select Register

This is a read/write register. Port address is Hex 3C5.
Default value after hardware reset is Hex 00.

D0-4 Memory bank C select bit 0 to 4
D5-7 Reserved

Bit 0-4 When the TP6508 is configured with over 512k-byte display memory, a segment memory i.e. , 64K-byte, only access a small part of the display region. These bits help the user to access the remaining pixel data. When the user wants to move lots of pixel data from one bank to another, the microprocessor suffers from executing I/O write to modify the content of the bank select register. With its dual and overlapping windows architecture, operations performance has improved drastically.Each window is associated with a four-bit bank select register. When the user wants to translate a good deal of pixel data from one bank to another, he can programs two bank registers before translation once instead of the modifying every pixel data movement. These bits are associated with the window down address region from Hex A0000 to Hex AFFFF.

Bit 5-7 Reserved.

Extended Indexed Register SREG 09 : Extended Memory Bank D Select Register

This is a read/write register. Port address is Hex 3C5.
Default value after hardware reset is Hex 00.

D0-4 Memory bank D select bit 0 to 4
D5-7 Reserved

Bit 0-4 These bits perform the same function as with the previous register except that they are associated with the window down address region from Hex B0000 to Hex BFFFF under SREG 06 bit-1 being set to logical 0. When SREG 06 bit-1 is set to logical 1, they are associated with the same address region from Hex A0000 to Hex AFFFF.

Bit 5-7 Reserved.

Extended Indexed Register SREG E0,E1,E2 : Scratched Register 1,2,3

This is a read/write register. Port address is Hex 3C5.
Default value after hardware reset is Hex 00.

D0-7 Reserved

Extended Indexed Register SREG EE : Memory Bank Select Register

This is a read/write register.
Port address is Hex 3C5.
Default value after hardware reset is Hex 00.

D0	Dual window operation enable
D1-3	Select Bank B bit 0 to 2
D4-6	Select Bank A bit 0 to 2
D7	Reserved=1

VGA Subsystem Enable Register

This is a read/write register.

Port address is Hex 3C3 or Hex 46E8 selected by VGA Subsystem Enable Port Select control bit that comes from Extended Indexed Reg. Hex CE bit 4. Default value after hardware reset is selected by Extended Indexed Reg. Hex CE bit 5. If this bit is a logical 1 , and then the value is Hex 00 when the port address is Hex 3C3 or is Hex 00 when the port address is Hex 46E8. If this bit is a logical 0 , and then the value is Hex 01 when the port address is Hex 3C3 or is Hex 08 when the port address is Hex 46E8.

D0	VGA subsystem enable (for Port Hex 3C3)
D1-2	Reserved
D3	VGA subsystem enable (for Port Hex 46E8)
D4-7	Reserved

Extended Sequencer Register Description

The following registers are TP6508 extended sequencer registers. These registers are accessed by first writing the index of the desired register to the Sequencer Index register, i.e. address Hex 3C4 and then accessing the register using the address Hex 3C5. These registers are protected by password/Identification register (Extended Index Register Hex 05) .

Extended Indexed Register SREG C0: VGA Control Register

This is a read/write register. Port address is Hex 3C5.
Default value after hardware reset is Hex 00.

D0	Enable CPU write buffer
D1	Disable VGA palette snooping for VESA local bus
D2	Enable linear addressing
D3	Enable memory map I/O
D4	Enable Graphics engine read/write
D5	Graphics engine active enable
D6	Enable VAFC interface
D7	Enable VAFC PCLK output divided by 2

Bit 0 TP6508 support CPU write buffer to improve the performance when CPU writes a data into video memory . A logical 1 enables this function, a logical 0 disables it.

Bit 1 A logical 0 enables TP6508 snoops VGA palette write for VESA local bus . A logical 0 disables it.

Bit 2 IBM compatible display address uses low base 1M address bit 0 to 19 and locates at Hex A0000 to AFFFF or Hex B0000 to BFFFF . A logical 1 enables TP6508 to remape display memory in continuously linear address at over the base 1M-byte address . A logical 0 disables it and forces TP6508 in bank memory addressing on enhanced display mode.

Bit 3 By base addressing, we can used the reg. SREG F0 and SREG F1 to assign the base low address . (See the reg. description of SREG F0 and SREG F1) Then TP6508 can access these registers with 16-bit data width by decoding at them, being conjunction with 'x..' and 'Y..' , directly. By memory map I/O addressing forces TP6508 uses memory command accessing to access I/O command and remapes I/O command address on where are determined by Memory Mapping I/O Command offset Register (See the reg. description of SREG D8).

Bit 3	Addressing mode
0	Base Addressing
1	Memory I/O Addressing

Bit 4 A logical 1 enables to access the Graphics Engine Control registers.

Bit 5 A logical 1 enables TP6508's Graphics Engine in operated mode. A logical 0 disables it .

Bit 6 A logical 1 enables TP6508 implement VAFC interface.

Bit 7 A logical 1 forces TP6508 output PCLK frequency divide by two for VAFC.

Extended Indexed Register SREG C1 : Extended mode select Register

This is a read/write register. Port address is Hex 3C5.
Default value after hardware reset is Hex 00.

D0	Enhanced 16 color mode enable
D1	Enhanced 256 color mode enable
D2	Enable 32k super-colors mode
D3	Enable 64k super-colors mode
D4	Enhanced 16.8M color enable

D5 Enable 132 column text mode
D6 Enable interlace display
D7 Enable bank memory addressing on enhanced 16-color display

Bit 0 A logical 1 directs the TP6508 to work in the enhanced 16 color mode.
Bit 1 A logical 1 forces the TP6508 to display the 256 color except the Mode 13.
Bit 2 When bit-1 was set to logical 1, we can force the build-in internal RAMDAC to support Hicolor-15™ compatible display mode architecture by setting this bit to logical 1.
Bit 3 When bit-1 was set to logical 1, we can force the build-in internal RAMDAC to support Hicolor-16™ compatible display mode architecture by setting this bit to logical 1.
Bit 4 When bit-1 was set to logical 1, we can force the build-in internal RAMDAC to support Hicolor-24™ compatible color display mode architecture by setting this bit to logical 1.
Bit 5 A logical 1 directs the TP6508 to display 132 columns text mode.
Bit 6 A logical 0 directs the TP6508 to perform a non-interlaced display mode. A logical 1 enables a interlaced display mode to fit the synchronous frequency of the monitor.
Bit 7 A logical 1 directs TP6508 to display enhanced 16-color mode by bank memory addressing. A logical 0 directs TP6508 to display enhanced 16-color mode by location continuous 128K-byte memory at A0000 to BFFFF.

Extended Indexed Register SREG C2: Clock Select Register

This is a read/write register. Port address is Hex 3C5.
Default value after hardware reset is Hex 00.

D0-1 Extended clock select bit 0 to 1
D2-3 Reserved
D4 Enable extended clock select bit 0 and bit 1
D5 ACTI statue/data
D6 ACTI Pin(pin 53) output control
D7 Select 16.8M color mode in four-byte architecture

Bit 0-1 When the bit-4 was set to logical 1, these two bits replace the MISCREG bit 2-3. The bit-0 or MISCREG bit-2 is used to select the internal VCLK clock synthesizer programming regs. set for deciding video clock frequency.

MISCREG bit-2 or SREG C2 bit-0	Selected Regs. group
0 :	Use the SREG C3,C5
1 :	Use the SREG C4,C6

Bit 2-3 Reserved.
Bit 4 A logical 1 directs previous two bits as the video clock select signals. A logical 0 inhibits the function of extended clock select bit 0 and 1.
Bit 5 This bit is reflected the ACTI pin status. When ACTI is redefined as user control output that is configured by bit 1, this bit determins the data output on ACTI pin.
Bit 6 When SREG D0 bit 6=1,SREG D9 bit 1-0=11, this bit can select ACTI Pin(pin 53) output function as following:

Bit 6	ACTI Pin Function
0	ACTI output. ACTI responces high during vaild VGA access operations.
1	User control output. Output data from SREG C2 bit 5.

Bit 7 Ture color(16.8M color) display mode memory access architecture selection:

Bit 7	16.8M color mode architecture selection
0	In three-byte memory architecture.
1	In four-byte memory architecture..

Extended Indexed Register SREG C3 : VCLK0 Numerator Value Register

This is a read/write register. Port address is Hex 3C5.
Default value after hardware reset is Hex 9C.

D0-6 VCLK0 numerator bit 0 to 6
D7 VCLK0 oscillation divider

Bit 0-6 This register,in conjunction with VCLK0 Denominator and Post Scalar Value Register, is used to determine the frequency of video clock. These 7 bits numerator (N), 7 bits denominator (D), and 1 bit post scalar (P), for each clock (VCLK) determines its frequency according to the following expression:

$$VCLK(MHz) = \frac{OSC \times [N+1] \times [2P+2]}{[D+1]}, \quad OSC = 14.318\ (MHz)$$

Bit 7 This bit is used to divide the internal generated oscillation frequency. A logical 0 indicates to do it divided by two. A logical 1 indicates to do it divided by four. Normally, we set to logical 1 when VCLK0 outputs frequency lower 50MHz.

Extended Indexed Register SREG C4 : VCLK1 Numerator Value Register

This is a read/write register. Port address is Hex 3C5.
Default value after hardware reset is Hex A8.

D0-6 VCLK1 numerator bit 0 to 6
D7 VCLK1 oscillation divider

Bit 0-6 This register,in conjunction with VCLK1 Denominator and Post Scalar Value Register, is used to determine the frequency of video clock .

Bit 7 This bit is used to divide the internal generated oscillation frequency. A logical 0 indicates to do it divided by two. A logical 1 indicates to do it divided by four . Normally, we set to logical 1 when VCLK1 outputs frequency lower 50MHz.

Extended Indexed Register SREG C5 : VCLK0 Denominator and Post Scalar Value Register

This is a read/write register. Port address is Hex 3C5.
Default value after hardware reset is Hex 83.

D0 VCLK0 post scalar
D1-7 VCLK0 denominator bit 0 to 6

Bit 0-7 This register,in conjunction with VCLK0 Numerator Value Register, is used to determine the frequency of video clock.

Extended Indexed Register SREG C6 : VCLK1 Denominator and Post Scalar Value Register

This is a read/write register. Port address is Hex 3C5.
Default value after hardware reset is Hex A3.

D0 VCLK1 post scalar
D1-7 VCLK1 denominator bit 0 to 6

Bit 0-7 This register,in conjunction with VCLK0 Numerator Value Register, is used to determine the frequency of video clock.

Extended Indexed Register SREG C7 : CRT FIFO Threshold Register

This is a read/write register. Port address is Hex 3C5.
Default value after hardware reset is Hex 00.

D0-3 CRT FIFO threshold high bit 0 to 2 (default = 0, point to actual value 4)
D4-7 CRT FIFO threshold low bit 0 to 2 (default = 0, point to actual value 3)

Bit 0-3 In the TP6508, memory cycle allocation is dynamic. When FIFO accumulated data is larger than FIFO threshold high value, CPU cycle can occur without any wait state.
Bit 4-7 When CPU access video memory, it must depend on remainder data of CRT FIFO . When the number of CRT FIFO data is less than the FIFO threshold low value, the only one thing can do is CRT access. Threshold value affects the performance of TP6508.

Extended Indexed Register SREG C8 : Attribute FIFO Threshold Register

This is a read/write register. Port address is Hex 3C5.
Default value after hardware reset is Hex 00.

D0-2 Attribute FIFO threshold bit 0 to 2 (default = 0, point to actual value 1)
D3-7 Reserved

Bit 0-2 This dynamic memory cycle allocation architecture is used in TP6508 . Specially, in text mode we integrate the Attribute FIFO storing attribute data in order to improve performance in text mode.
Bit 3-7 Reserved

Extended Indexed Register SREG C9 : MCLK Numerator Value Register

This is a read/write register. Port address is Hex 3C5.
Default value after hardware reset is Hex A1.

D0-6 MCLK numerator bit 0 to 6
D7 MCLK oscillation divider

Bit 0-6 This register,in conjunction with MCLK Denominator and Post Scalar Value Register, is used to determine the frequency of video clock. These 7 bits numerator (N), 7 bits denominator (D), and 1 bit post scalar (P) for clock (MCLK) determines its frequency according to the following expression:

$$MCLK(MHz) = \frac{OSC \times [N+1] \times [2P+2]}{[D+1]}, \quad OSC = 14.318\ (MHz)$$

Bit 7 This bit is used to divide the internal generated oscillation frequency. A logical 0 indicates to do it divided by two. A logical 1 indicates to do it divided by four . Normally, we set to logical 1 when MCLK outputs frequency lower 50MHz.

Extended Indexed Register SREG CA : MCLK Denominator and Post Scalar Value Register

This is a read/write register. Port address is Hex 3C5.
Default value after hardware reset is Hex 4D.

D0 MCLK post scalar
D1-7 MCLK denominator bit 0 to 6

Bit 0-7 This register,in conjunction with MCLK Numerator Value Register, is used to determine the frequency of memory clock.

Extended Indexed Register SREG CB: Clock Generator Test Register

This is a read/write register. Port address is Hex 3C5.
Default value after hardware reset is Hex 00.

D0-1 MCLK/VCLK signal output from OFF pin enable
D2-3 VCLK generated selection Select MCLK as VCLK source
D4 Enable pixel clock divide by two for TV display
D5 MCLK frequency synthesizer off enable
D6 VCLK frequency synthesizer off enable
D7 Oscillator off enable

Bit 0-1 These bits are used to select MCLK/VCLK signal output from OFF pin.

Bit 1	Bit 0	Output signal from OFF pin
0	0	Other signal
0	1	Internal MCLK signal
1	X	Internal VCLK signal

Bit 2-3 These bits are used to select VCLK clock source .

Bit 3	Bit 2	VCLK generated selection
0	0	From VCLK frequency synthesizer
0	1	MCLK synthesizer output dividing by 2 as the VCLK
1	0	VCLK synthesizer output dividing by 2 as the VCLK
1	1	From MCLK frequency synthesizer

Bit 4 A logical 1 forces TP6508 video clock frequency divide by two to generated the composite sync. signal for TV display .
Bit 5 A logical 1 forces TP6508 to power off MCLK frequency synthesizer.
Bit 6 A logical 1 forces TP6508 to power off VCLK frequency synthesizer.
Bit 7 A logical 1 forces TP6508 to power off Oscillator.

Extended Indexed Register SREG CC: MISC. Control Register

This is a read/write register. Port address is Hex 3C5.
Default value after hardware reset is Hex 00.

D0 DAC monitor senser off enable
D1 DAC off enable
D2 Synchronous reset timing generator
D3 VGA palette off enable
D4-5 Host bus memory access data bus select
D6 Emulation 16-bit access disable for 16 color display modes
D7 Bypass internal pallete enable

Bit 0 A logical 1 forces TP6508 to power off Monitor Sense logical block.
Bit 1 A logical 1 forces TP6508 to power off DAC block and disable CRT display refresh.
Bit 2 When logical 1 we can used this bit to reset TP6508 timing generator and synchronize the internal state machine.
Bit 3 A logical 1 forces TP6508 VGA palette power off.
Bit 4-5 These bits are used to set the host bus memory access data width.

Bit 5	Bit 4	Data width
0	0	8-bit
0	1	16-bit
1	0	32-bit
1	1	32-bit or 16-bit

Bit 6 This bit is used to set the host-to-display memory bus width on 16 color modes. A logical 1 enables TP6508 to expand to 16-bit data bus access. A logical 0 forces TP6508 to access in 8-bit data bus.

Bit 7 A logical 1 forces the pixel data bypass the internal palette and transfer through a special logical block to do as internal palette. In high speed video clock mode , the lookup internal palette operation is critical .

Extended Indexed Register SREG CD: Display Memory Register

This is a read/write register.
Port address is Hex 3C5.
Default value after hardware reset is Hex 00.

D0-1 Display memory configuration
D2 Asymmetical/symmetical address select for DRAM-A & B
D3 Dual-Write/Dual-Cas select for DRAM-A & B
D4 Asymmetical/symmetical address select for DRAM-C
D5 Dual-Write/Dual-Cas select for DRAM-C
D6 Enable 2M-byte display memory size
D7 Reserved

Bit 0-1 These bit are used to configure the DRAMs interface.

Bit 1	Bit 0	Display Memory Bus Width & Configuration
0	0	32-bit, Enable DRAM-A & DRAM-B interface
0	1	16-bit, Enable DRAM-A only
1	0	32-bit, Enable DRAM-A & DRAM-C interface *
1	1	Reserved

(*: DRAM-C isn't used as an external frame buffer with this setting, but does as display memory.)

Bit 2 A logical 0 indicates TP6508 to support symmetical DRAM memory addressing for DRAM-A & B. A logical 1 indicates TP6508 to support asymmetical DRAM memory addressing.

Bit 3 A logical 0 indicates TP6508 to support dual-CAS DRAM memory addressing for DRAM-A & B. A logical 1 indicates TP6508 to support dual-WRITE DRAM memory addressing.

Bit 4 A logical 0 indicates TP6508 to support symmetical DRAM memory addressing for DRAM-C. A logical 1 indicates TP6508 to support asymmetical DRAM memory addressing.

Bit 5 A logical 0 indicates TP6508 to support dual-CAS DRAM memory addressing for DRAM-C. A logical 1 indicates TP6508 to support dual-WRITE DRAM memory addressing.

Bit 6 A logical 1 enables TP6508 is operated on 2M-byte size memory configuration . Under the condition , TP6508 will adjust some of the counter length of the CRTC and size again the domain of display memory address.

Bit 7 Reserved.

Extended Indexed Register SREG CE: Configuration Register 1

This is a read only register. Port address is Hex 3C5.
Default value after hardware reset is Hex FF. (Chip internal pull high during power on reset)

D0 Enable BIOS ROMCS* signal output from OFF pin
D1 Enable 64k VGA BIOS decoding
D2 Relocation VGA BIOS address

D3 Enable IO 16 bit access
D4 VGA subsystem enable port address set to Hex46E8(default 3C3)
D5 Select VGA subsystem power-on in enable state
D6 Enable ISA bus width 8 bit
D7 Select SA address decoder
(These bits are latched from MAD0 to MAD7 at power on reset.)

Bit 0 When bus interface was selected VESA/CPU direct local bus connection , then this can set to logical 1 to enable BIOS ROMCS* signal output from OFF/EPROM* pin(pin 178).

Bit 1 We can set this bit to logical 0 to enable TP6508 BIOS decoding to expansion to 64 kb address domain.

Bit 2 When previous bit was set to logical 1, then this bit can be setting to relocate VGA BIOS decoding address.

Bit 2	Decoding address
0	Hex E0000 to EFFFF
1	Hex C0000 to CFFFF

Bit 3 A logical 0 enables TP6508 IO 16 bit access.

Bit 4 This bit selects the address of the video subsystem enable bit location. A logical 0 indicates the address of the video subsystem bit is Hex 46E8 , a logical 1 indicates that it is located on the address Hex 3C3.

Bit 5 A logical 0 indicates TP6508 power-on in the enable state that allows memory and IO accessing . A logical 1 indicates TP6508 in the disable state at power-on.

Bit 6 A logical 0 forces TP6508 connects to 8 bit width host bus . A logical 1 forces TP6508 connects to 16 bit width host bus.

Bit 7 A logical 1 indicates TP6508 use ALE signal to latch LA address signal . A logical 0 indicates TP6508 directs to decode SA address by bus command signals (MEMW*,MEMR*,IOW*,IOR*) .

Extended Indexed Register SREG CF: Configuration Register 2

This is a read only register. Port address is Hex 3C5.
Default value after hardware reset is Hex FF. (Chip internal pull high during power on reset)

D0-2 TP6508 into Test mode selection bit (Latched from MD 4 to 5)
D3 Reserved
D4-7 Display type selection bits
(These bits are latched from MAD8 to MAD15 at power on reset.)

Bit 0-2 These bit is used to enable TP6508 into test mode for the internal analog device blocks, including of the dual frequency synthesizer and RAMDAC . We can directly access the internal analog device blocks by TP6508's I/O pins.

Bit 2	Bit 1	Bit 0	Test device
1	1	0	MCLK analog device function test mode
1	0	1	VCLK analog device function test mode
0	1	1	DAC analog device function test mode

Bit 3 Reserved.

Bit 4-7 These bits are used to read back for VGA BIOS setting display type .

Bit-7	Bit-6	Bit-5	Bit-4	Display Type
0	0	0	0	NTSC TV
0	0	0	1	LCD/NTSC TV
0	0	1	0	800x600 color TFT
0	0	1	1	800x600 color DSTN
0	1	0	0	CRT-like TFT
0	1	0	1	Dual-scan STN LCD
0	1	1	0	800x600 color TFT

0	1	1	1	800x600 color DSTN
1	0	0	0	CRT/PLASMA
1	0	0	1	CRT/EL
1	0	1	0	CRT/Line-clock TFT
1	0	1	1	CRT/CRT-like TFT
1	1	0	0	CRT/Single-scan STN LCD
1	1	0	1	CRT/Dual-scan STN LCD
1	1	1	0	CRT/Mono LCD
1	1	1	1	CRT

Extended Indexed Register SREG D0: Configuration Register 3

This is a read only register. Port address is Hex 3C5.
Default value after hardware reset is Hex FF.

D0-2 Host bus selection bit 0 to 2 (Latched from AA0 to AA2)
D3 Disable A24 pin input data latch (Latched from AA3)
D4 Disable internal dual frequency synthesizer (Latched from AA4)
D5 Reserved (Latched from AA5)
D6 Reserved=1 (Latched from AA6)
D7 Disable PCI bus command asserted on configuration registers accessing (Latched (Latched from AA7)

Bit 0-2 In addition to an ISA bus connection, TP6508 can be connected directly to VESA local bus , PCI local bus or 486DX/DX2 local bus to provide additional graphics performance.

Bit 2	Bit 1	Bit 0	Host bus selection
0	0	0	Reserved
0	0	1	Reserved
0	1	0	Reserved
0	1	1	Reserved
1	0	0	Reserved
1	0	1	ISA bus
1	1	0	32-bit PCI Local Bus
1	1	1	Reserved

Bit 3 A logical 1 enables TP6508 to decode A24 pin input for linear address . This configuration bit must set to 1 for VESA/CPU local bus .

Bit 4 A logical 0 forces TP6508's internal dual frequency synthesizer not in operation. That make TP6508 to select the multiple pin OFF and XTALI as VCLK and MCLK pin . The source of video clock and memory clock are come from external component by VCLK and MCLK pin .

Bit 5 Reserved.

Bit 6 Reserved.

Bit 7 We can set this bit to logical 0 to force TP6508 not to assert a VGA access cycle on PCI local bus interface under the configuration read or write command being happend..

Extended Indexed Register SREG D1: GEC. Test Register

This is a read/write register. Port address is Hex 3C5.
Default value after hardware reset is Hex 00.

D0-7 Reserved

Bit 0-7 Reserved.

Extended Indexed Register SREG D2: Power Management Control Register

This is a read/write register. Port address is Hex 3C5.
Default value after hardware reset is Hex 00.

D0	Reserved
D1	Select OFF pin as input pin
D2	Select OFF pin control as active high control signal
D3	Select standby timer as suspend timer
D4	Force into standby mode
D5	Force into suspend mode
D6	Force into off mode
D7	Select Cover-Close mode (CRT display only this bit must =1)

Bit 0 Reserved.
Bit 1 A logical 1 select OFF pin as input pin, and a logical 0 select it as output pin.
Bit 2 A logical 0 select OFF pin signal polarity as active low, and a logical 1 select OFF pin signal polarity as active high.
Bit 3 A logical 1 select standby timer as suspend timer, then we can program this timer to change state from active mode to suspend mode and not to standby mode. A logical 0 we can program this timer to change state from active mode to standby mode.
Bit 4 User can to change state from active mode to standby mode by software programming this bit to logical 1.
Bit 5 User can to change state to suspend mode by software programming this bit to logical 1.
Bit 6 User can to change state to off mode by software programming this bit to logical 1.
Bit 7 A logical 1 select into Cover-close mode. Cover-close mode is the special power mode using for laptop PC or notebook pc system on closing the machine-cover . Specially, this mode replace off mode when the user programmed this bit to logical 1 . In cover-close mode, system will turn off panel backlight, and down saving internal partial panel block device power. Then the CRT display is normal.

Extended Indexed Register SREG D3: Backlight and Standby Timer Register

This is a read/write register. Port address is Hex 3C5.
Default value after hardware reset is Hex 00.

D0-3	Timer for backlight control bit 0 to 3 (Unit : 1 minute error -1/16 minute)
D4-7	Timer for standby/suspend control bit 0 to 3 (Unit : 2 minute error -1/8 minute) (User can use the value of 00 to disable the timer for power management .)

Bit 0-3 These bits are used to program the time that panel's backlight turn off after active mode into standby mode . The timer clock base is 14.318MHz for internal C.G. or external OSC. pin clock input divided by 4 .
Bit 4-7 These bits are used to program the time that active mode go into standby/suspend mode after the system was in the rest state.

Extended Indexed Register SREG D4 : Activity Monitoring Register

This is a read/write register. Port address is Hex 3C5.
Default value after hardware reset is Hex 00.

D0	Enable VGA access to reset backlight timer
D1	Enable Keyboard activity to reset backlight timer
D2-3	Reserved
D4	Enable VGA access to reset standby/off timer

D5 Enable Keyboard activity to reset standby/off timer
D6-7 Reserved

Bit 0 A logical 1 enables TP6508 to reset backlight timer for flat panel by VGA access.
Bit 1 A logical 1 enables TP6508 to reset backlight timer for flat panel by keyboard activity.
Bit 2-3 Reserved
Bit 4 A logical 1 enables TP6508 to reset standby timer for flat panel by VGA access.
Bit 5 A logical 1 enables TP6508 to reset standby timer for flat panel by keyboard activity.
Bit 6-7 Reserved

Extended Indexed Register SREG D5 : OFF Timer and Slow Refresh Register

This is a read only register. Port address is Hex 3C5.
Default value after hardware reset is Hex 00.

D0-3 Timer for off control bit 0 to 3 (Unit : 4 minute error -1/4 minute)
D4 Enable slow refresh in off mode
D5-6 Slow refresh rate selection bit 0 to 1
D7 Select external 32kHz clock as power management clock base

Bit 0-3 These bits are used to program the time that active mode go into off mode after the system was in the rest state.
Bit 4 A logical 1 enables TP6508 to slow down the refresh rate that specifies by next two bits in the off mode.
Bit 5-6 When TP6508 goes into off mode , it provide programmable refresh rate for power saving .

Bit 6	Bit 5	Refresh rate (KHz)
0	0	No refresh
0	1	32
1	0	16
1	1	8

Bit 7 User can use this bit to select the power management clock source. A logical 0 TP6508 selects the internal refresh clock base being divided the frequency of 14.318MHz clock source . And a logical 1 TP6508 switches the clock source to external 32KHz clock input.

Extended Indexed Register SREG D6 : Override and Status control Register

This is a read/write register. Port address is Hex 3C5.
Default value after hardware reset is Hex 00.

D0 FPBACK output override
D1 FPBACK polarity
D2 FPVCC/FPSIG/FPVEE output override
D3 FPVCC status
D4 FPSIG output status
D5 FPVEE output status
D6 Panel control state machine test mode enable
D7 FPVEE Pin(pin 61) output control

Bit 0 A logical 1 indicates TP6508 would override FPBACK standby mode.
Bit 1 If previous bit =1, then programming this bit would set the output state of FPBACK. If previous bit =0, then bit is used to invert the FPBACK output polarity.
Bit 2 A logical 1 indicates TP6508 would override FPVCC standby mode .

Bit 3 If previous bit =1 , then programming this bit would set the output state of FPVCC.

Bit 4 If bit2 =1 , then programming this bit would set the output state of panel control signal (FPVDCLK,MOD,LFS,LLCLK,DE*) and panel data bus. A logical 0 forces TP6508 set these output to logical 0 . A logical 1 indicates these signals output normal .

Bit 5 If bit2 =1 , then programming this bit would set the output state of FPVEE.

Bit 6 The bit is used to enable the panel control state machine into test mode (short the power sequency cycle time) . It is to be enable for internal test only.

Bit 7 A logical 0 enables TP6508 output FPVEE signal from Pin 61. A logical 1 enables TP6508 output FPBACK signal from Pin 61.

Extended Indexed Register SREG D7 : Memory mapping I/O Offset Low Register

This is a read/write register. Port address is Hex 3C5.
Default value after hardware reset is Hex 00.

D0-7 Graphics engine memory mapping I/O command offset bit 0 to 7

Bit 0-7 When memory map I/O was enabled (SREG bit-3=1), these bits would use to do as the segment address of I/O command for replacing the address A16 to A23. We can set these bits to relocate the I/O port address of Graphics Engine registers. By memory map I/O addressing, these registers are accessed as memory command and located at memory address binary ZZZZ,ZZZZ,ZZZZ,xxxx,xxYY,YYYY,YY00. The address value - 'Z..' is determined by this register and SREG D8. The low address value - 'Y..' is determined by SREG F0. The address value - 'x..' is determined by the Graphics Engine control register indexed value. Then TP6508 can access these registers with 16-bit data width by decoding at them, being conjunction with 'Y..' and 'x..' , directly.

Extended Indexed Register SREG D8 : Memory mapping I/O Offset High Register

This is a read/write register. Port address is Hex 3C5.
Default value after hardware reset is Hex 00.

D0-3 Graphics engine memory mapping I/O command offset bit 8 to 11
D4-7 Reserved

Bit 0-7 When memory map I/O was enabled, these bits would use to do as the segment address of I/O command for replacing the address A24 to A27.

Extended Indexed Register SREG D9 : PC Video Control Register

This is a read/write register. Port address is Hex 3C5.
Default value after hardware reset is Hex 00.

D0 Enable PC Video interface
D1 Select PC Video width
D2 Enable PC Video color key
D3-7 Reserved

Bit 0 A logical 1 enables PC video interface on DRAM-C pins that includes of RASC* ,CASCH* ,CASCL* ,WEC* , MCD[15:0]. A logical 0 disables it.

Bit 1 When previous bit is set to logical 1, this bit is used to select the PC video interface width. A logical 0 forces TP6508 inplements a 18-bit width PC video interface. A logical 1 enables TP6508 inplements a 24-bit width PC video interface and sets OEC*,AA9,FPBACK,ACTI as video input. When this bit is set to logical 1, a 24-bit panel interface is also avilable by CA[7:0] being becomed P[23:16]. Specially, this bit shouldn't be set to 1 if the SREG D0 bit-6 is set to 1.

Bit 2 If the previous bit-0 is set to logical 1 , then this bit is used to select the color key type for PC video Overlay . A logical 1 forces TP6508 use external color key signals and enables PC video Overlay on color key. A logical uses the following color compare registers to generate the color key .

Bit 3-7 Reserved.

Extended Indexed Register SREG DA : Color Key Compare Register 0

This is a read/write register. Port address is Hex 3C5.
Default value after hardware reset is Hex 00.

D0-7 Color compare data bit 0 to 7

Bit 0-7 These bits are compared to bit 0 to 7 of background video stream. They are in conjunction with color compare bit 8 to 15 and color compare bit 16 to 23 to compare with color key data. When all the enabled bits that are set by mask regs. SREG DB/DC/DD matches the relation color key data bits and the key is enabled, external video sent to the screen.

Extended Indexed Register SREG DB : Color Key Compare Register 1

This is a read/write register. Port address is Hex 3C5.
Default value after hardware reset is Hex 00.

D0-7 Color compare data bit 8 to 15

Bit 0-7 These bits are compared to bit 8 to 15 of background video stream. They are in conjunction with color compare bit 0 to 7 and color compare bit 16 to 23 to compare with color key data. When all the enabled bits that are set by mask regs. SREG DB/DC/DD matches the relation color key data bits and the key is enabled, external video sent to the screen.

Extended Indexed Register SREG DC : Color Key Compare Register 2

This is a read/write register. Port address is Hex 3C5.
Default value after hardware reset is Hex 00.

D0-7 Color compare data bit 16 to 23

Bit 0-7 These bits are compared to bit 16 to 23 of background video stream. They are in conjunction with color compare bit 0 to 7 and color compare bit 8 to 15 to compare with color key data . When all the enabled bits that are set by mask regs. SREG DB/DC/DD matches the relation color key data bits and the key is enabled, external video sent to the screen.

Extended Indexed Register SREG DD : Color Key Mask Register 0

This is a read/write register. Port address is Hex 3C5.
Default value after hardware reset is Hex 00.

D0-7 Color compare mask bit 0 to 7

Bit 0-7 These bits are used to select which bits of the background video data stream are used in the comparsion with the color compare data bit 0 to 23. This register control bits 0 to 7. The mask data bits format are as follow:

0: Data does particpate in compare operation
1: Data mask in compare operation

Extended Indexed Register SREG DE : Color Key Mask Register 1

This is a read/write register. Port address is Hex 3C5.
Default value after hardware reset is Hex 00.

D0-7 Color compare mask bit 8 to 15

Bit 0-7 These bits are used to select which bits of the background video data stream are used in the comparsion with the color compare data bit 0 to 23. This register control bits 8 to 15.

Extended Indexed Register SREG DF : Color Key Mask Register 2

This is a read/write register. Port address is Hex 3C5.
Default value after hardware reset is Hex 00.

D0-7 Color compare mask bit 16 to 23

Bit 0-7 These bits are used to select which bits of the background video data stream are used in the comparsion with the color compare data bit 0 to 23. This register control bits 16 to 23.

Extended Indexed Register SREG F0 : Graphics Engine Port Address Low Register

This is a read only register. Port address is Hex 3C5.
Default value after hardware reset is Hex F1.

D0-7 Graphics engine port address bit 2 to 9

Bit 0-7 TP6508 Graphics Engine control registers are accessed at Port binary address xxxx,xxYY,YYYY,YY00. These bits are used to determine the low address value - 'Y..' and they are set default hex. F1. The high address value - 'x..' is determined by Graphics Engine control registers indexed value. For example, as default value hex. F1, BITBLT Source X Offset Reg. port address at hex. 07C4.

Extended Indexed Register SREG F1 : Linear Addressing Register

This is a read/write register. Port address is Hex 3C5.
Default value after hardware reset is Hex 00.

D0-7 Base address bit 0 to 7

Bit 0-7 When SREG C0 bit-2 was set to logical 1 , then these bits would use to do as LA20 to LA27. IBM compatible display address uses low base 1M address bit 0 to 19 and locates at Hex A0000 to AFFFF or Hex B0000 to BFFFF. We can set these bits to relocate display address at upper high 255M memory address.

Extended CRTC Register Description

The following registers are TP6508 extended CRTC registers. These registers are accessed by first writing the index of the desired register to the Sequencer Index register, i.e. address Hex 3D4 and then accessing the register using the address Hex 3D5. These registers are protected by password/ Identification register (Extended Sequencer Indexed Register Hex 05) .

Extended Indexed Register CREG 20 : Extended memory address offset Register

This is a read/write register. Port address is Hex 3D5.
Default value after hardware reset is Hex 00.

D0-7 Extended memory address offset bit 0 to 7

Bit 0-7 In TP6508 interlace display design , you can use this register to program the memory address offset value as the memory length of one scan line to next scan line during odd or even filed for interlace display mode . The bit 8 are in the bit 4 of Extended register CREG 21.

Extended Indexed Register CREG 21 : Memory address offset High Register

This is a read/write register. Port address is Hex 3D5.
Default value after hardware reset is Hex 00.

D0 Extended memory address offset bit 8
D1-3 Reserved
D4-5 IBM Memory address offset bit 8,9
D6-7 Reserved

Bit 0 Extended memory address offset bit 8.
Bit 1-3 Reserved.
Bit 4-5 Memory address offset bit 8 to 9.
Bit 6-7 Reserved.

Extended Indexed Register CREG 22 : Start Address High Register

This is a read/write register. Port address is Hex 3D5.
Default value after hardware reset is Hex 00.

D0-3 Start address bit 16 to 19
D4-7 Cursor address bit 16 to 19

Bit 0-3 The most significant bit 16 and bit 19 of the start address register.
Bit 4-7 The most significant bit 16 and bit 19 of the cursor address register.

Extended Indexed Register CREG 23 : Reserved

This is a read/write register. Port address is Hex 3D5.
Default value after hardware reset is Hex 00.

D0-7 Reserved

Bit 0-7 Reserved.

Extended Indexed Register CREG 24 : CRT Vertical High Register

This is a read/write register. Port address is Hex 3D5.
Default value after hardware reset is Hex 00.

D0	Vertical total bit 10
D1	Vertical display enable end bit 10
D2	Vertical blank star bit 10
D3	Vertical retrace start bit 10
D4	Line compare bit 10
D5-7	Reserved

Bit 0 Bit 10 of the vertical total register.
Bit 1 Bit 10 of the vertical display enable register.
Bit 2 Bit 10 of the vertical blank start register.
Bit 3 Bit 10 of the vertical retrace start register.
Bit 4 Bit 10 of the line compare register.
Bit 5-7 Reserved.

Extended Indexed Register CREG 25 : Half Horizontal Retrace Start Register

This is a read/write register. Port address is Hex 3D5.
Default value after hardware reset is Hex 00.

D0-7	Half horizontal retrace start bit 0 to 7

Bit 0-7 In interlace display mode , TP6508 need a count point that point at half of a scan-line to generate the interlace display timing sequence . And these bits are nice to program doing it , a real interlace display .

Extended Indexed Register CREG 26 : TV Leading Horizontal Retrace Start Register

This is a read/write register. Port address is Hex 3D5.
Default value after hardware reset is Hex 00.

D0-7	TV leading horizontal retrace start bit 0 to 7

Bit 0-7 By TV display, it was designed to base on the interlace scan technique, TP6508 need two retrace signal(like VGA retrace signal) on even field and odd field. TV composite sync. signal waveform include two equalizing pulse interval, front and back the vertical sync. interval, those have three pulse individually. We need to define the intervals position in the TV composite sync. waveform. So we can use these bits to program the front equalizing pulse(front of horizontal sync. pulse interval) start position. on even field and make it be able using in TV display mode.

Extended Indexed Register CREG 27 : TV Horizontal Retrace End for Equalizing Pulse Register

This is a read/write register. Port address is Hex 3D5.
Default value after hardware reset is Hex 00.

D0-3	TV horizontal retrace end bit 0 to 3
D4-7	Reserved

Bit 0-3 These bits is used to program the back equalizing pulse(back of horizontal sync. pulse interval) start position. on even field and make it be able using in TV display mode.

Bit 4-7 Reserved .

Extended Indexed Register CREG 28 : TV Leading Half Horizontal Retrace Start Register

This is a read/write register. Port address is Hex 3D5.
Default value after hardware reset is Hex 00.

D0-3 TV leading half horizontal retrace start bit 0 to 3
D4-7 Reserved

Bit 0-3 By TV display, it was designed to base on the interlace scan technique, TP6508 need two retrace signal(like VGA retrace signal) on even field and odd field. TV composite sync. signal waveform include two equalizing pulse interval, front and back the vertical sync. interval, those have three pulse individually. We need to define the intervals position in the TV composite sync. waveform. So we can use these bits to program the front equalizing pulse(front of horizontal sync. pulse interval) start position. on even field and make it be able using in TV display mode.

Bit 4-7 Reserved .

Extended Indexed Register CREG 29 : TV Half Horizontal Retrace End for Equalizing Pulse Register

This is a read/write register. Port address is Hex 3D5.
Default value after hardware reset is Hex 00.

D0-3 TV leading half horizontal retrace end bit 0 to 3
D4-7 Reserved

Bit 0-3 These bits is used to program the back equalizing pulse(back of horizontal sync. pulse interval) start position. on odd field and make it be able using in TV display mode.

Bit 4-7 Reserved .

Panel Control Register Description

The following registers are TP6508 Panel Control registers. These registers are accessed by first writing the index of the desired register to the Sequencer Index register, i.e. address Hex 3D4 and then accessing the register using the address Hex 3D5. These registers are protected by password/ Identification register (Extended Index Register Hex 05) .

Extended Indexed Register CREG A0 : Panel Miscellaneous Control Register 1

This is a read/write register.
Port address is Hex 3D5.
Default value after hardware reset is Hex 00.

D0-2	Flat panel type 0 to 2
D3	Invert LP/PHSYNC control
D4	Invert FLM/PVSYNC control
D5	invert FPVDCLK/PSCLK
D6	Free run LLCLK
D7	Invert DEN control

Bit 0-2 These three bits select the type of Flat panel connected.

Bit 2	Bit 1	Bit 0	Panel type
0	0	0	Dual-Scan/Dual-data Monochrome LCD panels
0	0	1	Gray scale PLASMA panels
0	1	0	Single-Scan STN color LCD panels
0	1	1	TFT color LCD panels
1	0	0	Reserved
1	0	1	Gray scale EL panels
1	1	0	Dual-Scan STN color LCD panels
1	1	1	Reserved

Bit 3 A logical 1 would invert the LLCLK signal (normally active high).
Bit 4 A logical 1 would invert the LFS signal (normally active high).
Bit 5 A logical 1 would invert the FPVDCLK signal (normally active high).
Bit 6 The last line of every frame may display longer and brighter than other lines. When this bit is a logical 1 , it forces TP6508 to generate a free-running LLCLK and eliminates the brighter line during CRT blanking cycle.
Bit 7 A logical 1 would invert the DEN signal (normally active high) for PLASMA or TFT panel display mode .

Extended Indexed Register CREG A1 : Panel Miscellaneous Control Register 2

This is a read/write register.
Port address is Hex 3D5.
Default value after hardware reset is Hex 00.

D0	Select 8 bits color STN interface
D1	Select enhance color STN timing
D2	Select CRT-like LP and FLM for TFT LCD panel
D3	Disable CRT display
D4	Enable Flat panel interface
D5	Select 8 bit PLASMA panel interface

D6 Select gray conversion type for mono flat panel display
D7 Enable TV display

Bit 0 A logical 1 TP6508 selects 8 bits color STN interface
Bit 1 A logical 1 TP6508 switches the panel display timing to enhance color STN timing.
Bit 2 A logical 1 TP6508 selects CRT-like LP(Hsync) and FLM(Vsync) for TFT LCD panel.
Bit 3 A logical 1 disables the CRT display , and a logical 0 enables it.
Bit 4 A logical 1 enables the flat panel display, and a logical 0 disables the flat panel display.
Bit 5 A logical 1 TP6508 selects 8 bits PLASMA interface . And a logical 0 TP6508 selects 4 bits PLASMA interface.
Bit 6 This bit is use to set the gray conversion type for mono flat panel display . A logical 1 enable it , a logical 0 disable it.
Bit 7 A logical 1 enables the TV display and we can output composite SYNC signal to HSYNC pin.

Extended Indexed Register CREG A2 : Panel Miscellaneous Control Register 3

This is a read/write register.
Port address is Hex 3D5.
Default value after hardware reset is Hex 00.

D0 Reverse panel video output for text mode
D1 Reverse panel video output for graphic mode
D2-3 Blinking rate selection bit 0 to 1
D4 Select maximum contrast display for text mode
D5 Select attribute emulation display for text mode
D6 Select RGBI emulation display for 16 color graphic mode
D7 Enable full cursor display for text mode

Bit 0 A logical 1 reverses the pixel data that sends to the panel for text mode .
Bit 1 A logical 1 reverses the pixel data that sends to the panel for graphic mode .
Bit 2-3 LCD panel has low response time character, TP6508 provides flexible choice for blinking rate.

Bit 3	Bit 2	Blinking Rate
0	0	1/16
0	1	1/32
1	0	1/64
1	1	1/128

Bit 4 In panel text mode, when foreground RGB and background RGB mapping to the close gray level. It will produce ambiguous phenomenon. When this bit is a logical 1, TP6508 will compare foreground and background mapping gray level. If foreground gray level is larger than background gray level, TP6508 forces foreground to the maximum gray level , background to the minimum gray level . It will eliminate ambiguous situation. If the bit 6 of previous register set to logical 1 , then this bit is not valid .
Bit 5 When this bit is a logical 1, TP6508 provides 16 gray level without passing through gray palette for text mode . In this mode, Red, Green, Blue, and Intensity , four bits can make 16 gray level without losing color, mono mapping relation .
Bit 6 When this bit is a logical 1, TP6508 provides 16 gray level without passing through gray palette for 16 color graphic mode.
Bit 7 On LCD panel, a narrow cursor may difficult to observe. A logical 1 forces a full display cursor for easy find out and ignores the cursor sharp setting.

Extended Indexed Register CREG A3 : Panel Miscellaneous Control Register 4

This is a read/write register.
Port address is Hex 3D5.
Default value after hardware reset is Hex 00.

D0	Enable vertical expansion for text mode
D1	Enable vertical expansion for graphic mode
D2	Force 8 dots character clock
D3	Enable shadow frame buffer with internal Line buffer for Mono Dual-scan STN LCD
D4	Enable shadow frame buffer with internal Line buffer for Color Dual-scan STN LCD
D5	Enable external frame buffer for Color Dual-scan STN LCD
D6	Enable extra LLCLK 244
D7	Enable extra LLCLK 242

Bit 0 A logical 1 forces TP6508 to fit the panel vertical resolution for text mode.

Bit 1 A logical 1 forces TP6508 to fit the panel vertical resolution for graphic mode.

Bit 2 In panel mode , LCD and PLASMA manufactures produce 640x480 pixel panel . Some IBM standard modes define 9 dots per character , all characters cannot display 80 columns (720 dots) at the same time . When this bit is a logical 1, TP6508 force character width to be 8 dots.

Bit 3 In monochrome dual-scan STN LCD display,logical 1 enables shadow frame accelerate operation. At this time, TP6508 can gain better display quality and up to 64 gray level. Other flat panel display modes this bit is invaild .

Bit 4 In color dual-scan STN LCD display,logical 1 enables shadow frame accelerate operation. At this time, TP6508 can gain better display quality and up to 64k color level . Other flat panel display modes this bit is invaild .

Bit 5 In color dual-scan STN LCD display, logical 1 enables external frame accelerate operation to gain better display quality. At this time an extra DRAM(s) is necessary . A logical 0 disables the external frame buffer and TP6508 uses the Pseudo Frame Buffer technique to implement the display mode . Other display mode this bit is invaild .

Bit 6 A logical 1 enables one extra LLCLK for LCD monochrome panels that require 244 line clocks for the upper panel.

Bit 7 A logical 1 enables one extra LLCLK for LCD monochrome panels that require 242 line clocks for the upper panel.

Extended Indexed Register CREG A4 : LCD AC Modulation Period Register

This is a read/write register. Port address is Hex 3D5.
Default value after hardware reset is Hex 00.

D0-7	LCD AC modulation bit 0 to 7

Bit 0-7 AC modulation LCD panel cannot be driven in the DC level. Some LCD panel modules do not provide AC modulation signal, TP6508 offers this function to prevent LCD damage. These bits define the number of LP(Hsync) between adjacent phase changes on MOD output. As these bits are programmed to hex 00, then the MOD signal phase changes every frame.

Extended Indexed Register CREG A5 : Panel Miscellaneous Control Register 5

This is a read/write register. Port address is Hex 3D5.
Default value after hardware reset is Hex 00.

D0	Panel resolution selection

D1 Select 600-line Extended CRT vertical group registers
D2 Enable horizontal expansion for text mode
D3 Enable horizontal expansion for graphic mode
D4 Enable TV equalizing pulse
D5-7 Reserved

Bit 0 This bit is used to select the flat panel resolution .(for vertical expansion and horizontal centering)
0 : 640x flat panel size
1 : 800x flat panel size

Bit 1 This bit is used to select the extended vertical timing set register group when the bit-1 of CREG AC(Enable extended vertical timing) was set to logical 1 and the bit-6,7 of MISCREG were set to 1,1. The more description is in CREG AC bit-1 description.
0 : Use the 480-line vertical timing CRT regs. CREG B6-BC
1 : Use the 600-line vertical timing CRT regs. CREG C7-CD

Bit 2 A logical 1 forces TP6508 to fit the panel horizontal resolution for text mode.

Bit 3 A logical 1 forces TP6508 to fit the panel horizontal resolution for graphic mode.

Bit 4 This bit is used to select the TV composit signal generated type.
0 : No equalizing pulse, it only composits horizontal and vertical sync.
1 : Insert equalizing pulse

Bit 5-7 Reserved.

Extended Indexed Register CREG A6 : Reserved

This is a read/write register. Port address is Hex 3D5.
Default value after hardware reset is Hex 00.

D0-7 Reserved

Extended Indexed Register CREG A7:Reserved

This is a read/write register.
Port address is Hex 3D5.
Default value after hardware reset is Hex 00.

D0-7 Reserved

Extended Indexed Register CREG A8 : X Offset Control Register

This is a read/write register. Port address is Hex 3D5.
Default value after hardware reset is Hex 00.

D0-4 LCD panel gray modulation X offset bit 0 to 4
D5-6 TFT LCD panel amplitude modulation bit 0 to 1
D7 Reserved

Bit 0-4 TP6508 has a special function to eliminate stippling wave . You can program X-directional offset values for best looking.

Bit 5-6 User can use the amplitude modulation to smooth and get to colorfully by these two bits.

Bit 6	Bit 5	Description
0	0	Disable amplitude modulation
0	1	Select two bits and Ground signal modulation (data bit 1 to 0)
1	0	Select three bits modulation (data bit 2 to 0)
1	1	Select three bits modulation (data bit 3 to 1)

Bit 7 Reserved

Extended Indexed Register CREG A9 : Y Offset Control Register

This is a read/write register. Port address is Hex 3D5.
Default value after hardware reset is Hex 00.

D0-4 LCD panel gray modulation Y offset bit 0 to 4
D5-6 Flat panel dithering type bit 0 to 1
D7 Dither algorithm selection

Bit 0-4 TP6508 has a special function to eliminate stippling wave . You can program Y-directional offset values for best looking.

Bit 5-6 User can select the dithering type to smooth and get to colorfully by these two bits.

Bit 6	Bit 5	Description
0	0	Disable dithering function
0	1	Select two bits dithering (data bit 1 to 0)
1	0	Select two bits dithering (data bit 2 to 1)
1	1	Select two bits dithering (data bit 3 to 2)

Bit 7 This bit is used to select the dither algorithm method. A logical 0 select the color modulation bit to be the next bit of the two selected dithering bits in bit 5-6 of this register. A logical 1 select the color modulation bit to be the LSB of the color data.

Extended Indexed Register CREG AA : Frame Buffer Start Address High register

This is a read/write register. Port address is Hex 3D5.
Default value after hardware reset is Hex 00.

D0-3 Frame buffer start address bit 0 to 3
D4 Reserved
D5 M Pin selection
D6 LP Pin selection
D7 Reserved

Bit 0-3 With integrated frame accelerator technology . TP6508 can use the video memory space as internal frame buffer to replace the external frame buffer . These bits is programming to set the internal frame buffer starting address of video memory. They replace and do as memory address MA14 to MA17.

Bit 4 Reserved.

Bit 5 This bit is used to select the M Pin(pin 69) output function.

Bit 5	Output function
0	M signal output
1	DE* signal output

Bit 6 This bit is used to select the LP Pin(pin 68) output function.

Bit 6	Output function
0	LP signal output
1	DE* signal output

Bit 7 Reserved.

Extended Indexed Register CREG AB : Line Buffer Terminal Count Register

This is a read/write register. Port address is Hex 3D5.
Default value after hardware reset is Hex 00.

D0-5 Line buffer terminal count bit 0 to 5 (Unit : 32 pixels)
D6-7 Reserved

Bit 0-5 TP6508 has a internal line buffer to store pixel-data of a line for dual flat panel device. Specially, the line buffer must work on the condition that TP6508 has turned on panel frame buffer and it do as a temp store of frame buffer. These bits can be programmed to set the line buffer length which base on flat panel horizontal resolution or do for simulation test only.

Bit 6-7 Reserved.

Extended Indexed Register CREG AC : Extended CRT Control Register

This is a read/write register. Port address is Hex 3D5.
Default value after hardware reset is Hex 00.

D0 Enable extended horizontal timing set
D1 Enable extended vertical timing set
D2 IBM CRT control registers lock
D3 Half panel timing source selection
D4 Text mode vertical expansion selection
D5 Enable 24-bit TFT panel interface
D6-7 Reserved

Bit 0 A logical 1 forces TP6508 using the extended CRT horizontal timing set registers to match or fit the flat panel resolution for LCD or LCD-CRT display mode. A logical 0 set TP6508 working on using the IBM CRT horizontal timing set registers.

Bit 1 A logical 0 set TP6508 working on using the IBM CRT vertical timing set registers . A logical 1 forces TP6508 using the extended CRT vertical timing set registers to match or fit the flat panel resolution for LCD or LCD-CRT display mode. Then, we can use the MISCREG bit 6,7 to select the extended vertical timing set register group. The more description is in CREG A5 bit-3 description.

MISCREG Bit-7,	Bit-6	Selected Vertical CRT register group
0	0	Reserved
0	1	Use the 400-line vertical timing CRT regs. CREG C7-CD
1	0	Use the 350-line vertical timing CRT regs. CREG C7-CD
1	1	Decided by CREG A5 bit-3

Bit 2 A logical 1 enables CRTC lock to protect the parameter of IBM CRT control register.

Bit 3 A logical 0 inducates TP6508 to generate the half panel timing by setting Ext. Reg. hex A5 for internal panel controller use . A logical 1 forces TP6508 use the half of VDE signal as it by programming the CRT Reg. hex 12.

Bit 4 A logical 0 selects to insert a line by counting every 3 or 5 lines for x350 or x400 resolution text mode to fit the vertical resolution of flat panel . A logical 1 selects to insert 5 or 3 line into every character for x350 or x400 resolution text mode to fit the vertical resolution of flat panel .

Bit 5 A logical 1 enables TP6508 to implement 24-bit panel interface for 18-bit or 24-bit TFT panel. A logical 0 forces TP6508 to implement 16-bit panel interface for 9/12/15/16-bit panel.

Bit 6-7 Reserved

Extended Indexed Register CREG AD : Extended CRT Horizontal Total Register

This is a read/write register. Port address is Hex 3D5.
Default value after hardware reset is Hex 00.

D0-7 Extended CRT horizontal total bit 0 to 7 (-5)

Extended Indexed Register CREG AE : Extended CRT Horizontal Display Enable End Register

This is a read/write register. Port address is Hex 3D5.
Default value after hardware reset is Hex 00.

D0-7 Extended CRT horizontal display enable end bit 0 to 7 (-1)

Extended Indexed Register CREG AF : Extended CRT Horizontal Blanking Start

This is a read/write register. Port address is Hex 3D5.
Default value after hardware reset is Hex 00.

D0-7 Extended CRT horizontal blanking start bit 0 to 7 (-1)

Extended Indexed Register CREG B0 : Extended CRT Horizontal Blanking End

This is a read/write register. Port address is Hex 3D5.
Default value after hardware reset is Hex 00.

D0-5 Extended CRT horizontal blanking end bit 0 to 5
D6-7 Reserved

Extended Indexed Register CREG B1 : Extended CRT Horizontal Retrace Start

This is a read/write register. Port address is Hex 3D5.
Default value after hardware reset is Hex 00.

D0-7 Extended CRT horizontal retrace start bit 0 to 7

Extended Indexed Register CREG B2 : Extended CRT Horizontal Retrace End

This is a read/write register. Port address is Hex 3D5.
Default value after hardware reset is Hex 00.

D0-4 Extended CRT horizontal retrace end bit 0 to 4
D5-7 Reserved

Extended Indexed Register CREG B3 : Reserved

This is a read/write register. Port address is Hex 3D5.
Default value after hardware reset is Hex 00.

D0-7 Reserved

Extended Indexed Register CREG B4 : Extended CRT Horizontal Retrace Start for TFT LCD panel

This is a read/write register. Port address is Hex 3D5.
Default value after hardware reset is Hex 00.

D0-7 Extended CRT horizontal retrace start bit 0 to 7 for TFT LCD panel

Extended Indexed Register CREG B5 : Extended CRT Horizontal Retrace End for TFT LCD panel

This is a read/write register. Port address is Hex 3D5.
Default value after hardware reset is Hex 00.

D0-4 Extended CRT horizontal retrace end bit 0 to 4 for TFT LCD panel
D5-7 Extended CRT horizontal retrace skew bit 0 to 2 for TFT LCD panel

Extended Indexed Register CREG B6 : 480-Line Extended CRT Vertical Total Register

This is a read/write register. Port address is Hex 3D5.
Default value after hardware reset is Hex 00.

D0-7 Extended CRT Extended CRT vertical total bit 0 to 7 (-2)

Extended Indexed Register CREG B7 : 480-Line Extended CRT Vertical Display Enable End Register

This is a read/write register. Port address is Hex 3D5.
Default value after hardware reset is Hex 00.

D0-7 Extended CRT Extended CRT vertical display enable end bit 0 to 7 (-1)

Extended Indexed Register CREG B8 : 480-Line Extended CRT Vertical Blank Start

This is a read/write register. Port address is Hex 3D5.
Default value after hardware reset is Hex 00.

D0-7 Extended CRT vertical blank start bit 0 to 7 (-1)

Extended Indexed Register CREG B9 : 480-Line Extended CRT Vertical Blank End

This is a read/write register. Port address is Hex 3D5.
Default value after hardware reset is Hex 00.

D0-7 Extended CRT vertical blank end bit 0 to 7

Extended Indexed Register CREG BA : 480-Line Extended CRT Vertical Retrace Start

This is a read/write register. Port address is Hex 3D5.
Default value after hardware reset is Hex 00.

D0-7 Extended CRT vertical retrace start bit 0 to 7

Extended Indexed Register CREG BB : 480-Line Extended CRT Vertical Retrace End

This is a read/write register. Port address is Hex 3D5.
Default value after hardware reset is Hex 00.

D0-3 Extended CRT vertical retrace end bit 0 to 3
D4-7 Reserved

Extended Indexed Register CREG BC : 480-Line Extended CRT Vertical Overflow

This is a read/write register. Port address is Hex 3D5.
Default value after hardware reset is Hex 00.

D0-1 Extended CRT vertical total bit 8 to 9
D2-3 Extended vertical display enable end bit 8 to 9 for vertical expansion mode
D4-5 Extended CRT vertical blank start bit 8 to 9
D6-7 Extended CRT vertical retrace start bit 8 to 9

Extended Indexed Register CREG C0 : Flat Panel 350 Scan line Mode Display Centering Control Register

This is a read/write register. Port address is Hex 3D5.
Default value after hardware reset is Hex 00.

D0-7 LCD panel 350 scan line mode screen shift bit 0 to 7

Bit 0-7 These bits are used to program the vertical screen shift length from the top or bottom of panel to actual display part on 350 scan line mode. And you can get through the screen display centering.

Extended Indexed Register CREG C1: Flat Panel 400 Scan line Mode Display Centering Control Register

This is a read/write register. Port address is Hex 3D5.
Default value after hardware reset is Hex 00.

D0-7 LCD panel 400 scan line mode screen shift bit 0 to 7

Bit 0-7 These bits are used to program the vertical screen shift length from the top or bottom of panel to actual display part on 400 scan line mode. And you can get through the screen display centering.

Extended Indexed Register CREG C2: Flat Panel 480 Scan line Mode Display Centering Control Register

This is a read/write register. Port address is Hex 3D5.
Default value after hardware reset is Hex 00.

D0-7 LCD panel 480 scan line mode screen shift bit 0 to 7

Bit 0-7 These bits are used to program the vertical screen shift length from the top or bottom of panel to actual display part on 480 scan line mode. And you can get through the screen display centering.

Extended Indexed Register CREGC3 : Half Panel Size Low Register

This is a read/write register. Port address is Hex 3D5.
Default value after hardware reset is Hex 00.

D0-7 Half panel size bit 0 to 7

Bit 0-7 These bits use to decide the half panel size (scan lines - 1) and make TP6508 generating accurate flat panel interface timing.

Extended Indexed Register CREG C4 : Half Panel Size High Register

This is a read/write register. Port address is Hex 3D5.
Default value after hardware reset is Hex 00.

D0 Half panel size bit 8
D1-7 Reserved

Bit 0 This bit is the high bit of half panel size register.
Bit 1-7 Reserved.

Extended Indexed Register CREG C5: Flat Panel Text Mode Display Horizontal Centering Control Register

This is a read/write register. Port address is Hex 3D5.
Default value after hardware reset is Hex 00.

D0-3 LCD panel horizontal screen shift bit 0 to 3 for text mode display (in character as unit)
D4-7 Reserved

Bit 0-3 These bits are used to program the horizontal screen shift length from the left or right of panel to actual display part. And you can get through the screen display centering .
Bit 4-7 Reserved.

Extended Indexed Register CREG C6: Flat Panel Graphics Mode Display Horizontal Centering Control Register

This is a read/write register. Port address is Hex 3D5.
Default value after hardware reset is Hex 00.

D0-3 LCD panel horizontal screen shift bit 0 to 3 for graphics mode display (in character as unit)
D4-7 Reserved

Bit 0-3 These bits are used to program the horizontal screen shift length from the left or right of panel to actual display part. And you can get through the screen display centering.
Bit 4-7 Reserved.

Extended Indexed Register CREG C7 : 600-Line Extended CRT Vertical Total Register

This is a read/write register. Port address is Hex 3D5.
Default value after hardware reset is Hex 00.

D0-7 Extended CRT Extended CRT vertical total bit 0 to 7 (-2)

Extended Indexed Register CREG C8 : 600-Line Extended CRT Vertical Display Enable End Register

This is a read/write register. Port address is Hex 3D5.
Default value after hardware reset is Hex 00.

D0-7 Extended CRT Extended CRT vertical display enable end bit 0 to 7 (-1)

Extended Indexed Register CREG C9 : 600-Line Extended CRT Vertical Blank Start

This is a read/write register. Port address is Hex 3D5.
Default value after hardware reset is Hex 00.

D0-7 Extended CRT vertical blank start bit 0 to 7 (-1)

Extended Indexed Register CREG CA : 600-Line Extended CRT Vertical Blank End

This is a read/write register. Port address is Hex 3D5.
Default value after hardware reset is Hex 00.

D0-7 Extended CRT vertical blank end bit 0 to 7

Extended Indexed Register CREG CB : 600-Line Extended CRT Vertical Retrace Start

This is a read/write register. Port address is Hex 3D5.
Default value after hardware reset is Hex 00.

D0-7 Extended CRT vertical retrace start bit 0 to 7

Extended Indexed Register CREG CC : 600-Line Extended CRT Vertical Retrace End

This is a read/write register. Port address is Hex 3D5.
Default value after hardware reset is Hex 00.

D0-3 Extended CRT vertical retrace end bit 0 to 3
D4-7 Reserved

Extended Indexed Register CREG CD : 600-Line Extended CRT Vertical Overflow

This is a read/write register. Port address is Hex 3D5.
Default value after hardware reset is Hex 00.

D0-1 Extended CRT vertical total bit 8 to 9
D2-3 Extended vertical display enable end bit 8 to 9 for vertical expansion mode
D4-5 Extended CRT vertical blank start bit 8 to 9
D6-7 Extended CRT vertical retrace start bit 8 to 9

Extended Indexed Register CREG F0 : 400-Line Extended CRT Vertical Total Register

This is a read/write register. Port address is Hex 3D5.
Default value after hardware reset is Hex 00.

D0-7 Extended CRT Extended CRT vertical total bit 0 to 7 (-2)

Extended Indexed Register CREG F1 : Reserved

This is a read/write register. Port address is Hex 3D5.
Default value after hardware reset is Hex 00.

D0-7 Reserved

Extended Indexed Register CREG F2 : 400-Line Extended CRT Vertical Blank Start

This is a read/write register. Port address is Hex 3D5.
Default value after hardware reset is Hex 00.

D0-7 Extended CRT vertical blank start bit 0 to 7 (-1)

Extended Indexed Register CREG F3 : 400-Line Extended CRT Vertical Blank End

This is a read/write register. Port address is Hex 3D5.
Default value after hardware reset is Hex 00.

D0-7 Extended CRT vertical blank end bit 0 to 7

Extended Indexed Register CREG F4 : 400-Line Extended CRT Vertical Retrace Start

This is a read/write register. Port address is Hex 3D5.
Default value after hardware reset is Hex 00.

D0-7 Extended CRT vertical retrace start bit 0 to 7

Extended Indexed Register CREG F5 : 400-Line Extended CRT Vertical Retrace End

This is a read/write register. Port address is Hex 3D5.
Default value after hardware reset is Hex 00.

D0-3 Extended CRT vertical retrace end bit 0 to 3
D4-7 Reserved

Extended Indexed Register CREG F6 : 400-Line Extended CRT Vertical Overflow

This is a read/write register. Port address is Hex 3D5.
Default value after hardware reset is Hex 00.

D0-1 Extended CRT vertical total bit 8 to 9
D2-3 Reserved
D4-5 Extended CRT vertical blank start bit 8 to 9
D6-7 Extended CRT vertical retrace start bit 8 to 9

Extended Indexed Register CREG F7 : 350-Line Extended CRT Vertical Total Register

This is a read/write register. Port address is Hex 3D5.
Default value after hardware reset is Hex 00.

D0-7 Extended CRT Extended CRT vertical total bit 0 to 7 (-2)

Extended Indexed Register CREG F8 : Reserved

This is a read/write register. Port address is Hex 3D5.
Default value after hardware reset is Hex 00.

D0-7 Reserved

Extended Indexed Register CREG F9 : 350-Line Extended CRT Vertical Blank Start

This is a read/write register. Port address is Hex 3D5.
Default value after hardware reset is Hex 00.

D0-7 Extended CRT vertical blank start bit 0 to 7 (-1)

Extended Indexed Register CREG FA : 350-Line Extended CRT Vertical Blank End

This is a read/write register. Port address is Hex 3D5.
Default value after hardware reset is Hex 00.

D0-7 Extended CRT vertical blank end bit 0 to 7

Extended Indexed Register CREG FB : 350-Line Extended CRT Vertical Retrace Start

This is a read/write register. Port address is Hex 3D5.
Default value after hardware reset is Hex 00.

D0-7 Extended CRT vertical retrace start bit 0 to 7

Extended Indexed Register CREG FC : 350-Line Extended CRT Vertical Retrace End

This is a read/write register. Port address is Hex 3D5.
Default value after hardware reset is Hex 00.

D0-3 Extended CRT vertical retrace end bit 0 to 3
D4-7 Reserved

Extended Indexed Register CREG FD : 350-Line Extended CRT Vertical Overflow

This is a read/write register. Port address is Hex 3D5.
Default value after hardware reset is Hex 00.

D0-1 Extended CRT vertical total bit 8 to 9
D2-3 Reserved
D4-5 Extended CRT vertical blank start bit 8 to 9
D6-7 Extended CRT vertical retrace start bit 8 to 9

PCI Local Bus Configuration Register Description

The following registers are TP6508 PCI local bus configuration registers. These registers are accessed by first writing the index of the desired register to the Index register, i.e. address Hex CF8 and then accessing the register using the address Hex CFC. Read accesses to reserved (index Hex 0C,0D,0F,18,1C,20,24,28,2C,30,34,38,3E,3F) or unimplemented (index Hex 40 to FF) register can be completed normally and a data value of 0 returned.

Extended Index Register PREG Hex 00 : Vendor ID Register

This is a read only register. Port address is Hex CFC.
Default value after hardware reset is Hex 10D4.

D0-15	Vendor ID bit 0 to 15

Bit 0-15 This field identifies the manufacturer of the device.

Extended Index Register PREG Hex 02 : Device ID Register

This is a read only register. Port address is Hex CFC.
Default value after hardware reset is Hex 860B.

D0-15	Device ID bit 0 to 15

Bit 0-15 This field identifies the particular device. The bit 0 to 4 is as same as the bit of Identification Code in Extended Reg. SREG 05.

Extended Index Register PREG Hex 04 : Command Register

This is a read/write register. Port address is Hex CFC.
Default value after hardware reset is Hex 0000.

D0	IO space
D1	Memory space
D2	Bus Master (Reserved =0)
D3	Special cycle (Reserved =0)
D4	Memory write and invalidate (Reserved =0)
D5	VGA palette snoop
D6	PERR# enable
D7	Wait cycle control (Reserved =0)
D8	SERR# enable
D9	Fast Back-to-Back Enable (Reserved =0)
D10-15	Reserved =0

Bit 0 Controls TP6508 response to I/O space accesses . A logical 0 disables the device response. A logical 1 allows the device to respond to I/O space accesses .

Bit 1 Controls TP6508 response to memory space accesses . A logical 0 disables the device response. A logical 1 allows the device to respond to memory space accesses .

Bit 2 Implemented by bus masters only. Controls a device's ability to act as a master on PCI bus. A logical 1 allows the device to behave as a bus master . A logical 0 disables it .

Bit 3 Controls a device's action on special cycle operation .

Bit 4 This is an enable bit for using the Memory Write and Invalidate command .

Bit 5 When this bit is set to logical 1 , special palette snooping behavior is enabled . When this bit is reset to logical 0 , the device should treat palette accesses like all other accesses .

Bit 6 This bit controls the device's response to data parity errors. When this bit is set, the devicem u s t take its normal action when a parity error is detected. When this bit is reset, the device must ignore any parity error that it detects and continue normal operation.

Bit 7 This bit is used to control whether or not a device does address/data stepping.

Bit 8 This bit is an enable bit for the SERR# driver. A logical 1 enables the SERR# driver and report address parity error. A logical 0 disables the SERR# driver.

Bit 9 Implemented by bus masters only.

Bit 10-15 Reserved.

Extended Index Register PREG Hex 06 : Status Register

This is a read/write register. Port address is Hex CFC.
Default value after hardware reset is Hex 0280.

D0-4	Reserved =0
D5	66 MHz capable (read only =0)
D6	UDF support (read only =0)
D7	Fast Back-to-Back capable (read only =1)
D8	Data Parity Error Detected (reserved =0)
D9-10	DEVSEL# timing (read only =01)
D11	Signaled Target Abort
D12	Received Target Abort (Reserved =0)
D13	Received Master Abort (Reserved =0)
D14	Signaled System Error
D15	Dected Parity Error

(A write operation to this register can be reset, but not set.)

Bit 0-4 Reserved.

Bit 5 A logical 1 indicates a device is capable of running at 66 MHz. A logical 0 indicates 33 MHz.

Bit 6 This optional bit indicates that this device supports User Difinable Features.

Bit 7 This optional bit indicates whether or not the target is capable of accepting fast back-to-back transactions when the transactions are not to the same agent.

Bit 8 Implemented by bus masters only.

Bit 9-10 These bits encode timing of DEVSEL#. There are three allowable timings for asserted of DEVESEL# . They are encoded as binary value 00 for fast , 01 for medium , and 10 for slow .

Bit 11 This bit is set by TP6508 whenever its transaction is terminated with target-abort.

Bit 12 Implemented by bus masters only.

Bit 13 Implemented by bus masters only.

Bit 14 This bit must be set whenever the device asserts SERR#.

Bit 15 This bit must be set by the device whenever it detects a parity error, even if parity error handing is disabled by bit 6 in the Command register.

Extended Index Register PREG Hex 08 : Revision ID Register

This is a read only register. Port address is Hex CFC.
Default value after hardware reset is Hex 00.

D0-7	Revision ID bit 0 to 7

Bit 0-7 These bits specify TP6508 specific revision identifier. The bit 0 to 2 is as same as the bit of Revision Code of Extended Reg. SREG 05.

Extended Index Register PREG Hex 09 : Prog. Class Code Register

This is a read only register. Port address is Hex CFC.
Default value after hardware reset is Hex 00.

D0-7 Class code bit 0 to 7

Bit 0-7 The class code register is broken into three byte-size field. The upper byte (at offset 0Bh) is a base class code which broadly classifies the type of function the device performs. The middle byte (at offset 0Ah) is a sub-class code which identifies more specific the function of the device. The lower byte (at offset 09h) identifies a specific register-level programming interface so that device independent software can interact with the device. TP6508 sets the class code of Hex 03,00,00 to mean that is a VGA compatible controller .

Extended Index Register PREG Hex 0A : Sub-Class Code Register

This is a read only register. Port address is Hex CFC.
Default value after hardware reset is Hex 00.

D0-7 Class code bit 8 to 15

Extended Index Register PREG Hex 0B : Base Class Code Register

This is a read only register. Port address is Hex CFC.
Default value after hardware reset is Hex 03.

D0-7 Class code bit 16 to 23

Extended Index Register PREG Hex 0C : Reserved

This is a read/write register. Port address is Hex CFC.
Default value after hardware reset is Hex 00.

D0-7 Reserved=0

Extended Index Register PREG Hex 0D : Reserved

This is a read/write register. Port address is Hex CFC.
Default value after hardware reset is Hex 00.

D0-7 Reserved=0

Extended Index Register PREG Hex 0E : Header Type Register

This is a read/write register. Port address is Hex CFC.
Default value after hardware reset is Hex 00.

D0-7 Header type bit 0 to 7

Bit 0-7 These bits identify the layout of bytes index 10h through 3Fh in configuration space .

Extended Index Register PREG Hex 0F : Reserved

This is a read/write register. Port address is Hex CFC.
Default value after hardware reset is Hex 00.

D0-7 Reserved =0

Extended Index Register PREG Hex 10 : Display Memory Base Address Register

This is a read/write register. Port address is Hex CFC.
Default value after hardware reset is Hex 0000,0000.

D0	Display memory space indicator (read-only =0)
D1-2	Type select bit 0 to 1 (read-only =00)
D3	Prefectchable bit (read-only =0)
D4-20	Base address bit 4 to 19 (read-only =0)
D21	Base address bit 21 (read-only =0; for 4M-byte display memory)
D22-31	Base address bit 22 to 31

(SREG F1 provides the same function for ISA/Local bus only.)

Bit 0 This bit is read-only and used to determine whether the register maps into Memory or I/O space. Base registers that map to Memory space must return a 0 in bit 0 . Base registers that map to I/O space must return a 1 in bit 0. Then , TP6508 set this bit to logical 0 .

Bit 1-2 These bit is read-only . For memory base registers , bit 2 and 1 have an encoded meaning as shown in the following description . Then , TP6508 set these bits to binary logical 00 .

Bit 2	Bit 1	Meaning
0	0	Base register is 32 bits wide and mapping can be done anywhere in the 32-bit memory space .
0	1	Base register is 32 bits wide Bust must be mapped below 1M in memory space.
1	0	Base register is 64 bits wide and can be mapped anywhere in the 64-bit memory space .
1	1	Reserved.

Bit 3 This bit is read-only . TP6508 set this bits to logical 1 and the data is perfectible .

Bit 4-21 There are 4M-byte display memory address space for TP6508 setting. The lower 2MB is for display memory and upper 2MB is for memory mapped IO. Power-up software can determine how much address space TP6508 required by writing a value of all 1's to the register and then reading the value back. When TP6508 has over 1M-byte display memory , it will return 0's in these don't care address bits.

Bit 22-31 By the description of previous bits , the bits 22 through 31 would implement on read and write operation for power-up software determining 4M-byte address space.

Extended Index Register PREG Hex 14 : I/O command Base Address Register

This is a read/write register. Port address is Hex CFC.
Default value after hardware reset is Hex 0000,0001.

D0	I/O command space indicator (read-only =1)
D1	Reserved =0
D2-7	Base address bit 2 to 7 (read-only =0)
D8-31	Base address bit 8 to 31

Bit 0 This bit is read-only and used to determine whether the register maps into Memory or I/O space. Base registers that map to Memory space must return a 0 in bit 0 . Base registers that map to I/O space must return a 1 in bit 0. Then , TP6508 set this bit to logical 1 .

Bit 1 This bit is reserved , and must return 0 on reads.

Bit 2-7 TP6508 has 256-byte I/O address space . Power-up software can determine how much address space TP6508 required by writing a value of all 1's to the register and then reading the value back . TP6508 will return 0's in these don't care address bits .

Bit 8-31 By the description of previous bits , the bits 8 through 31 would implement on read and write operation for power-up software determining 256-byte address space.

Extended Index Register PREG Hex 18, 1C, 20, 24, 28, 2C, 30, 34, 38 : Reserved

This is a read/write register. Port address is Hex CFC.
Default value after hardware reset is Hex 0000,0000.

D0-31 Reserved =0

Extended Index Register PREG Hex 3C : Interrupt Line Register

This is a read/write register. Port address is Hex CFC.
Default value after hardware reset is Hex 00.

D0-7 Reserved =0

Extended Index Register PREG Hex 3D : Interrupt Pin Register

This is a read/write register. Port address is Hex CFC.
Default value after hardware reset is Hex 00.

D0-7 Reserved =0

Extended Index Register PREG Hex 3E : Reserved

This is a read/write register. Port address is Hex CFC.
Default value after hardware reset is Hex 00.

D0-7 Reserved =0

Extended Index Register PREG Hex 3F : Reserved

This is a read/write register. Port address is Hex CFC.
Default value after hardware reset is Hex 00.

D0-7 Reserved =0

Graphics Engine Control Register Description

The following registers with 16-bit data width are Topro VGA Graphics Engine control registers. There are two addressing types, base addressing, and memory map I/O addressing, to access these registers.

By base addressing, these registers are accessed at Port binary address xxxx,xxYY,YYYY,YY00. The address value - 'Y..' is determined by Graphics Engine Port Address Low Register. They are set default hex. F1 and F3. The high address value - 'xx' is determined by following Graphics Engine control register indexed value. Then Topro VGA can access these registers with 16-bit data width by decoding at them, being conjunction with 'x..' and 'Y..' , directly .

By memory map I/O addressing, these registers are accessed as memory command and located at memory address binary ZZZZ,ZZZZ,xxxx,xxYY,YYYY,YY00. The 'Y..' and 'x..' are as same as the decription of previours paragraph. The address value - 'Z..' is determined by Extended register-Memory Mapping I/O Offset Register and it is set default Hex 00.

For PCI system access, the GEC. regs. are addressed at by setting PREG 14 and the PCI port address low which is described in the following GEC. register description. The PCI configuration register PREG 14 is used as the higher 8-bit port address and the PCI port address low is defined as the lower 8-bit port address for PCI local bus.

GAREG Hex 01 : Source X Offset Register

This is a read/write register. Default port address 07C4. PCI port address low 04.
Default value after hardware reset is Hex 00,00.

D0-10	Source X bit 0 to 10
D11-15	Reserved

Bit 0-10 These bits would use to define source X screen position and transfer to memory address for BITBLT operations. Also, these bits are use to define starting X screen position for Line Drawing operations.
Bit 11-15 Reserved .

GAREG Hex 02 : Source Y Offset Register

This is a read/write register. Default port address 0BC4. PCI port address low 08.
Default value after hardware reset is Hex 00,00.

D0-10	Source Y bit 0 to 10
D11-15	Reserved

Bit 0-10 These bits would use to define source Y screen position and transfer to memory address for BITBLT operations. Also, these bits are use to define starting Y screen position for Line Drawing operations.
Bit 11-15 Reserved .

GAREG Hex 03 : Pattern X Offset Register

This is a read/write register. Default port address 0FC4. PCI port address low 0C.
Default value after hardware reset is Hex 00,00.

D0-15	Line drawing pattern bit 0 to 15

D3-10 BITBLT pattern X bit 3 to 10

Bit 0-15 These bits would use to do as the pixel-pattern when Topro VGA is in line drawing command operation.

Bit 3-10 These bits would use to define pattern X screen position and transfer to memory address for BITBLT operations.

GAREG Hex 04 : Pattern Y Offset Register

This is a read/write register. Default port address 13C4. PCI port address low 10.
Default value after hardware reset is Hex 00,00.

D0-15 Line drawing pattern bit 16 to 31
D3-10 BITBLT pattern Y bit 3 to 10

Bit 0-15 These bits would use to do as the pixel-pattern when Topro VGA is in line drawing command operation.

Bit 3-10 These bits would use to define pattern Y screen position and transfer to memory address for BITBLT operations.

GAREG Hex 05 : Destination X Offset Register

This is a read/write register. Default port address 17C4. PCI port address low 14.
Default value after hardware reset is Hex 00,00.

D0-10 BITBLT destination Y bit 0 to 10
D11-15 Reserved

Bit 0-10 These bits would use to define destination Y screen position and transfer to memory address for BITBLT operations.

Bit 11-15 Reserved.

GAREG Hex 06 : Destination Y Offset Register

This is a read/write register. Default port address 1BC4. PCI port address low 18.
Default value after hardware reset is Hex 00,00.

D0-10 BITBLT destination Y bit 0 to 10
D11-15 Reserved

Bit 0-10 These bits would use to define destination Y screen position and transfer to memory address for BITBLT operations.

Bit 11-15 Reserved.

GAREG Hex 07 : X Width & MAX. Term Register

This is a read/write register. Default port address 1FC4. PCI port address low 1C.
Default value after hardware reset is Hex 00,00.

D0-10 Width X bit 0-10 for BITBLT (number of bytes-1 per line)
Maxmum term for Line drawing (M)
D11-15 Reserved

Bit 0-10 These bits would use to define the X direction width of the rectangular region to be copied for BITBLT

operations , and as the value of the maximum term of the caculated equation for the Line Drawong operation. In BILBLK operations, these bits define the X direction width using byte as unit . The caculated equation of the maximum term (M) is :

$$M = Max (|X_2-X_1| , |Y_2-Y_1|)$$

Bit 11-15 Reserved .

GAREG Hex 08 : Y Width & Error Term Register

This is a read/write register. Default port address 23C4. PCI port address low 20.
Default value after hardware reset is Hex 00,00.

D0-10 Width Y bit 0-10 for BITBLT (number of line-1)
D0-12 Error term for Line drawing (E)
D13-15 Reserved

Bit 0-10/12 These bits would use to define the Y direction width of the rectangular region to be copied for BITBLT operations , and as the value of the error term of the caculated equation for the Line Drawong operation. In BILBLK operations, these bits define the Y direction width using line as unit . The caculated equation of the error term (E) is :

$$E = 2 [Min (|X_2-X_1| , |Y_2-Y_1|)-Max (|X_2-X_1| , |Y_2-Y_1|)]$$

Bit 13-15 Reserved .

GAREG Hex 09 : Foreground Color Register 1

This is a read/write register. Default port address 27C4. PCI port address low 24.
Default value after hardware reset is Hex 00,00.

D0-15 Foreground color bit 0 to 15

Bit 0-15 These bits would use to define the foreground color for rectangular fill, color expansion, and line drawing. Conjunction with foreground color bit 16 to 31,that descripts in GAREG 0A, we must write with the same color data(byte) into bit 0-7, bit 8-15, bit 16-23, and bit 24-31 for 256-color mode. In different we must write with the same color data(word) into bit 0-15, and bit 16-31 for hi-color mode. Another condiction we use bit 0-23 as color data and reserved bit 24-31 for ture-color mode.

GAREG Hex 0A : Foreground Color Register 2

This is a read/write register. Default port address 2BC4. PCI port address low 28.
Default value after hardware reset is Hex 00,00.

D0-15 Foreground color bit 16 to 31

Bit 0-15 These bits would use to define the foreground color for rectangular fill, color expansion, and line drawing.

GAREG Hex 0B : Background Color Register 1

This is a read/write register. Default port address 2FC4. PCI port address low 2C.
Default value after hardware reset is Hex 00,00.

D0-15 Background color bit 0 to 15

Bit 0-15 These bits would use to define the background color for background fill, color expansion, and line drawing. Conjunction with background color bit 16 to 31,that descripts in GAREG 0C, we must write with the same color data(byte) into bit 0-7, bit 8-15, bit 16-23, and bit 24-31 for 256-color mode. In different we must write with the same color data(word) into bit 0-15, and bit 16-31 for hi-color mode. Another condiction we use bit 0-23 as color data and reserved bit 24-31 for ture-color mode.

GAREG Hex 0C : Background Color Register 2

This is a read/write register. Default port address 33C4. PCI port address low 30.
Default value after hardware reset is Hex 00,00.

D0-15 Background color bit 16 to 31

Bit 0-15 These bits would use to define the background color for background, color expansion, and line drawing.

GAREG Hex 0D : Transparency Color Register 1

This is a read/write register. Default port address 37C4. PCI port address low 34.
Default value after hardware reset is Hex 00,00.

D0-15 Transparency color bit 0 to 15

Bit 0-15 These bits would use to define the transparency color for all graphics engine commands except image read. Conjunction with transparency color bit 16 to 31,that descripts in GAREG 0E, we must write with the same color data(byte) into bit 0-7, bit 8-15, bit 16-23, and bit 24-31 for 256-color mode. In different we must write with the same color data(word) into bit 0-15, and bit 16-31 for hi-color mode. Another condiction we use bit 0-23 as color data and reserved bit 24-31 for ture-color mode.

GAREG Hex 0E : Transparency Color Register 2

This is a read/write register. Default port address 3BC4. PCI port address low 38.
Default value after hardware reset is Hex 00,00.

D0-15 Transparency color bit 16 to 31

Bit 0-15 These bits would use to define the transparency color all graphics engine commands except image read if transparnecy enabled.

GAREG Hex 0F : Transparency Mask Register 1

This is a read/write register. Default port address 3FC4. PCI port address low 3C.
Default value after hardware reset is Hex 00,00.

D0-15 Transparency mask bit 0 to 15

Bit 0-15 These bits would use to define the transparency mask bits that are used to compare with the transparency color all graphics engine commands except image read . Conjunction with transparnecy color bit 16 to 31,that descripts in GAREG 10, we must write with the same color data(byte) into bit 0-7, bit 8-15, bit 16-23, and bit 24-31 for 256-color mode. In different we must write with the same color data(word) into bit 0-15, and bit 16-31 for hi-color mode. Another condiction we use bit 0-23 as color data and reserved bit 24-31 for ture-color mode. The pixels of the destination are compared against the transparency color under control of the transparency mask. Eachbit of transparency mask

that is a logical 1 makes “Don’t care” for the corresponding bit of the transparency color .

GAREG Hex 10 : Transparency Mask Register 2

This is a read/write register. Default port address 43C4. PCI port address low 40.
Default value after hardware reset is Hex 00,00.

D0-15 Transparency mask bit 16 to 31

Bit 0-15 These bits would use to define the transparency mask bits that are used to compare with the transparency color all graphics engine commands except image read. The pixels of the destination are compared against the transparency color under control of the transparency mask. Each bit of transparency mask that is a logical 1 makes “Don’t care” for the corresponding bit of the transparency color .

GAREG Hex 11 : Top Clipping Position Register

This is a read/write register. Default port address 47C4. PCI port address low 44.
Default value after hardware reset is Hex 00,00.

D0-10 Top Clipping position bit 0-10
D11-15 Reserved

Bit 0-10 These bits are conjunction with GAREG 12,13,14 to define a rectangular area . Any pixel inside and on the boundary of the rectangular area can be updated during a Graphics Command operation .
Bit 11-15 Reserved

GAREG Hex 12 : Left Clipping Position Register

This is a read/write register. Default port address 4BC4. PCI port address low 48.
Default value after hardware reset is Hex 00,00.

D0-10 Left Clipping position bit 0-10
D11-15 Reserved

Bit 0-10 These bits are conjunction with GAREG 11,13,14 to define a rectangular area . Any pixel inside and on the boundary of the rectangular area can be updated during a Graphics Command operation .
Bit 11-15 Reserved

GAREG Hex 13 : Bottom Clipping Position Register

This is a read/write register. Default port address 4FC4. PCI port address low 4C.
Default value after hardware reset is Hex 00,00.

D0-10 Bottom Clipping position bit 0-10 of bit 0 to 10
D11-15 Reserved

Bit 0-10 These bits are conjunction with GAREG 11,12,14 to define a rectangular area . Any pixel inside and on the boundary of the rectangular area can be updated during a Graphics Command operation .
Bit 11-15 Reserved

GAREG Hex 14 : Right Clipping Position Register

This is a read/write register. Default port address 53C4. PCI port address low 50.
Default value after hardware reset is Hex 00,00.

D0-10	Right Clipping position bit 0-10 of bit 0 to 10
D11-15	Reserved

Bit 0-10 These bits are conjunction with GAREG 11,12,13 to define a rectangular area . Any pixel inside and on the boundary of the rectangular area can be updated during a Graphics Command operation .

Bit 11-15 Reserved

GAREG Hex 15 : Raster Operation Register

This is a read/write register. Default port address 57C4. PCI port address low 54.
Default value after hardware reset is Hex 00,00.

D0-7	Raster operation code bit 0 to 7
D8-10	Scan line width selection bits
D11-15	Reserved

Bit 0-7 Raster Operation as defined by Microsoft Windows.All logical operation of Source,Pattern, and Destination data are supported.

Bit 8-10 These bit are used to set the scanline offset in pixel unit.

Bit-10	Bit-9	Bit-8	Definition
0	0	0	1024 pixels per line
0	0	1	640 pixels per line
0	1	X	800 pixels per line
1	0	0	2048 pixels per line
1	0	1	1280 pixels per line
1	1	X	1600 pixels per line

Bit 11-15 Reserved.

GAREG Hex 16 : Graphics Engine Control Register

This is a read/write register. Default port address 5BC4. PCI port address low 58.
Default value after hardware reset is Hex 00,00.

D0	X direction
D1	Y direction
D2	Source select/Major movement
D3	Destination select/Last pixel display enable
D4	Graphics function mode select
D5	Background transparency enable for color expansion and line drawing
D6	Transparency enable
D7	Rectangular clipping enable
D8-9	Source format
D10	Transparency polarity
D11	Rectangular clipping polarity
D12	Line drawing pattern width select
D13-15	Reserved

Bit 0 This bit is used to select the direction of X direction. A logical 0 indicates in the increasing direction , and a logical 1 indicates in the decreasing direction.

Bit 1 This bit is used to select the direction of Y direction . A logical 0 indicates in the increasing direction , and a logical 1 indicates in the decreasing direction .

Bit 2 This bit selects the source as either the screen memory or the host CPU memory for BITBLT opera-

tion. A logical 1 selects Host CPU memory, and a logical 0 select screen memory. Also, it is used to control whether the major movement is in the X or Y direction for Line Drawing operation. A logical 0 indicates in the Y direction(ΔY>ΔX)
, and a logical 1 indicates in the X direction(ΔY<ΔX).

Bit 3 This bit selects the destination as either the screen memory or the host CPU memory. A logical 1 selects Host CPU memory , and a logical 0 screen memory. Also, this bit is used enable last pixel write for Line Drawing. A logical 1 enables to write last pixel, and a logical 0 disables it.

Bit 4 This bit would use to select the active Graphics Engine command . A logical 0 indicates Topro VGA to be selected in BITBLT operation. A logical 1 indicates Topro VGA to be selected in Line Drawing operation.

Bit 5 A logical 1 enables the color expansion or line drawing transparency feature . A logical 0 disables it, and enables the Background color.

Bit 6 A logical 1 enables the transparency feature .

Bit 7 A logical 1 enables the rectangular clipping feature.

Bit 8-9 These bits specify the format of the BITBLT source .

Bit 9	Bit 8	Function
0	0	VGA Color (256/64k/16.8M format)
0	1	Video color (Video engin enable)
1	0	Fixed color (From foreground color Reg.)
1	1	Monochrome from Host for color expansion

Bit 10 This bit is used to control the transparency polarity. A logical 1 is set to positive polarity , a logical 0 is set to negative polarity.

Bit 11 This bit is used to control the rectangular clipping polarity. A logical 0 is enables the write access of pixels in or on the rectangular defined by GAREG11,12,13,14. A logical 1 is enables the write access of pixels out of the rectangular defined by GAREG11,12,13,14.

Bit 12 These bits specify the Line Drawing pattern width.

Bit 12	Pattern Width
0	8 bit ; if ΔX>ΔY, each bit represent 4 pixel. if ΔX<ΔY, each bit represent 3 pixel.
1	32 bit ; each bit represent 1 pixel.

Bit 13-15 Reserved.

GAREG Hex 20 : Host to Display Data Transfer Register

This is a read/write register. Default port address 83C4. PCI port address low 80.
Default value after hardware reset is Hex 00,00,00,00.

D0-31 Data port for image read/write, color expansion

GAREG Hex 21 : Hardware Cursor Pattern Start Address Register

This is a read/write register. Default port address 87C4. PCI port address low 84.
Default value after hardware reset is Hex 00,00.

D0-15	Memory address A6 to A21 for hardware cursor pattern

Bit 0-15 These bits would use to define the location in the display memory where the cursor pattern is stored . The cursor pattern may be stored anywhere in the display memory but is generally stored in a non-visible location (off-screen memory) . We can set the line offset of hardware cursor pattern in GAREG 26 bit-14 . Others , the start address of hardware cursor pattern has an address-alignment limit as follows :

1) If GAREG 26 bit-14 = 0 (line offset = 16 bytes) , then the start address of hardware cursor pattern must be 1k-byte alignment . It is easy to fill hardware cursor pattern data contiuously . This register bit-mapping of memory address is : (x : no used)

D0 ,D1 ,D2 ,D3 ,D4 ,D5 ,D6 ,D7 ,D8 ,D9 ,D10,D11,D12,D13,D14,D15
== x , x , x , x ,A10,A11,A12,A13,A14,A15,A16,A17,A18,A19,A20,A21

2) If GAREG 26 bit-14 = 1 (line offset = 2048 bytes) , then the start address of hardware cursor pattern can be 64-byte alignment in the first 2048-byte memory address (A6-A10) of any 64x2048-byte memory segment (A17-A21) . It is useful for 1280x or 1600x display mode . This register bit-mapping of memory address is : (x : no used)

D0 ,D1 ,D2 ,D3 ,D4 ,D5 ,D6 ,D7 ,D8 ,D9 ,D10,D11,D12,D13,D14,D15
== A6 ,A7 ,A8 ,A9 ,A10, x , x , x , x , x ,A17,A18,A19,A20,A21

GAREG Hex 22 : Hardware Cursor X&Y Origin Register

This is a read/write register. Default port address 8BC4. PCI port address low 88.
Default value after hardware reset is Hex 00,00.

D0-5	Hardware cursor X-size Xbit 0-5
D6-7	Reserved
D8-13	Hardware cursor Y-size Ybit 0-5
D14-15	Reserved

Bit 0-5 These bits would use to define the X offset in pixels from the left edge of the pattern which will be displayed at the cursor display position .

D0 ,D1 ,D2 ,D3 ,D4 ,D5
==XO0,XO1,XO2,XO3,XO4,XO5

Bit 6-7 Reserved

Bit 8-13 These bits would use to define the Y offset in pixels from the top edge of the pattern which will be displayed at the cursor display position .

D8 ,D9 , D10,D11 ,D12 ,D13
==YO0,YO1,YO2,YO3,YO4,YO5

Bit 14-15 Reserved

GAREG Hex 23 : Hardware Cursor X Display Position Register

This is a read/write register. Default port address 8FC4. PCI port address low 8C.
Default value after hardware reset is Hex 00,00.

D0-7	Hardware cursor display X position bit 0-7
D8-10	Hardware cursor display X position bit 8-10
D11-15	Reserved

Bit 0-10 These bits would use to define the X location on the screen at which the cursor origin is displayed . These values represent a position in pixels , referenced to the left edge of the screen .

D0, D1, D2 , D3 ,D4 ,D5 ,D6 ,D7 ,D8 ,D9 ,D10

== XP0,XP1,XP2,XP3,XP4,XP5,XP6,XP7,XP8,XP9,XP10

Bit 11-15 Reserved

GAREG Hex 24 : Hardware Cursor Y Display Position Register

This is a read/write register. Default port address 93C4. PCI port address low 90.
Default value after hardware reset is Hex 00,00.

D0-7	Hardware cursor display Y position bit 0-7
D8-10	Hardware cursor display Y position bit 8-10
D11-15	Reserved

Bit 0-10 These bits would use to define the Y location on the screen at which the cursor origin is displayed . These values represent a position in pixels , referenced to the top edge of the screen .

D0 ,D1 ,D2 ,D3 ,D4 ,D5 ,D6 ,D7 ,D8 ,D9 ,D10

== YP0,YP1,YP2,YP3,YP4,YP5,YP6,YP7,YP8,YP9,YP10

Bit 11-15 Reserved

GAREG Hex 25 : Hardware Cursor Primary Color Register 1

This is a read/write register. Default port address 97C4. PCI port address low 94.
Default value after hardware reset is Hex 00,00.

D0-7	Hardware cursor primary color bit 0 to 7 for 8 bit color mode
D8-15	Hardware cursor primary color bit 8 to 15 for 16 bit color mode

Bit 0-7 These bits would use to define the primary color of hardware cursor for 8 bit color mode.
Bit 8-15 These bits would use to define the primary color of hardware cursor for 16 bit color mode.

GAREG Hex 26 : Hardware Cursor Primary Color Register 2

This is a read/write register. Default port address 97C4. PCI port address low 98.
Default value after hardware reset is Hex 00,00.

D0-7	Hardware cursor primary color bit 16 to 23 for 24 bit color mode
D8-13	Reserved
D14	Hardware cursor pattern address line offset selection
D15	Enable hardware cursor

Bit 0-7 These bits would use to define the primary color of hardware cursor for 24 bit color mode.
Bit 8-13 Reserved
Bit 14 This bit is used to select memory line offset of hardware cursor pattern.

0: 16-byte
1: 2048-byte

Bit 15 A logical 1 enables Topro VGA's Hardware Cursor function in operation . A logical 0 disables it. The data definition of hardware cursor pattern list in following description .

Data bit-1	Data bit-0	Definition
0	0	Hardware cursor Primary color
0	1	Hardware cursor Secondary color
1	0	Transparent
1	1	Inversion or hardware cursor auxiliary color (decided by GAREG 2A bit-15 selection)

GAREG Hex 27 : Hardware Cursor Secondary Color Register 1

This is a read/write register. Default port address 9FC4. PCI port address low 9C.
Default value after hardware reset is Hex 00,00.

D0-7	Hardware cursor secondary color bit 0 to 7 for 8 bit color mode
D8-15	Hardware cursor secondary color bit 8 to 15 for 16 bit color mode

Bit 0-7 These bits would use to define the secondary color of hardware cursor for 8 bit color mode.
Bit 8-15 These bits would use to define the secondary color of hardware cursor for 16 bit color mode.

GAREG Hex 28 : Hardware Cursor Secondary Color Register 2

This is a read/write register. Default port address A3C4. PCI port address low A0.
Default value after hardware reset is Hex 00,00.

D0-7	Hardware cursor secondary color bit 16 to 23 for 24 bit color mode
D8-14	Reserved
D15	Exchange primary color and secondary color

Bit 0-7 These bits would use to define the secondary color of hardware cursor for 24 bit color mode.
Bit 8-14 Reserved.
Bit 15 A logical 1 forces the hardware cursor display color to be Reverse . The Hardware cursor Primary color and Secondary color are changed each other in the data definition description of GAREG 26 by bit-15. A logical 0 disables it .

GAREG Hex 29 : Hardware Cursor Auxiliary Color Register 1

This is a read/write register. Default port address A7C4. PCI port address low A4.
Default value after hardware reset is Hex 00,00.

D0-7	Hardware cursor auxiliary color bit 0 to 7 for 8 bit color mode
D8-15	Hardware cursor auxiliary color bit 8 to 15 for 16 bit color mode

Bit 0-7 These bits would use to define the auxiliary color of hardware cursor for 8 bit color mode.
Bit 8-15 These bits would use to define the auxiliary color of hardware cursor for 16 bit color mode.

GAREG Hex 2A : Hardware Cursor Auxiliary Color Register 2

This is a read/write register. Default port address ABC4. PCI port address low A8.
Default value after hardware reset is Hex 00,00.

D0-7	Hardware cursor auxiliary color bit 16 to 23 for 24 bit color mode
D8-14	Reserved
D15	Enable three color mode

Bit 0-7 These bits would use to define the auxiliary color of hardware cursor for 24 bit color mode.
Bit 8-14 Reserved
Bit 15 This bit is used to select Hardware Cursor display color mode . A logical 0 indicates Topro VGA is operated in two color mode . A logical 1 forces Topro VGA is operated in three color mode by using cursor Auxiliary color to replace inversion destination data color.

GAREG Hex 2B : Graphics Command FIFO Status Register

This is a read/write register. Default port address AFC4. PCI port address low AC.
Default value after hardware reset is Hex 00,00.

D0	Graphics command access status
D1	Host memory from Display memory write status
D2	Host memory to Display memory read status
D3	Command FIFO empty status
D4	Command FIFO full status
D5-7	Video line buffer valid status
D8-15	Command FIFO valid status

(*: Write access operation will reset graphic engine)

Bit 0 This bit reflects the access status of Graphics commands . A logical 1 indicates Topro VGA is excuting the Graphics command in busy ststus now . A logical 0 indicates Topro VGA has excuted the Graphics command.
Bit 1 This bit reflects the write access status of Host memory to Display memory . A logical 1 indicates Topro VGA is busy now .
Bit 2 This bit reflects the read access status of Host memory from Display memory . A logical 1 indicates Topro VGA is busy now .
Bit 3 This bit reflects the command FIFO empty status . A logical 0 indicates the command FIFO is empty now . A logical 1 indicates the command FIFO isn't empty .
Bit 4 This bit reflects the command FIFO full status . A logical 0 indicates the command FIFO isn't full . A logical 1 indicates the command FIFO is full now .
Bit 5-7 These bits reflects the video line buffer vaild status as following description .

Bit-7	Bit-6	Bit-5	Status description
0	0	0	Video line buffer empty blocks < 4 (32-bits data/1 block)
0	0	1	Video line buffer empty blocks >= 4
0	1	1	Video line buffer empty blocks >= 8
1	1	1	Video line buffer empty blocks >= 16

Bit 8-15 These bits reflects the command FIFO vaild status as following description .

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit 8	Status description
1	1	1	1	1	1	1	1	0 empty FIFO is available (Full)
0	1	1	1	1	1	1	1	1 empty FIFO is available
0	0	1	1	1	1	1	1	2 empty FIFO is available
0	0	0	1	1	1	1	1	3 empty FIFO is available
0	0	0	0	1	1	1	1	4 empty FIFO is available
0	0	0	0	0	1	1	1	5 empty FIFO is available
0	0	0	0	0	0	1	1	6 empty FIFO is available
0	0	0	0	0	0	0	1	7 empty FIFO is available
0	0	0	0	0	0	0	0	8 empty FIFO is available (Empty)

VIII. Absolute Maximum Rating

Storage temperature	-40 to +125 degree c
Ambient temperature under bias	0 to +70 degree c
Voltage on any pin with respect to ground	GND-0.5 to VCC +0.5V
Active mode power dissipation	1.8 Watts
Power supply voltage	7 Volts

IX. DC Electrical Characteristic

DC Characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
VCC	Power Supply (+5.0V)	4.75	5	5.25	V	Normal Operation
	Power Supply (+3.3V)	3	3.3	3.6	V	Normal Operation
VIL	Input Low Voltage	-0.5	-	0.8	V	VCC=5.0+-5% (a)
VIH	Input High Voltage	2	-	VCC+0.5	V	VCC=5.0+-5%
Vt+	Low to High Threshold Voltage	-	-	3.5	V	Schmitt Trigger(preset) (h)
Vt-	High to Low Threshold Voltage	1.5	-	-	V	Schmitt Trigger(preset) (h)
VOL	Output Low Voltaget (5.0V)	-	-	0.4	V	IOL=+12mA (b)
	Output Low Voltage (3.3V)	-	-	0.4	V	IOL=+12mA (b)
VOH	Output High Voltage (5.0V)	2.4	-	-	V	IOH=-12mA (b)
	Output High Voltage (3.3V)	2.4	-	-	V	IOH=-12mA (b)
Icc0	Operating Current (5.0V)	-	-	320	mA	On power mode (c)
Icc1	Operating Current (3.3V)	-	-	150	mA	On power mode (d)
Icc2	Operating Current	-	-	32	mA	Standby/Suspend mode (e)
Icc3	Operating Current	-	-	18	mA	Off power mode (f)
Icc4	Operating Current (5.0V)	-	-	165	mA	Cover close mode (g)
IIL	Input Leakage Current	-10	-	10	uA	VSS<VIN<VCC
IOTL	Output Tri-state Leakage	-10	-	10	uA	
CIN	Input Capacitance	-	-	10	pF	
COUT	Output Capactance	-	-	10	pF	

(a) RESET pin is CMOS level

(b) See the DC Drive Characteristics on the next table

(c) VCLK = 25.175 MHz , MCLK = 55 MHz (CRT-PANEL Dual display)

VCLK = 129.400 MHz , MCLK = 60 MHz (CRT only display)

(d) VCLK = 65 MHz , MCLK = 55 MHz (CRT only display)

(e) VCLK = 0, MCLK = 7 MHz (CRT-PANEL Dual display)

(f) VCLK = 0 , MCLK = DRAMs refresh frequency 32KHz (CRT-PANEL Dual display)

(g) VCLK = 25.175 MHz , MCLK = 55 MHz

(h) Test voltage level range : +/- 200mv

[85.12.09 508DC.TBL]

DC Drive Characteristics

Symbol	Parameter	Output Pins	Min	Unit	Conditions
IOL	Output Low Drive	LRDY#,LDEV#,HSYNC,VSYNC SHFCLK,FPVCC,FPVEE,FPBACK	12	mA	Output voltage=VOL
		D[31:0],A[27:24],OEAB* LP,FLM,M,P[23:0]	8	mA	Output voltage=VOL
		All other output pins	4	mA	Output voltage=VOL
IOH	Output High Drive	LRDY#,LDEV#,HSYNC,VSYNC SHFCLK,FPVCC,FPVEE,FPBACK	12	mA	Output voltage=VOH
		D[31:0],A[27:24],OEAB* LP,FLM,M,P[23:0]	8	mA	Output voltage=VOH
		All other output pins	4	mA	Output voltage=VOH

<note> Operating voltage is 4.75v for 5V operation and 3.3v for 3.3V operation.

[85.02.09 508DC2.TBL]

DAC Characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
Vo	Output voltage		1		V	Io< 20mA
Io	Output Current		20	30	mA	Vo< 1.0v, 37.5ohm load
	DAC Resolution			8	Bits	
	Full Scale Error			+/-5	%	
	DAC to DAC Cross-talk			TBD	%	
	DAC Linearity	+/-2			LSB	
	Full Scale settling Time			15	ns	
	Output Rise/Fall Time			6	ns	10% to 90%
	Comparator Sensitivity		50		mV	

<note> Operating voltage is 5.0v for 5V operation and 3.3v for 3.3V operation.

[85.02.09 508DC3.TBL]

X. AC Electrical Characteristic

AC Testing VIH / VIL : 5.0/0.0 Volt
VOH / VOL : 2.0/0.8 Volt
(VCLK = 28.322MHZ / MCLK = 55MHz)
" Non-100% test "

BIOS ROM Interface Timing SPEC.

Symbol	Parameter Description	MIN.	MAX.	Units
T1	SA0-19 setup time to SMEMR*	20		ns
T2	SA0-19 hold time to SMEMR*	150		ns
T3	SMEMR* pulse low width	150		ns
T4	SMEMR* asserted to SD floated delay		20	ns
T5	SD floated delay from SMEMR* negated		60	ns
T6	Delay time from SMEMR* low to ROMCS* low		40	ns
T7	Delay time from SMEMR* high to ROMCS* high		40	ns

[84.06.26 SP508T01.TBL]

ISA Bus Interface Timing SPEC.

Symbol	Parameter Description	MIN.	MAX.	Units
T1	SBHE*,SA[16:0] to COMMAND (SMEMR*, SMEMW*, IORD*, IOWR*) low setup time	18		ns
T2	SBHE*,SA[16:0] to COMMAND low hold time	10		ns
T3	LA[23:17] to COMMAND low setup time	20		ns
T4	LA[23:17] to COMMAND high hold time	10		ns
T5	SD[15:0] write data to IOWR*/MEMW* high setup time	20		ns
T6	SD[15:0] read/write data/ to COMMAND high hold time	10		ns
T7	IORD* pulse low width	70		ns
T8	IOWR* pulse low width	40		ns
T9	SD[15:0] read data valid after IORD* low		70	ns
T10	IORDY* high from SMEMR* low	10	2.45us	ns
T11	SD[15:0] read data valid from IORDY* high		40	ns
T12	OWS low from IORD* , SMEMR* low		15	ns
T13	IORDY* low from COMMAND low	10	25	ns
T14	SA[16:0] valid to IOCS16* low		35	ns
T15	IOCS16* from IOW* high hold time		20	ns
T16	LA[23:17] valid to MEMCS16*		41	ns
T17	MEMCS16* tristate from the next active ALE		39	ns
T18	AEN to IORD* , IOWR* low setup time	5		ns
T19	AEN from IORD* , IOWR* high setup time	5		ns
T20	REF* to SMEMR* low setup time	20		ns
T21	REF* from SMEMR* high hold time	0		ns

[84.06.26 SP508T02.TBL]

PCI Local Bus Interface Timing SPEC.

Symbol	Parameter Description	MIN.	MAX.	Units
T1	FRAME# setup time to CLK high	5.1		ns
T2	FRAME# hold time from CLK high	3.7		ns
T3	Address setup time to CLK high	4.9		ns
T4	Address hold time from CLK high	1.6		ns
T5	Read data activ delay from CLK high		25	ns
T6	Read data hold time from CLK high	4.1		ns
T7	Command setup time to CLK high	2		ns
T8	Command hold time from CLK high	0.8		**ns**
T9	BE[3:0] setup time to CLK high	1.3		ns
T10	BE[3:0] hold time from CLK high	2		ns
T11	IRDY# setup time to CLK high	3		ns
T12	IRDY# hold time from CLK high	0.3		ns
T13	DEVSEL# low delay from CLK high		14.4	ns
T14	DEVSEL# high delay from CLK high	3.8	12.1	ns
T15	DEVSEL# tristate delay from CLK high	3.5	11.5	ns
T16	TRDY# low delay from CLK high		15.4	ns
T17	TRDY# high delay from CLK high	4	12.7	ns
T18	TRDY# tristate delay from CLK high	3.6	11	ns
T19	STOP# low delay from CLK high		19.3	ns
T20	STOP# high delay from CLK high	3.6	11.8	ns
T21	STOP# tristate delay from CLK high	3.9	12.7	ns
T22	PAR setup time to CLK high		10.4	ns
T23	PAR time from CLK high	3.1	10.4	ns

[84.06.26 SP508T12.TBL]

Memory Bus Interface Timing SPEC.

MCLK Frequency = 56 MHz

Symbol	Parameter Description	MIN.	MAX.	Units
Tm	MCLK period	17.86		ns
Th	MCLK high pulse	8.93+/-5%		ns
Tl	MCLK low pulse	8.93+/-5%		ns
T1	RAS precharge time (16-bit CPU/GFX CRT cycle)	3		Tm
T2	RAS pulse width (16-bit CPU/GFX CRT cycle)	6		Tm
T3	RAS to CAS delay time	3		Tm
T4	CAS pluse width	1.5		Tm
T5	CAS percharge time	0.5		Tm
T6	ROW address setup time	1		Tm
T7	ROW address hold time	2		Tm
T8	COLUMN address setup time	1		Tm
T9	COLUMN address hold time	1		Tm
T10	Access time from RAS	3.75		Tm
T11	Random Read/Write cycle time	9		Tm
T12	Fast Page mode cycle time	2		Tm
T13	Access time from OE* low	1.75		Tm
T14	Output disable time after OE* low	0.75		Tm
T15	Wite command setup time	1		Tm
T16	Wite command hold time	1.5		Tm
T17	Write command pulse width	4.5		Tm
T18	RAS pulse width	4		Tm
T19	Random Read/Write cycle time	7		Tm

[84.06.26 SP508T05.TBL]

Memory Interface Timing SPEC.

(Continuance)

Symbol	Parameter Description	MIN.	MAX.	Units
T20	Read-modify-Write RAS pulse width	12		Tm
T21	Read-modify-Write Random Read/Write cycle time (16-bit)	15		Tm
T22	Read-modify-Write RAS to CAS delay time	3		Tm
T23	Read-modify-Write CAS pluse width	1.5		Tm
T24	Read-modify-Write CAS percharge time	0.5	1.5	Tm
T25	Read-modify-Write Fast Page mode cycle time	2	3	Tm
T26	Read-modify-Write COLUMN address hold time	4		Tm
T27	Read-modify-Write Date-In setup time	0.5		Tm
T28	Read-modify-Write Date-In hold time	1		Tm
T29	Read-modify-Write Write command pulse width	2.5		Tm
T30	Read-modify-Write OE* command pulse width	2.5		Tm
T31	Read-modify-Write Access time from OE* low	1.25		Tm
T32	Read-modify-Write Output disable time after OE* low	0.25		Tm
T33	Read-modify-Write RAS pulse width	7		Tm
T34	Read-modify-Write Random Read/Write cycle time (32-bit)	10		Tm

[84.06.26 SP508T14.TBL]

RAMDAC & Feature Connector Interface Timing

PCLK frequency: 110 MHz

Symbol	Parameter Description	MIN.	MAX.	Units
T1	Pixel clock cycle time	9.1		ns
T2	Pixel clock pulse width high time	3.5		ns
T3	Pixel clock pulse width low time	3.5		ns
T4	VP[23:0],HSYNC,VSYNC,BLANK* setup time	3		ns
T5	VP[23:0],HSYNC,VSYNC,BLANK* hold time	3		ns
T6	Analog output delay		30	ns
T7	Analog output skew		2	ns

[84.06.26 SP508T13.TBL]

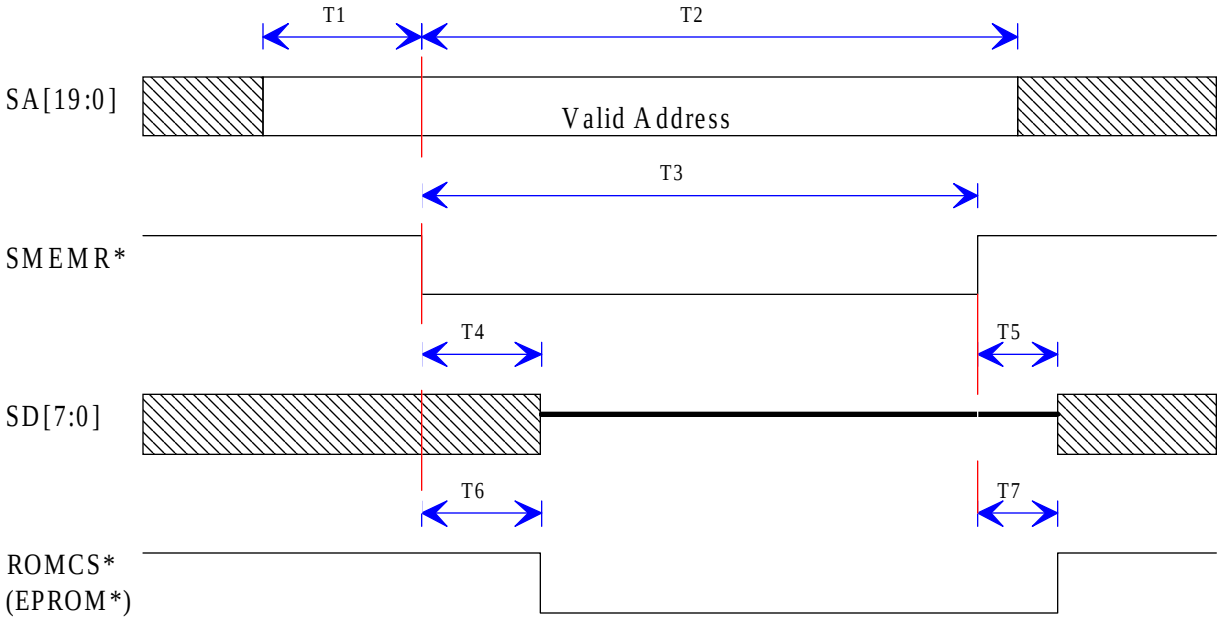
Color-Key PC Video & VAFC Interface Timing

Symbol	Parameter Description	MIN.	MAX.	Units
Tvclk	VCLK Input frequency	-	37.5	MHz
T1	VCLK Input clock High time	10	-	ns
T2	VCLK Input clock Low time	10	-	ns
T3	PC Video input data to PCLK setup time	12	-	ns
T4	PC Video input data from PCLK hold time	0	-	ns
T5	VAFC input data to PCLK setup time	10	-	ns
T6	VAFC input data from PCLK hold time	2	-	ns

[84.08.28 SP508T16.TBL]

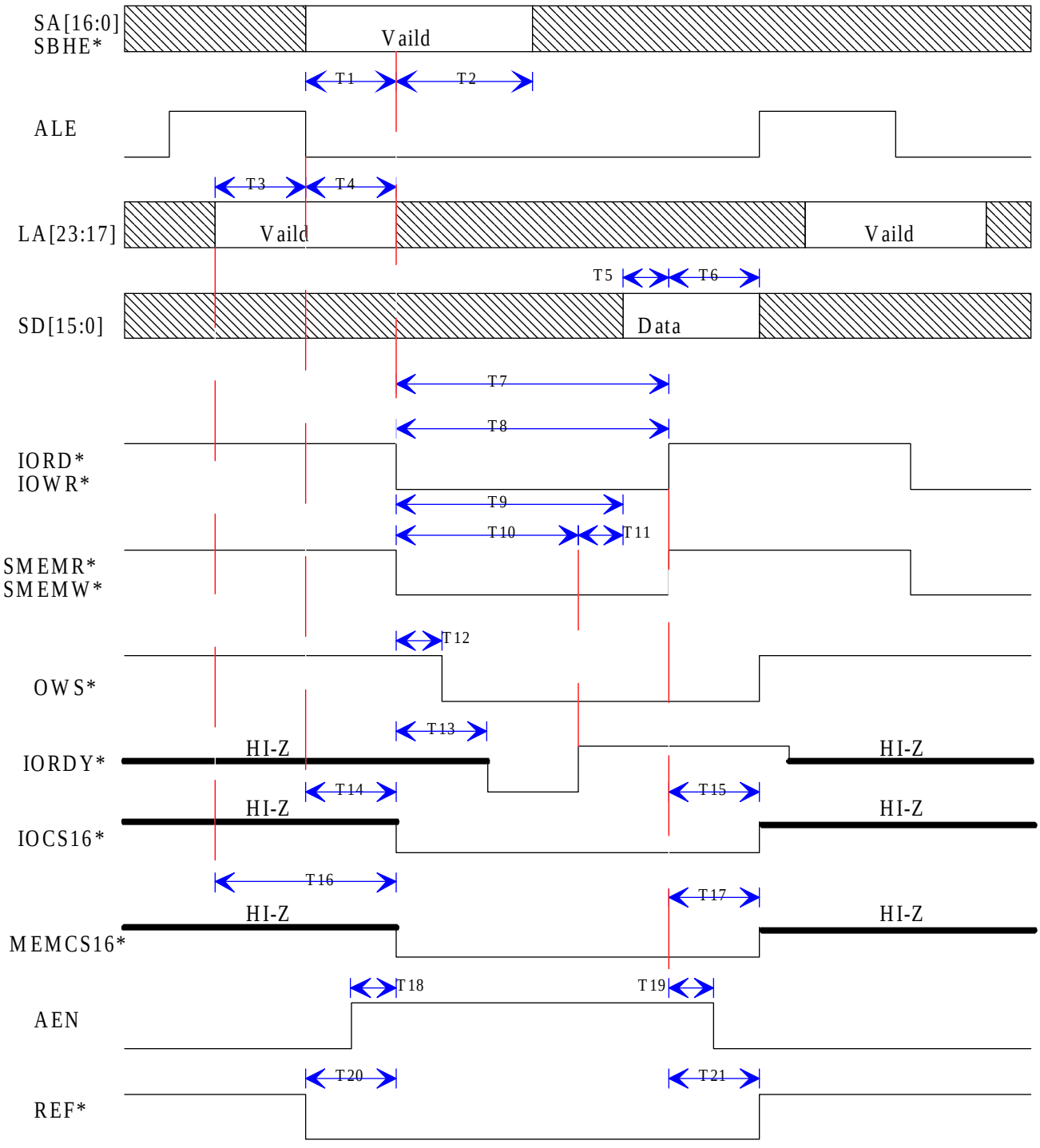
XI. Timing Diagrams

BIOS ROM Read Cycle



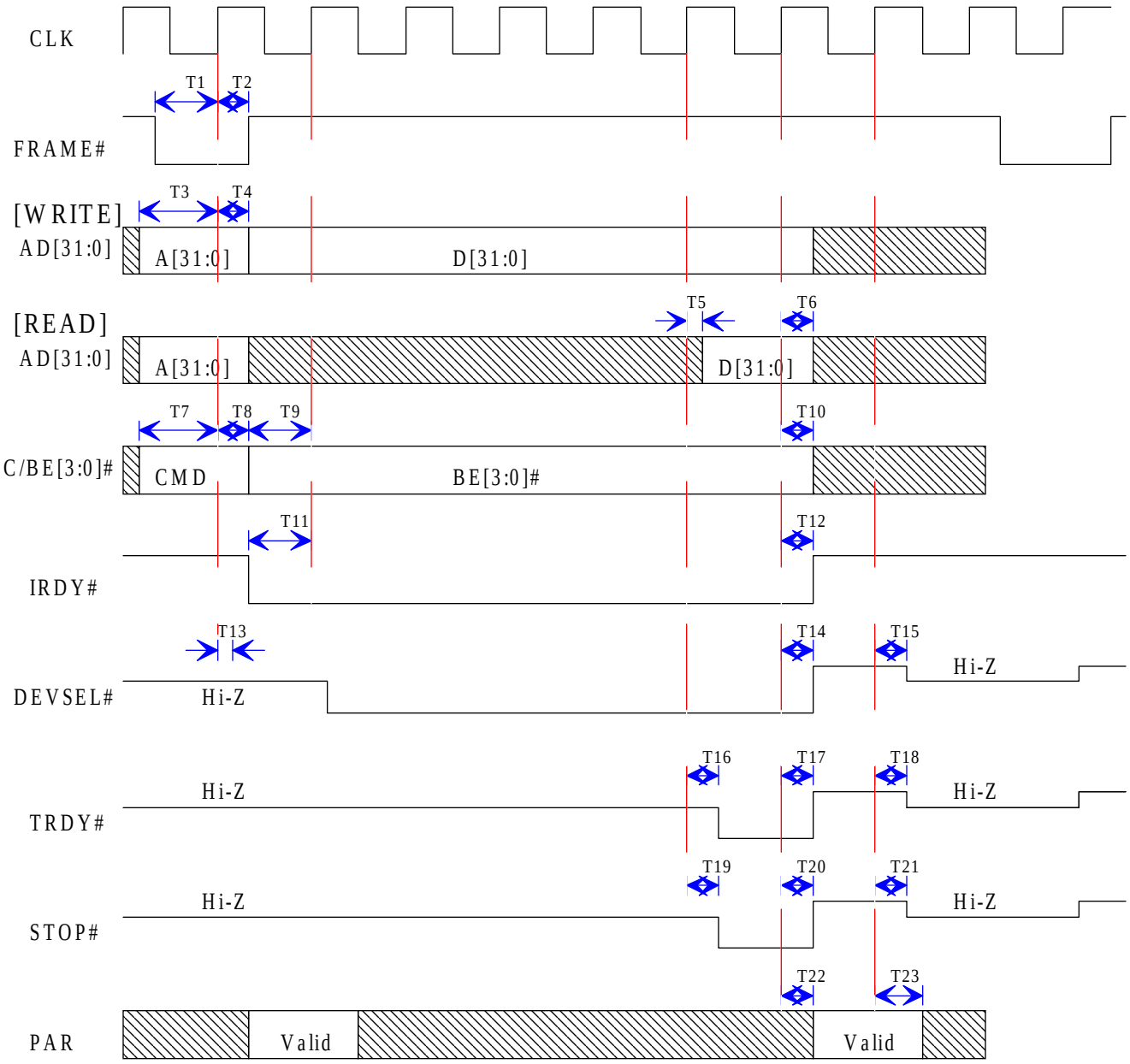
SP508E01.DRW 84/(

ISA Bus Interface Timing



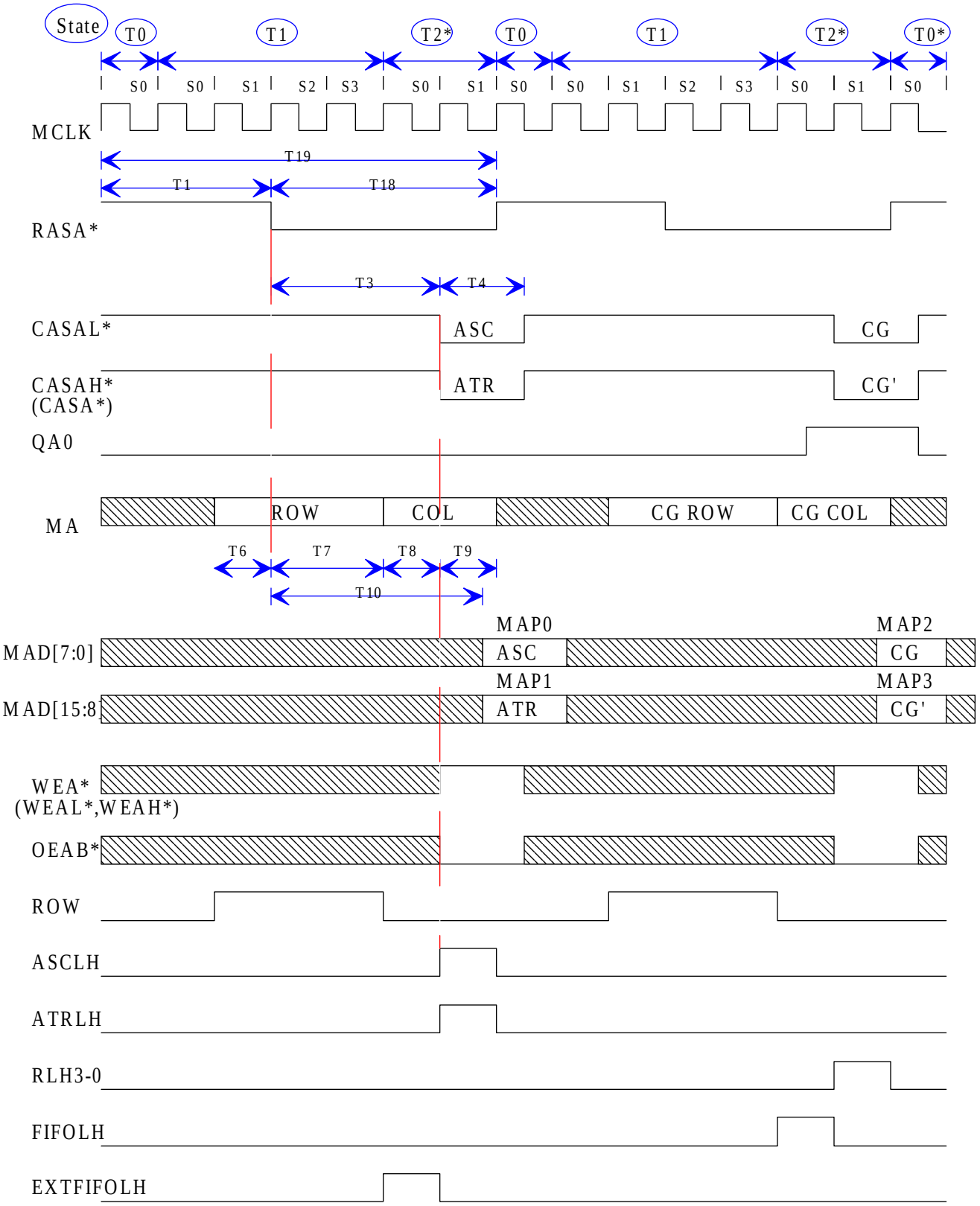
SP508E02.DRW 84/0

PCI Local Bus Interface Timing (32-bit data bus)

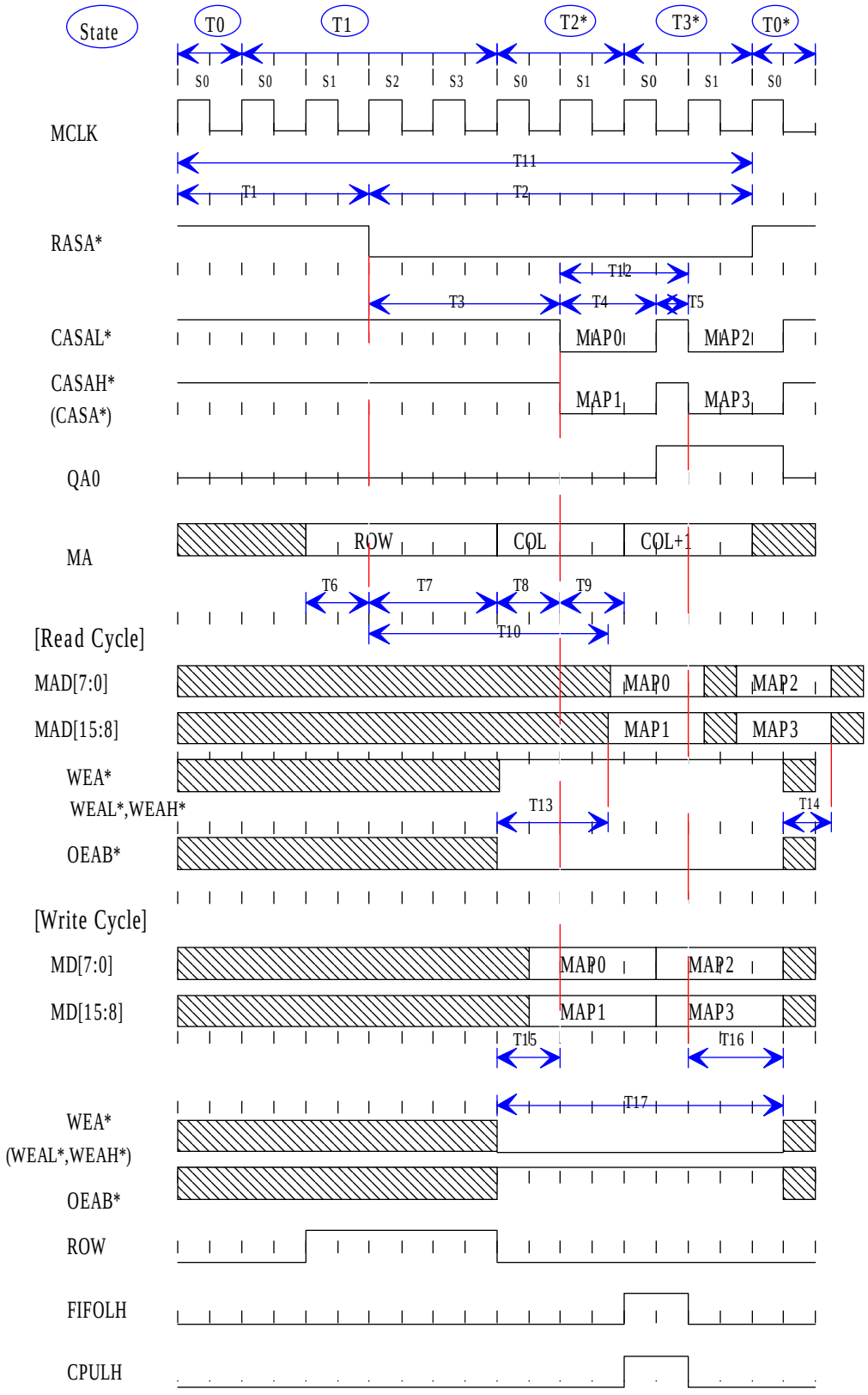


SP508E05.DRW 84/06/

16-Bit TXT CRT Cycle

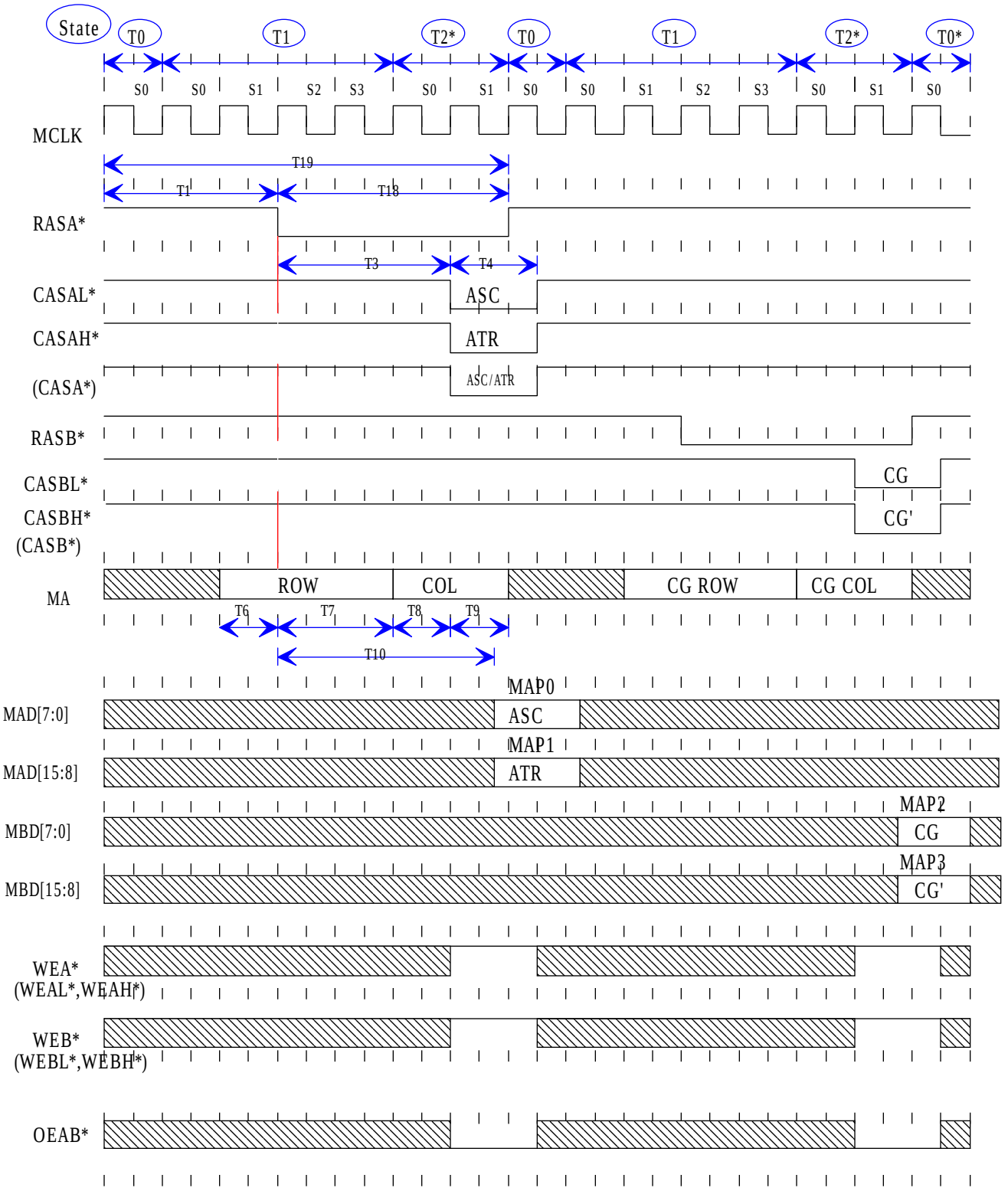


16-Bit CPU/GFX CRT/Shadow Frame Buffer Cycle



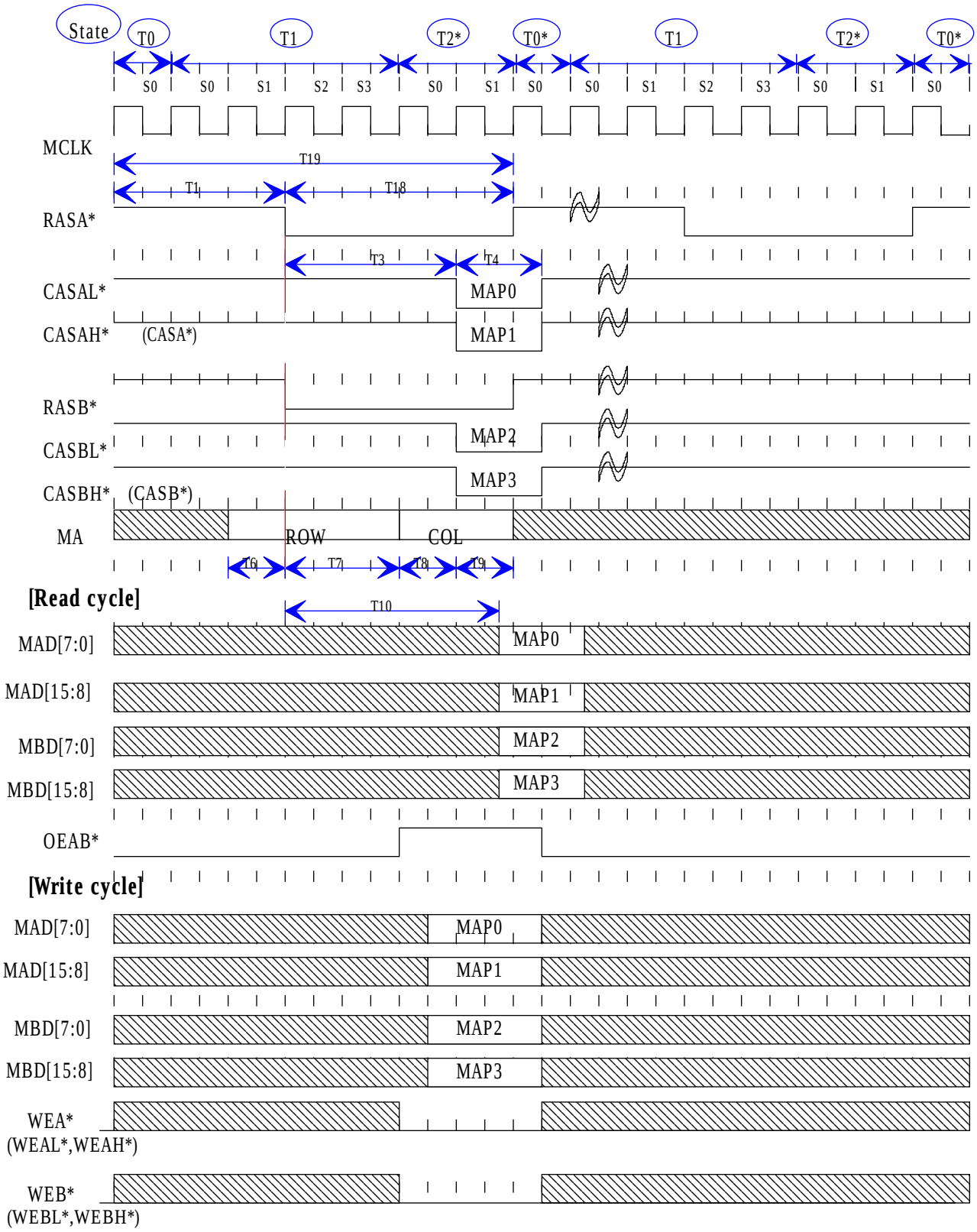
[SP508E07.DRW 84/06/19]

32-Bit TXT CRT Cycle



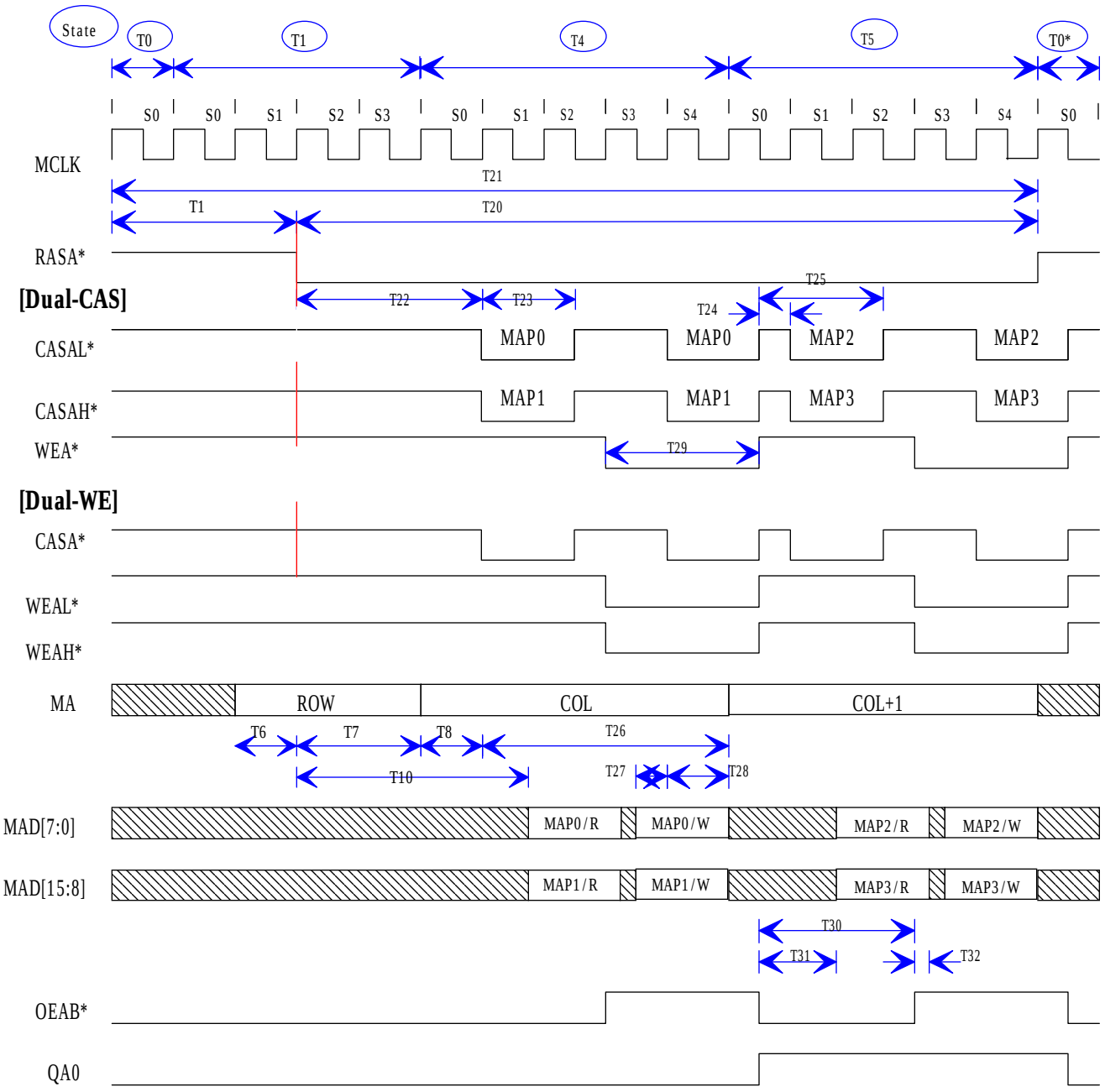
[SP508E08.DRW 84/06/19

32-Bit CPU/GFX CRT/Shadow Frame Buffer Cycle



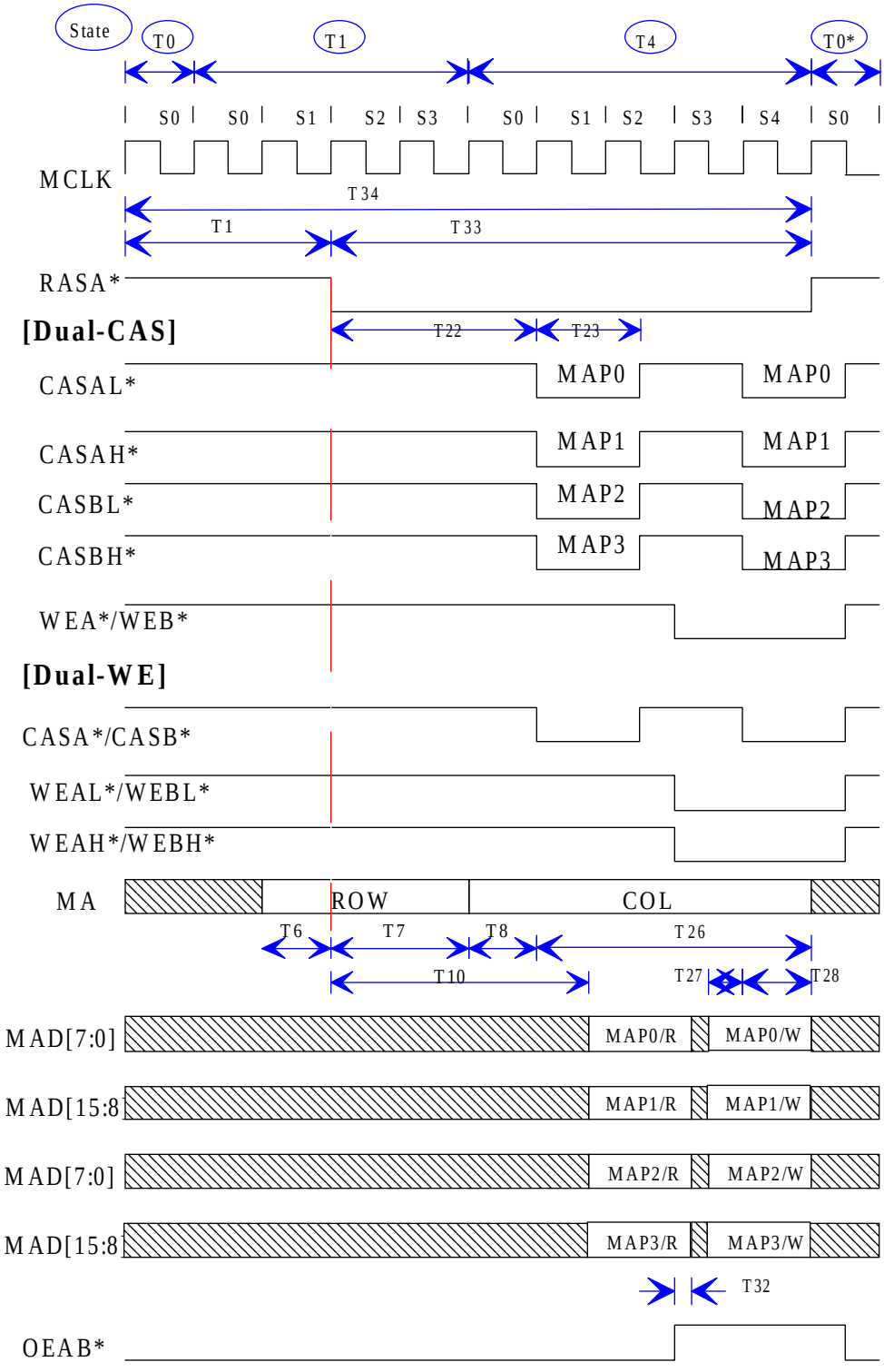
[SP508E09.DRW 84/06/19]

16-Bit Read-Modify-Write Cycle

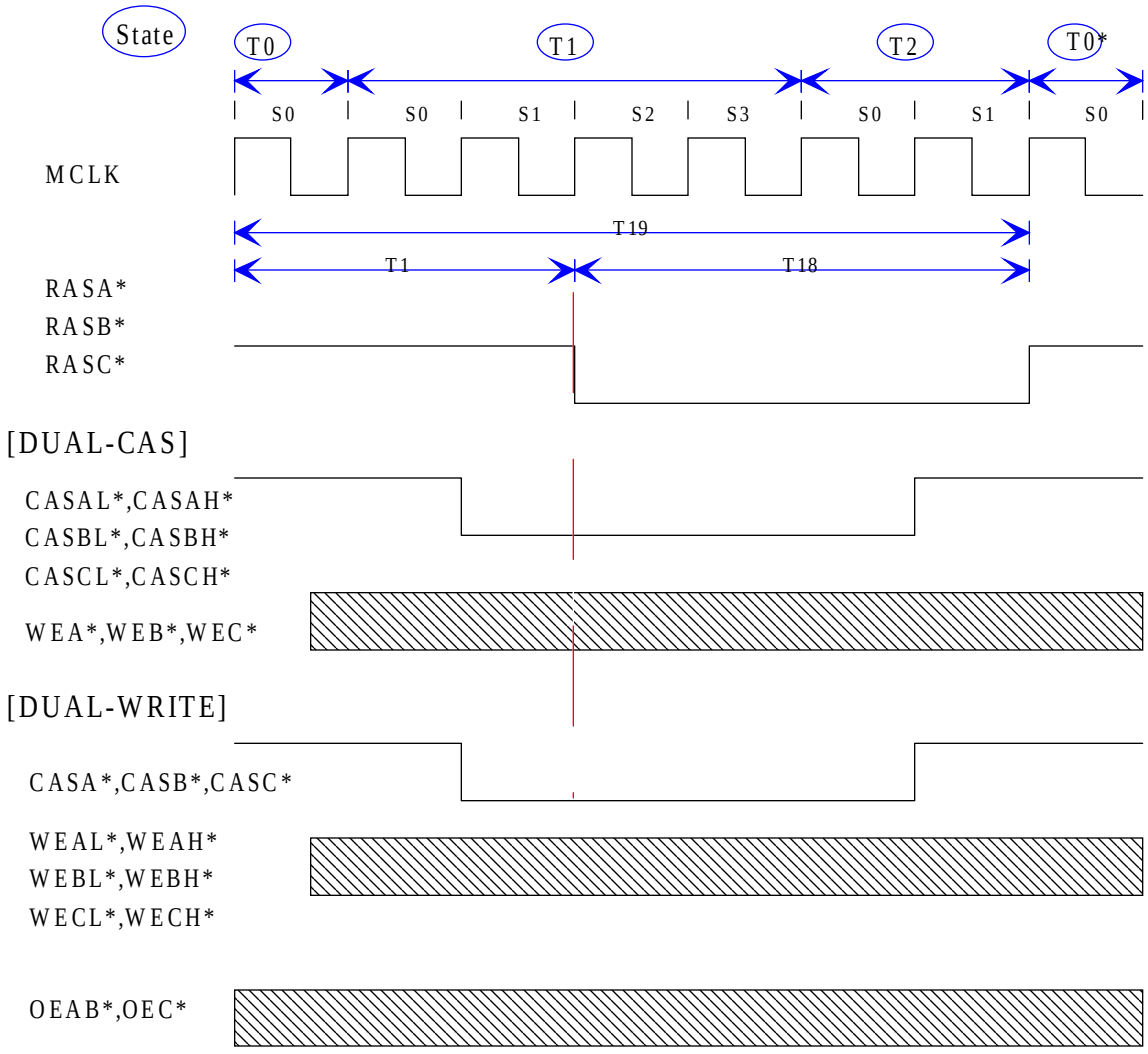


[SP508E10.DRW 84/06/19]

32-Bit Read-Modify-Write Cycle

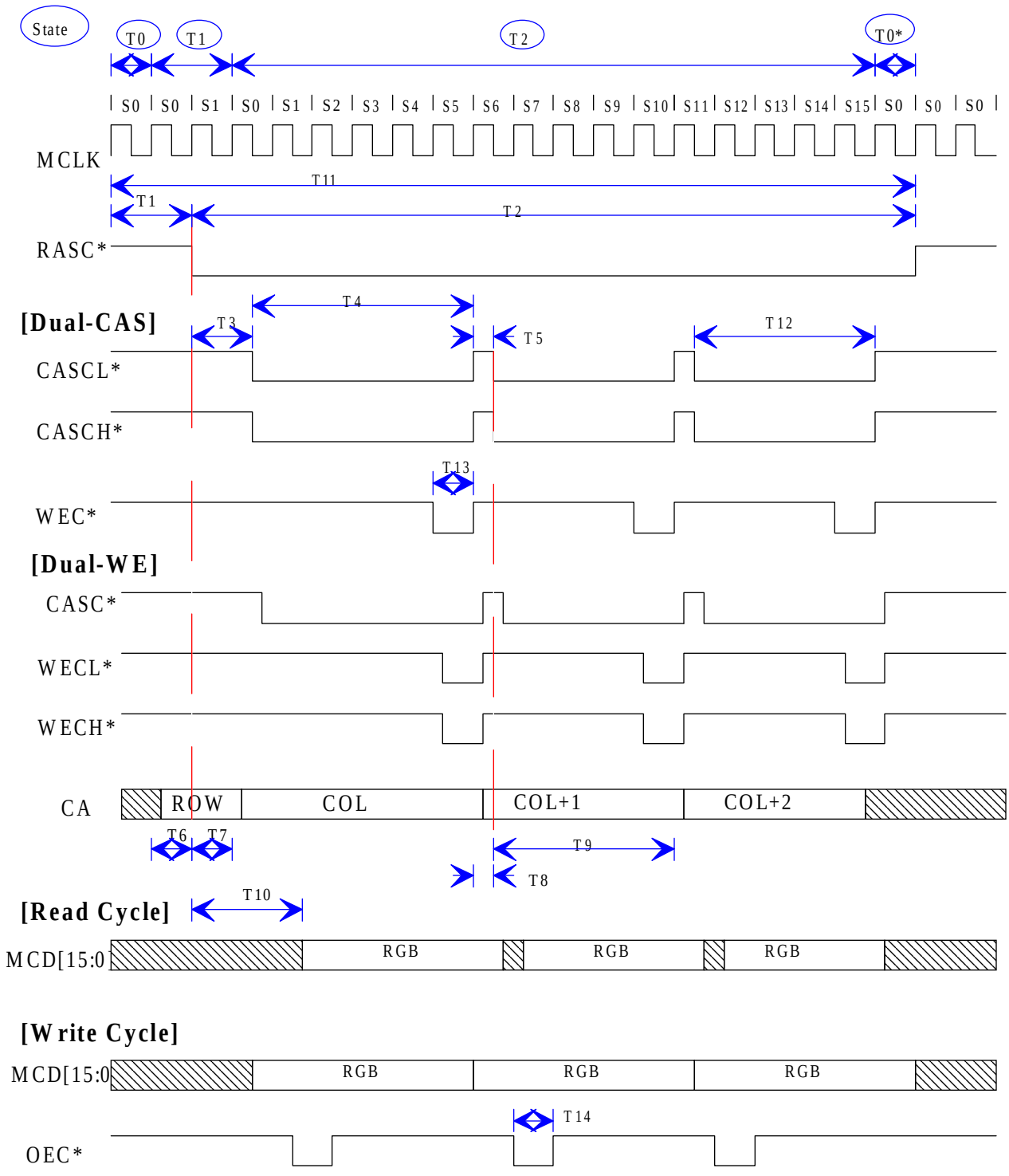


Refresh Cycle Cycle(CAS Before RAS)

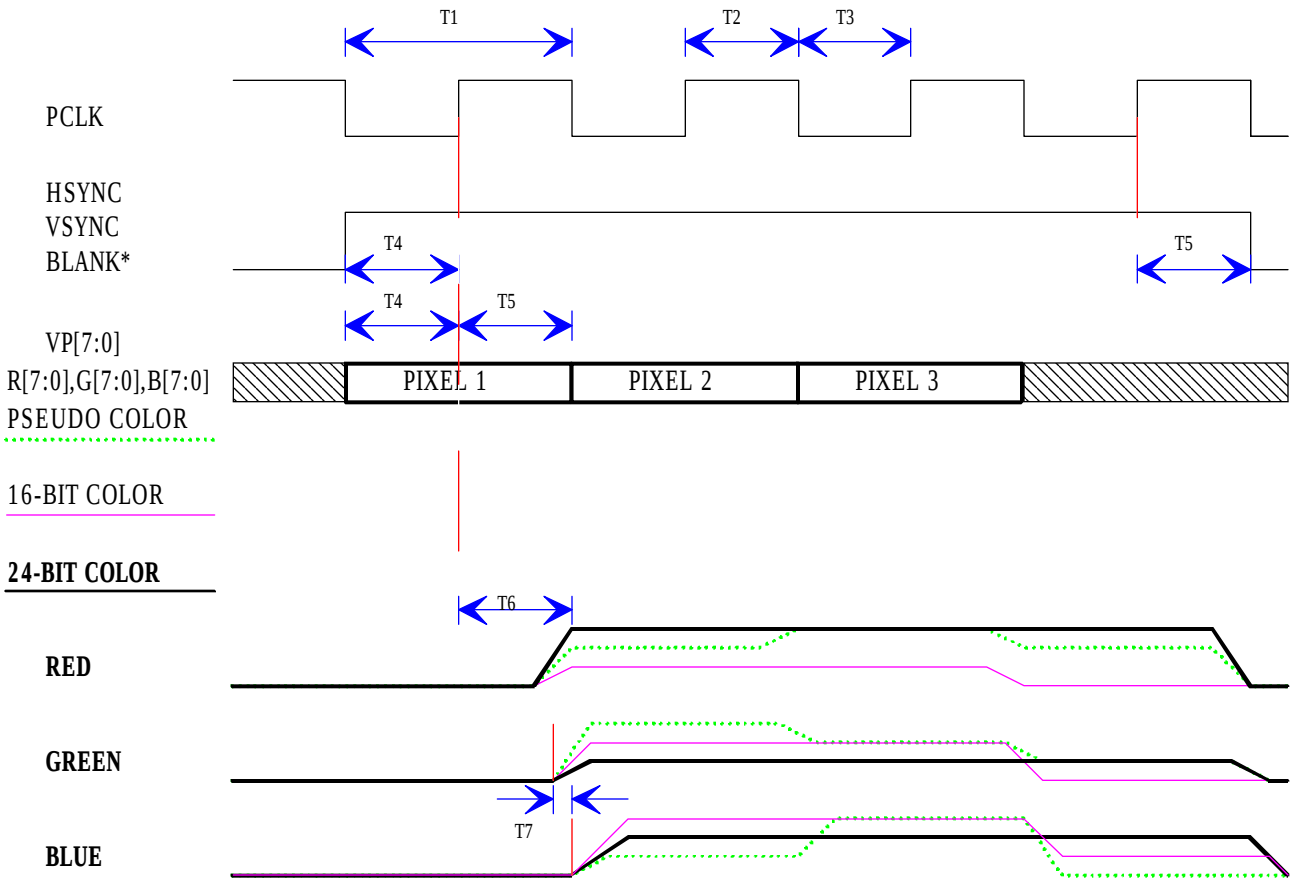


SP508E15.DRW 84/(

External Frame Buffer Interface Timing (16-bit)

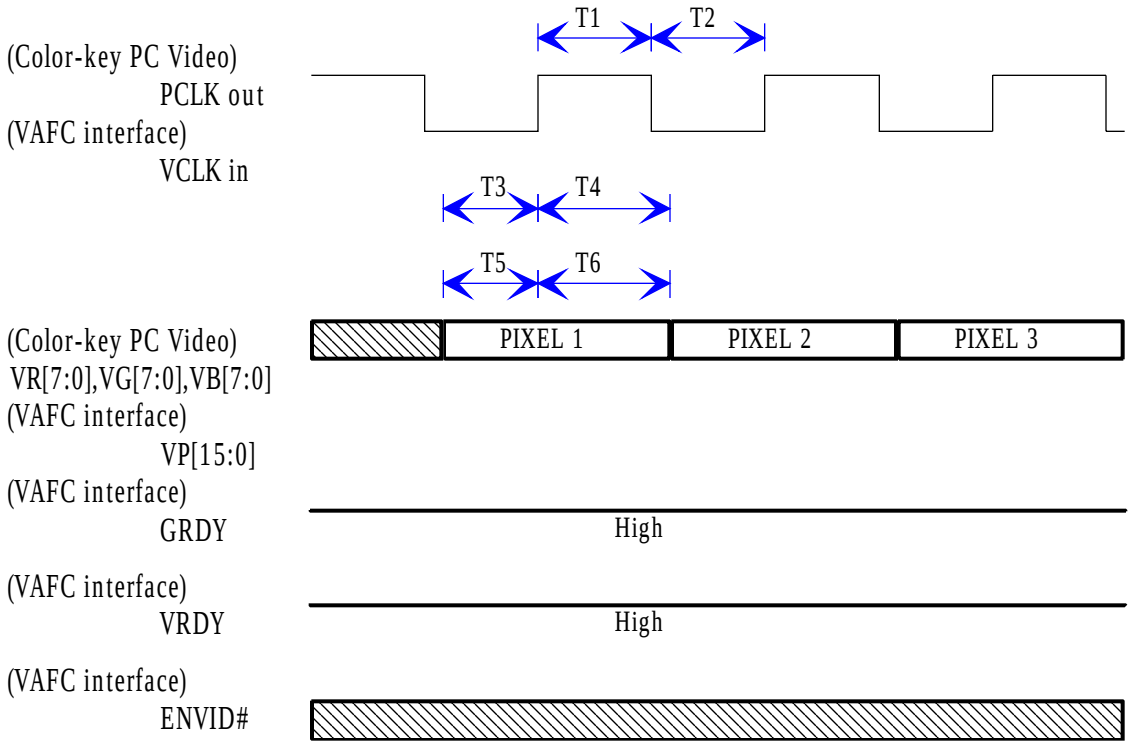


RAMDAC & Feature Connector Interface Timing



[SP508E18.DRW 84/06/2

Color-Key PC Video & VAFC Interface Timing



XII. Appendix

A. Monitor Specification

*** Super VGA Display Monitor Spec.**

Mode	VCLK	HSYNC	VSYNC
IBM 320x , 640x	25.175MHz	31.5KHz	70Hz
IBM 360x , 720x	28.322MHz	31.5KHz	70Hz
TXT 132x25(Font 8x16,8x14)	40MHz	31.5KHz	60Hz
TXT 132x44(Font 8x8)	40MHz	31.5KHz	70Hz
640x400	25.175MHz	31.5KHz	70Hz
640x480	25.175MHz	31.5KHz	60Hz
800x600	36MHz	35.156KHz	56.25Hz
1024x768 /Interlaced	44.9MHz	35.52KHz	87Hz
1024x768 /Non-Interlaced	65MHz	48.363KHz	60Hz
1280x1024 /Interlaced	75MHz	46.875KHz	87Hz
1280x1024 /Non-Interlaced	102.4MHz	64KHz	60Hz
1600x1280 /Interlaced	108MHz	57.447KHz	87Hz

*** VESA VGA Display Monitor Spec**

Mode	VCLK	HSYNC	VSYNC
IBM 320x , 640x	31.5MHz	37.86KHz	84Hz
IBM 360x , 720x	31.5MHz	37.86KHz	84Hz
640x400	31.5MHz	37.86KHz	84Hz
640x480	31.5MHz	37.86KHz	72.8Hz
640x480	31.5MHz	37.5KHz	75Hz
800x600	40MHz	37.879KHz	60.3Hz
800x600	50MHz	48.077KHz	72.2Hz
800x600	49.5MHz	46.875KHz	75Hz
1024x768 /Non-Interlaced	65MHz	48.363KHz	60Hz
1024x768 /Non-Interlaced	75MHz	56.476KHz	70Hz
1024x768 /Non-Interlaced	78.75MHz	60.023KHz	70Hz
1280x1024 /Non-Interlaced	135MHz	79.976KHz	75Hz

B. TP6508 VGA Modes

TP6508 VGA Modes

Mode	Display Size	Type	Colors /Shades	Alpha Format	Buff Start	Box Size	VCLK (MHz)	HSync (KHz)	VSync (Hz)	Min. Memory Size	Max. Page
0 / 1	320x200	A/N	16/256K	40X25	B80	8X8	25.17	31.5	70	256KB	8
0*/1*	320x350	A/N	16/256K	40X25	B80	8X14	25.17	31.5	70	256KB	8
0+/1	360x400	A/N	16/256K	40X25	B80	9X16	28.32	31.5	70	256KB	8
2 / 3	640x200	A/N	16/256K	80X25	B80	8X8	25.17	31.5	70	256KB	8
2*/3*	640x350	A/N	16/256K	80X25	B80	8X14	25.17	31.5	70	256KB	8
2+/3	720x400	A/N	16/256K	80X25	B80	9X16	28.32	31.5	70	256KB	8
4 / 5	320x200	APA	4/256K	40X25	B80	8X8	25.17	31.5	70	256KB	1
6	640x200	APA	2/256K	80X25	B80	8X8	25.17	31.5	70	256KB	1
7	720x350	A/N	Mono	80X25	B00	9X14	28.32	31.5	70	256KB	8
7+	720x400	A/N	Mono	80X25	B00	9X16	28.32	31.5	70	256KB	8
D	320x200	APA	16/256K	40X25	A00	8X8	25.17	31.5	70	256KB	8
E	640x200	APA	16/256K	80X25	A00	8X8	25.17	31.5	70	256KB	4
F	640x350	APA	Mono	80X25	A00	8X14	25.17	31.5	70	256KB	2
10	640x350	APA	16/256K	80X25	A00	8X14	25.17	31.5	70	256KB	2
11	640x480	APA	2/256K	80X30	A00	8X16	25.17	31.5	60	256KB	1
12	640x480	APA	16/256K	80X30	A00	8X16	25.17	31.5	60	256KB	1
13	320x200	APA	256/256	40X25	A00	8X8	25.17	31.5	70	256KB	1
20	1056x400	A/N	16/256K	132X25	B80	8X16	40	30.9	60	256KB	4
21	1056x396	A/N	16/256K	132X44	B80	8X8	40	30.9	70	256KB	2
22	1056x400	A/N	16/256K	132X25	B80	8X14	40	30.9	70	256KB	4
23	1600x1280/I	APA	256/256	200X80	A00	8X16	108	57.44	87	2MB	1
24	1600x1280/	APA	256/256	200X80	A00	8X16	166.6	79.2	60	2MB	1
25	1600x1280/I	APA	65536	200X80	A00	8X16	108	57.44	87	4MB	1
26	1600x1280/	APA	65536	200X80	A00	8X16	166.6	79.2	60	4MB	1
27	1600x1280/	APA	16/256K	200X80	A00	8X16	166.6	79.2	60	1MB	1
28	800x600	APA	16/256K	100X37	A00	8X16	36	35.5	57	256KB	1
29	1024x768/I	APA	16/256K	128X48	A00	8X16	44.9	35.5	87	512KB	1
2A	1024x768/N	APA	16/256K	128X48	A00	8X16	65	48.36	60	512KB	1
2B	640x200	APA	256/256	80X25	A00	8X16	25.17	31.5	70	512KB	1
2C	640x400	APA	256/256	80X25	A00	8X16	25.17	31.5	70	512KB	1
2D	640x480	APA	256/256	80X30	A00	8X16	25.17	31.5	60	512KB	1
2E	800x600	APA	256/256	100X37	A00	8X16	36	35.5	57	512KB	1
2F	1024x768/I	APA	256/256	128X48	A00	8X16	44.9	35.5	87	1MB	1
30	1024x768/N	APA	256/256	128X48	A00	8X16	65	48.36	60	1MB	1

[88.04.12 TPMODE1.TBL]

TP6508 VGA Modes

(Continuous)

Mode	Display Size	Typ	Colors /Shades	Alpha Format	Buff Start	Box Size	VCLK (MHz)	HSync (KHz)	VSync (Hz)	Min. Memory size	Max. Page
31	1280x1024/I	APA	1677721	160X64	A00	8X16	75	46.87	87	4MB	1
32	1280x1024/	APA	1677721	160X64	A00	8X16	102.4	64	60	4MB	1
33	1280x1024/I	APA	16/256K	160X64	A00	8X16	75	46.87	87	1MB	1
34	1280x1024/	APA	16/256K	160X64	A00	8X16	135	79.97	75	1MB	1
35	1280x1024/I	APA	256/256	160X64	A00	8X16	75	46.87	87	2MB	1
36	1280x1024/	APA	256/256	160X64	A00	8X16	102.4	64	60	2MB	1
37	1600x1280/I	APA	16/256K	200X80	A00	8X16	129.4	64.7	96	1MB	1
38	640x480	APA	65536	80X30	A00	8X16	25.17	31.5	60	1MB	1
39	800x600	APA	65536	100X37	A00	8X16	36	35.5	56.25	1MB	1
3A	640x480	APA	1677721	80X30	A00	8X16	25.17	31.5	60	1MB	1
3B	800x600	APA	1677721	100X37	A00	8X16	36	35.5	56.25	2MB	1
3C	1024x768/I	APA	65536	128X48	A00	8X16	44.9	35.5	87	2MB	1
3D	1024x768/N	APA	65536	128X48	A00	8X16	65	48.36	60	2MB	1
3E	1024x768/I	APA	1677721	128X48	A00	8X16	44.9	35.5	87	4MB	1
3F	1024x768/N	APA	1677721	128X48	A00	8X16	65	48.36	60	4MB	1
40	1280x1024/I	APA	65536	160X64	A00	8X16	75	46.87	87	4MB	1
41	1280x1024/	APA	65536	160X64	A00	8X16	102.4	64	60	4MB	1

[88.04.12 TPVGAM2.TBL]

<Note> : TP6508 don't support mode 23 , 24 , 25 , 26 , 27 , 3E , 3F , 40 , 41 .

C. Rast Operation Code List

Operation : a : and
o : or
x : xor
n : not

Objects : D : destination
P : pattern
S : source

Boolean function :

in HEX	in R Polish	in HEX	in R Polish
00	0	FF	1
01	DPSoon	FE	DPSoo
02	DPSona	FD	PSDnoo
03	PSon	FC	PSo
04	SDPona	FB	DPSnoo
05	DPon	FA	DPo
06	PDSxnon	F9	PDSxno
07	PDSaon	F8	PDSao
08	SDPnaa	F7	PDSano
09	PDSxon	F6	PDSxo
0A	DPna	F5	PDno
0B	PSDnaon	F4	PSDnao
0C	SPna	F3	PSno
0D	PDSnaon	F2	PDSnao
0E	PDSonon	F1	PDSono
0F	Pn	F0	P
10	PDSona	EF	SDPnoo
11	DSon	EE	DSo
12	SDPxnon	ED	SDPxno
13	SDPaon	EC	SDPao
14	DPSxnon	EB	DPSxno
15	DPSaon	EA	DPSao
16	PSDPSanaxx	E9	DSPDSanaxxn
17	SSPxDSxaxn	E8	SSPxDSxax
18	SPxPDxa	E7	SPxPDxan
19	SDPSanaxn	E6	SDPSanax
1A	PDSPaox	E5	PDSPaoxn
1B	SDPSxaxn	E4	SDPSxax
1C	PSDPaox	E3	PSDPaoxn
1D	DSPDxaxn	E2	DSPDxax
1E	PDSox	E1	PDSoxn
1F	PDSoan	E0	PDSoa
20	DPSnaa	DF	SDPano
21	SDPxon	DE	SDPxo
22	DSna	DD	SDno
23	SPDnaon	DC	SPDnao
24	SPxDSxa	DB	SPxDSxan

25	PDSPanaxn	DA	PDSPanax
26	SDPSaoxxn	D9	SDPSaoxn
27	SDPSxnox	D8	SDPSxax
28	DPSxa	D7	DPSxan
29	PSDPSaoxxn	D6	PSDPSaoxx
2A	DPSana	D5	DPSanan
2B	SSPxPDxaxn	D4	SSPxPDxax
2C	SPDSoax	D3	SPDSoaxn
2D	PSDnox	D2	PDSnax
2E	PSDPxox	D1	PSDPxoxn
2F	PSDnoan	D0	PSDnoa
30	PSna	CF	SPno
31	SDPnaon	CE	SDPnao
32	SDPSoox	CD	SDPono
33	Sn	CC	S
34	SPDSaox	CB	SPDSaoxn
35	SPDSxnox	CA	DPSDxax
36	SDPox	C9	SPDoxn
37	SDPoan	C8	SDPoa
38	PSDPoax	C7	PSDPoaxn
39	SPDnox	C6	SDPnax
3A	SPDSxox	C5	SPDSxoxn
3B	SPDnoan	C4	SPDnoa
3C	PSx	C3	PSxn
3D	SPDSonox	C2	SPDSonoxn
3E	SPDSnaox	C1	SPDSnaoxn
3F	PSan	C0	PSa
40	PSDnaa	BF	DPSano
41	DPSxon	BE	DPSxo
42	SDxPDxa	BD	SDxPDxan
43	SPDSanaxn	BC	SPDSanax
44	SDna	BB	DSno
45	DPSnaon	BA	DPSnao
46	DSPDaox	B9	DSPDaoxn
47	PSDPxaxn	B8	PSDPxax
48	SDPxa	B7	SDPxan
49	PDSPDoaxxn	B6	PDSPDoaxx
4A	DPSDoax	B5	DPSDoaxn
4B	PDSnox	B4	PSDnax
4C	SDPana	B3	SDPanan
4D	SSPxDSxoxn	B2	SSPxDSxox
4E	PDSPxox	B1	PDSPxoxn
4F	PDSnoan	B0	PDSnoa
50	PDna	AF	DPno
51	DSPnaon	AE	DSPnao
52	DPSDaox	AD	DPSDaoxn

53	SPDSxaxn	AC	SPDSxax
54	DPSonon	AB	DPSono
55	Dn	AA	D
56	DPSox	A9	DPSoxn
57	DPSoan	A8	DPSoa
58	PDSPoax	A7	PDSPoaxn
59	DPSnox	A6	DSPnax
5A	DPx	A5	DPxn
5B	DPSDonox	A4	DPSDonoxn
5C	DPSDxox	A3	DPSDxoxn
5D	DPSnoan	A2	DPSnoa
5E	DPSDnaox	A1	DPSDnaoxn
5F	DPan	A0	DPa
60	PDSxa	9F	PDSxan
61	DSPDSaoxxn	9E	DSPDSaoxx
62	DSPDoax	9D	DSPDoaxn
63	SDPnox	9C	SPDnax
64	SDPSoax	9B	SDPSoaxn
65	DSPnox	9A	DPSnax
66	DSx	99	DSxn
67	SDPSonox	98	SDPSonoxn
68	DSPDSonoxxn	97	DSPDSonoxx
69	PDSxxn	96	PDSxx
6A	DPSax	95	DPSaxn
6B	PSDPSoaxxn	94	PSDPSoaxx
6C	SDPax	93	SDPaxn
6D	PDSPDoaxxn	92	PDSPDoaxx
6E	SDPSnoax	91	SDPSnoaxn
6F	PDSxnan	90	PDSxna
70	PDSana	8F	PDSanan
71	SSDxPDxaxn	8E	SSDxPDxax
72	SDPSxox	8D	SDPSxoxn
73	SDPnoan	8C	SDPnoa
74	DSPDxox	8B	DSPDxoxn
75	DSPnoan	8A	DSPnoa
76	SDPSnaox	89	SDPSnaoxn
77	DSan	88	DSa
78	PDSax	87	PDSaxn
79	DSPDSoaxxn	86	DSPDSoaxx
7A	DPSDnoax	85	DPSDnoaxn
7B	SDPxnan	84	SDPxna
7C	SPDSnoax	83	SPDSnoaxn
7D	DPSxnan	82	DPSxna
7E	SPxDSxo	81	SPxDSxon
7F	DPSaan	80	DPSaa

D. Memory Address Table

CPU Address Multiplexing - Symmetry Addressing

	VGA Mode	Enhance 16 color Mode	Enhance 256/Hi-/Ture Color	Enhance Text Mode
	16-bit / 32-bit	16-bit / 32-bit//*	16-bit / 32-bit	16-bit / 32-bit
CAS-A0	QA0/BANK0	QA0/BANK0//BANK	QA0/BA3	QA0/BANK0
CAS-A1	PG	SA0	BA0	SA5
CAS-A2	CH	SA1	BA1	SA6
CAS-A3	SA2	SA2	SA2	SA7
CAS-A4	SA3	SA3	SA3	SA8
CAS-A5	SA4	SA4	SA4	SA9
CAS-A6	SA5	SA5	SA5	SA10
CAS-A7	SA6	SA6	SA6	SA11
CAS-A8	0	SA169/SA169//BAN	BA2	0
RAS-A0	SA7	SA7	SA7	SA0
RAS-A1	SA8	SA8	SA8	SA1
RAS-A2	SA9	SA9	SA9	SA2
RAS-A3	SA10	SA10	SA10	SA3
RAS-A4	SA11	SA11	SA11	SA4
RAS-A5	SA12	SA12	SA12	SA12
RAS-A6	SA13	SA13	SA13	SA13
RAS-A7	SA14	SA14	SA14	SA14
RAS-A8	SA159	SA15	SA159	SA159

* : Bank addressing for enhanced 16-color display mode

[84.06.12 SP508T06.TBL]

CPU Address Multiplexing - Asymmetry Addressing

	VGA Mode	Enhance 16 color Mode	Enhance 256/Hi-/Ture Color	Enhance Text Mode
	16-bit / 32-bit	16-bit / 32-bit//*	16-bit / 32-bit	16-bit / 32-bit
CAS-A0	QA0/BANK0	QA0/BANK0//BANK	QA0/BA3	QA0/BANK0
CAS-A1	PG	SA0	BA0	SA5
CAS-A2	CH	SA1	BA1	SA6
CAS-A3	SA2	SA2	SA2	SA7
CAS-A4	SA3	SA3	SA3	SA8
CAS-A5	SA4	SA4	SA4	SA9
CAS-A6	SA5	SA5	SA5	SA10
CAS-A7	SA6	SA6	SA6	SA11
CAS-A8	0	0	BA2	0
RAS-A0	SA7	SA7	SA7	SA0
RAS-A1	SA8	SA8	SA8	SA1
RAS-A2	SA9	SA9	SA9	SA2
RAS-A3	SA10	SA10	SA10	SA3
RAS-A4	SA11	SA11	SA11	SA4
RAS-A5	SA12	SA12	SA12	SA12
RAS-A6	SA13	SA13	SA13	SA13
RAS-A7	SA14	SA14	SA14	SA14
RAS-A8	SA159	SA15	SA159	SA159
RAS-A9	0	SA169/SA169//BAN	BA2	0

* : Bank addressing for enhanced 16-color display mode

[84.06.12 SP508T07.TBL]

CRT Address Multiplexing - Symmetry Addressing

	Byte Mode	**Word Mode**	**Double Word Mode**	**IBM Text Mode**	**Enhance Text Mode**
	16-bit / 32-bit	16-bit / 32-bit	16-bit / 32-bit	16-bit / 32-bit	16-bit / 32-bit
CAS-A0	QA0/MA17	QA1/MA17	QA0/MA17	QA1/MA17	QA1/ASC7
CAS-A1	MA0	MA15/MA13	MA14	RA0	ASC0
CAS-A2	MA1	MA0	MA15	RA1	ASC1
CAS-A3	MA2	MA1	MA0	RA2	ASC2
CAS-A4	MA3	MA2	MA1	RA3	ASC3
CAS-A5	MA4	MA3	MA2	RA4	ASC4
CAS-A6	MA5	MA4	MA3	ASC0	ASC5
CAS-A7	MA6	MA5	MA4	ASC1	ASC6
CAS-A8	MA16	MA16	MA16	0	0
RAS-A0	MA7	MA6	MA5	ASC2	RA0
RAS-A1	MA8	MA7	MA6	ASC3	RA1
RAS-A2	MA9	MA8	MA7	ASC4	RA2
RAS-A3	MA10	MA9	MA8	ASC5	RA3
RAS-A4	MA11	MA10	MA9	ASC6	RA4
RAS-A5	MA12	MA11	MA10	ASC7	0
RAS-A6	MA13/RA0	MA12/RA0	MA11/RA0	CHHAP2	CHHAP2
RAS-A7	MA14/RA1	MA13/RA1	MA12/RA1	CHHAP0	CHHAP0
RAS-A8	MA15	MA14	MA13	CHHAP1	CHHAP1

[84.06.13 SP508T08.TBL]

CRT Address Multiplexing - Asymmetry Addressing

	Byte Mode	Word Mode	Double Word Mode	IBM Text Mode	Enhance Text Mode
	16-bit / 32-bit	16-bit / 32-bit//*	16-bit / 32-bit	16-bit / 32-bit	16-bit / 32-bit
CAS-A0	QA0/MA17	QA1/MA17	QA0/MA17	QA1/MA17	QA1/ASC7
CAS-A1	MA0	MA15/MA13	MA14	RA0	ASC0
CAS-A2	MA1	MA0	MA15	RA1	ASC1
CAS-A3	MA2	MA1	MA0	RA2	ASC2
CAS-A4	MA3	MA2	MA1	RA3	ASC3
CAS-A5	MA4	MA3	MA2	RA4	ASC4
CAS-A6	MA5	MA4	MA3	ASC0	ASC5
CAS-A7	MA6	MA5	MA4	ASC1	ASC6
CAS-A8	0	0	0	0	0
RAS-A0	MA7	MA6	MA5	ASC2	RA0
RAS-A1	MA8	MA7	MA6	ASC3	RA1
RAS-A2	MA9	MA8	MA7	ASC4	RA2
RAS-A3	MA10	MA9	MA8	ASC5	RA3
RAS-A4	MA11	MA10	MA9	ASC6	RA4
RAS-A5	MA12	MA11	MA10	ASC7	0
RAS-A6	MA13/RA0	MA12/RA0	MA11/RA0	CHHAP2	CHHAP2
RAS-A7	MA14/RA1	MA13/RA1	MA12/RA1	CHHAP0	CHHAP0
RAS-A8	MA15	MA14	MA13	CHHAP1	CHHAP1
RAS-A9	MA16	MA16	MA16	0	0

[84.06.13 SP508T09.TBL]

BA0 to BA4 Selection Table

	Bank Addressing mode	Linear Addressing mode
BA0	BANK0	SA16
BA1	BANK1	SA17
BA2	BANK2	SA18
BA3	BANK3	SA19
BA4	BANK4	SA20

[84.06.26 SP508T10.TBL]

PG*,CH*,SAA* Table

EXTMEM	ODD/EVEN	EGA/128K	VGA CHAIN4	PG*	CH*	SAA*
X	0	X	0	SA0	-	-
0	1	0	0	SA14	-	-
1	1	1	0	SA16	-	-
1	1	0	0	/PAGBIT	-	-
X	X	X	1	0	-	-
Byte mode				BA2/BA3**	-	-
-	-	-	0	-	SA1	-
-	-	-	1	-	0	-
Word Mode					BA2/BA3**	-
				-	-	SA2
Dword Mode				-	-	BA2/BA3**

EXTMEM : Sequencer Register indexed hex 04 bit 1

ODD/EVEN : Graphics Control Register indexed hex 06 bit 1

VGA CHAIN4 : Sequencer Register indexed hex 04 bit 3

EGA128K : 1- Graphics Control Register indexed hex 06 bit 2=0 and bit 3=0

0- Graphics Control Register indexed hex 06 bit 2=1 and bit 3=1

PAGBIT : Miscellaneousn Output Register bit 5

** : 256K 64-bit bus--BA2 , 512k 64-bit bus--BA3

[84.09.08 SP508T11.TBL]

E. MCLK & VCLK Frequency Programming Table

TP6508 VGA VCLK Synthesizer Parameter Table

VCLK SPEC.	VCLK Frequenc	O	N	D	P	REG. 22/C3h 23/C4h	REG. 24/C5h 25/C6h	HM8694-304	
25.175	**25.165**	1	1C	41	1	9C	83	00,00	0
25.267	**25.2671**	1	E	10	0	8E	20		
28.322	**28.2991**	1	29	54	1	A9	A9	00,01	1
28.636	**28.636**	1	14	29	1	94	53	00,01	1
31.5	**31.4996**	1	A	9	1	8A	12	10,10	A
32.514	**32.5188**	1	42	3A	0	C2	74	00,10	2
34	**33.8425**	1	0C	A	0	8C	14		
35	**34.9996**	1	0A	8	0	8A	10		
36	**35.9995**	1	E	B	0	8E	16	00,11	3
40	**39.9823**	1	F	16	1	8F	2D	01,00	4
44.9	**44.9065**	1	A	6	0	8A	0C	01,01	5
49.5	**49.5325**	1	12	A	0	92	14		
50	**50.3299**	1	39	20	0	B9	40	01,10	6
56.644	**56.5982**	0	53	54	1	53	A9	11,00	C
57.272	**57.272**	0	47	47	1	47	8F		
58.8	**58.7993**	0	4C	4A	1	4C	95	10,11	B
65	**65.0115**	0	18	15	1	18	2B	01,11	7
70	**69.9991**	0	2B	23	1	2B	47		
75	**75.0461**	0	10	C	1	10	19	11,01	D
78.75	**78.749**	0	A	3	0	0A	06		
85	**84.8853**	0	52	37	1	52	6F	11,10	E
90	**89.9989**	0	4C	30	1	4C	61		
94.5	**94.4988**	0	41	27	1	41	4F		
100	**99.9214**	0	51	2E	1	51	5D		
102.4	**102.3954**	0	18	6	1	18	0C		
108	**107.9986**	0	10	8	1	10	11		
110	**110.023**	0	48	25	1	48	4B		
115	**114.544**	0	11	8	1	11	11		
120	**119.7985**	0	2B	14	1	2B	29		
129.4	**129.3923**	0	2A	12	1	2A	25		
135	**134.998**	0	20	6	0	20	0C		

TP6508 VGA MCLK Synthesizer Parameter Table

MCLK SPEC.	MCLK Frequenc	O	N	D	P	REG. 26/C9h	REG. 27/CAh
30MHz	**29.9996**	1	24	3E	1	A0	7D
33MHz	**33.0042**	1	21	3A	1	A1	75
36MHz	**36.0259**	1	26	3D	1	A6	7B
40MHz	**39.9823**	1	24	34	1	A4	69
45MHz	**44.9994**	1	20	29	1	A0	53
50MHz	**49.9294**	1	21	26	1	A1	4D
55MHz	**54.9993**	0	78	3E	0	78	7C
60MHz	**59.9992**	0	41	3E	1	41	7D
65MHz	**64.9817**	0	3A	33	1	3A	67
68MHz	**68.0105**	0	38	2F	1	38	5F
69MHz	**69.9867**	0	34	2B	1	34	57
70MHz	**69.9991**	0	41	35	1	41	6B
71MHz	**70.9675**	0	38	2D	1	38	5B
72MHz	**72.0519**	0	4D	3D	1	4D	7B
73MHz	**72.9937**	0	40	32	1	40	65
74MHz	**74.0345**	0	34	28	1	34	51
75MHz	**74.9743**	0	47	36	1	47	6D
78MHz	**77.9874**	0	3F	2E	0	3F	5D
80MHz	**80.034**	0	6C	26	0	6C	4C
82MHz	**82.0383**	0	34	34	1	34	49
85MHz	**85.0898**	0	33	22	1	33	45
88MHz	**88.0033**	0	3E	28	1	3E	51
90MHz	**89.9989**	0	36	22	1	36	45
95MHz	**94.9877**	0	43	28	1	43	51
100MHz	**99.893**	0	4A	2A	1	4A	55

[88.04.12 TPVGAM2.TBL]

F. Pins Selection Configuration

*1. Disable internal dual frequency synthesizer

(SREG D0 D4 = 0)

PIN Name	PIN Number	Selected Multipelx Function
OFF	178	EXVCLK ~ External VCLK input
XTAL1	203	EXMCLK ~ External MCLK input

*2. VGA BIOS ROM interface

(SREG D0 D2-0 = 101) ~ ISA Bus

PIN Name	PIN Number	Selected Multipelx Function
ROMCS*	29	BIOS ROM chip_select signal output

*3. OFF pin control selection (Pin Number =178)

(if SREG CE D0 = 1 & if *1 isn't true) ~ SREG CB D1-0 = selection bits

D1	D0	Selected Multipelx Function
0	0	VESA DPMS OFF mode pin trigger input/output pin
0	1	Output internal MCLK frequency signal
1	x	Output internal VCLK frequency signal

*4. 24-bit TFT panel interface selection

(CREG AC D5 = 1)

PIN Name	PIN Number	Selected Multipelx Function
CA[7:0]	97-90	P[23:16] ~ Flat panel data signals

*5. Video interface selection

[a]. (SREG D9 D1-0 = 01) ~ 18-bit video port interface

PIN Name : RASC* , WEC*, CASCH*, CASCL* , MCD[15:0]

Selected Multipelx Function : KEY , PCLK , VR[7:2] ,VG[7:2] , VB[7:2]

[b]. (SREG D9 D1-0 = 11 , SREG D0 D6 = 1) ~ 24-bit video port interface

PIN Name : RASC* , CASCH*, CASCL* , WEC*, MCD[15:0] , OEC* , 32KHZ , CA8 , CA9 , A27 , A26

Selected Multipelx Function : KEY , PCLK , VR[7:2] ,VG[7:2] , VB[7:2] , VR[1,0] , VG[1,0] , VB[1:0]

[c]. (SREG D9 D0 = 0 , SREG D0 D6 = 1 , SREG C0 D6=1) ~ VAFC interface

PIN Name : RASC* , CASCH*, CASCL* , WEC*, MCD[15:0] , OEC* , 32KHZ , CA8 , CA9 , A27 , A26

Selected Multipelx Function : VRDY , PCLK , GRDY , EVID# , VP[15:0] , VCLK , BLANK*

*6. External LCD frame buffer interface selection

(if *4,*5 isn't true)

PIN Name : RASC* , CASCH*, CASCL* , WEC*, MCD[15:0] , OEC* , CA[9:0]

Selected Multipelx Function : External LCD frame buffer DRAM interface

*7. ACTI & FPBACK output selection

(CREG D0 D6 = 1 , & if *5 [b])

PIN Name	PIN Number	Selected Multipelx Function
A26	53	ACTI ~ responses high during valid VGA access
A27	54	FPBACK ~ Flat panel power control signal output

*8. Pin-61 output control

(SREG D1 D4 = selection bit)

D7	Selected Multipelx Function
0	FPVEE ~ Flat panel power control signal output
1	FPBACK ~ Flat panel power control signal output