PM5945

SONET
ATM PHYSICAL INTERFACE
BOARD

CONTENTS

OVERVIEW

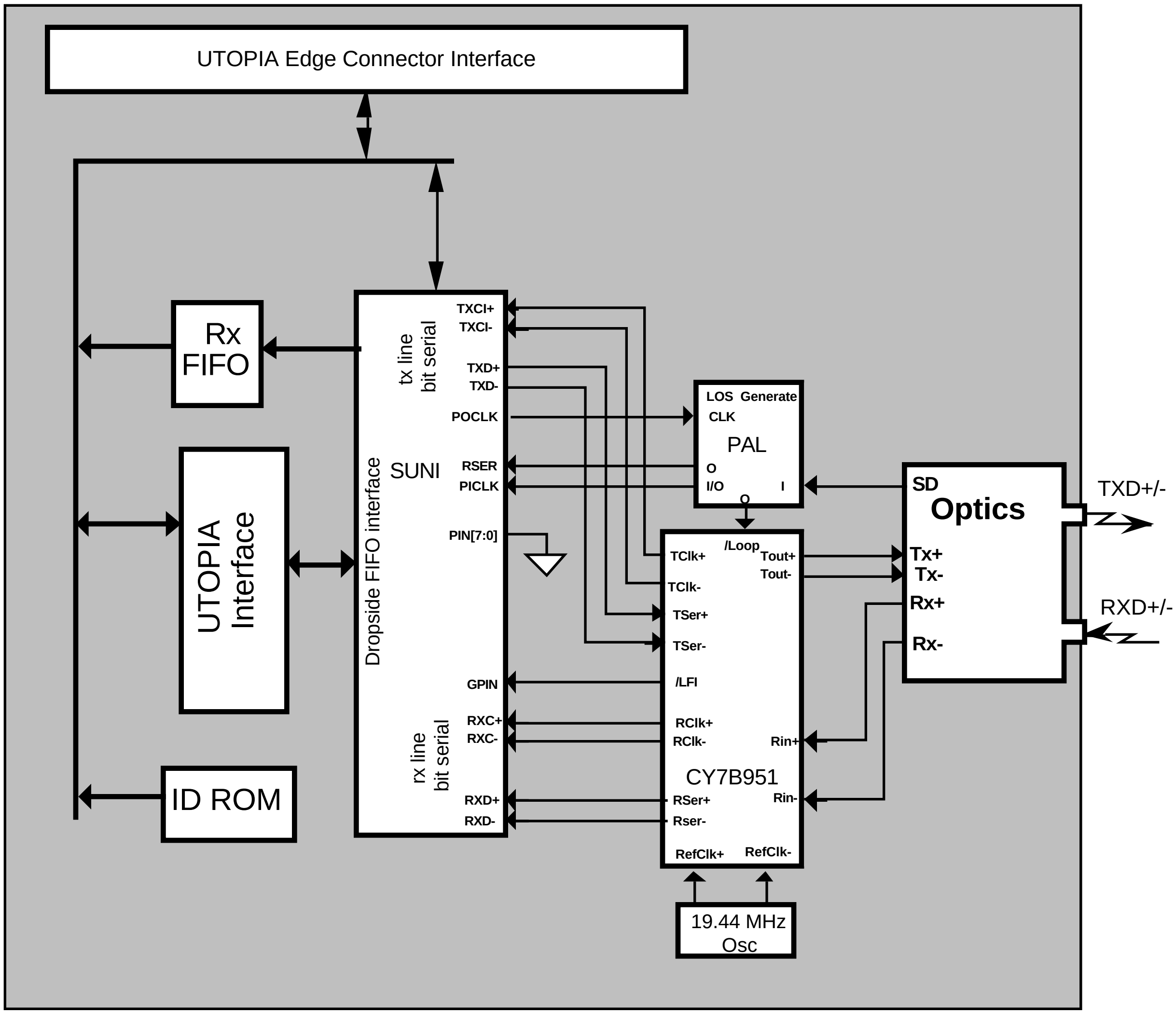
The PM5945 SAPI daughter board contains the PMC PM5345 SUNI-155 (SATURN User Network Interface), the Cypress CY7B951 SONET/SDH Serial Transceiver (a clock and data recovery and clock synthesis unit), and optical PMD in a complete optical ATM (Asynchronous Transfer Mode) physical interface. The SUNI is an ATM physical layer processor for a SONET STS-3C transmission system. This daughter board has been designed to mate with National Semiconductor Corporation's Vicksburg EISA adapter motherboard to form a complete evaluation system. The SAPI daughter board is configured, monitored, and powered through a 100 pin edge connector that mates with the Vicksburg motherboard. The motherboard provides all of the software and decoding logic necessary to directly access all of the registers on the SAPI board.

The SAPI line side interface uses any 9-pin duplex SC receptacle. The optical Transceiver PMD device runs at 155.52 MHz. On the receive side, the receive optical PMD connects to the clock and data recovery section of the Cypress SONET/SDH Serial Transceiver (CY7B951). The output of the CY7B951 is ac-coupled to the SUNI's bit serial input. On the transmit side, the SUNI's PECL data outputs connect directly to the Cypress CY7B951 serial input which buffers the data and outputs the data directly to the transmit optics. The CY7B951 can mux the output data to the input of the PLL and transfer back the recovered clock and data to the input of the SUNI for diagnostic purposes.

The SAPI drop side interface uses a 100 pin edge connector. The 22V10 PLDs transform the SUNI drop side signals to comply with the UTOPIA like signals of the Vicksburg motherboard. The receive drop side also incorporates an additional FIFO, as the internal 4 cell FIFO of the SUNI device is insufficient to handle the latency time between burst cell reads by the R-FRED device on the Vicksburg motherboard.

FUNCTIONAL DESCRIPTION

Block Diagram



SUNI

The SUNI is a monolithic integrated circuit that implements the SONET/SDH processing and ATM mapping functions of a 155 Mbit/s SONET STS-3c User Network Interface. It is the heart of the SAPI board; all traffic goes through the SUNI. On the line side, the SUNI transmits SONET frames through the line interface and receives frames from the line interface. On the drop side, the SUNI sinks cells provided by the buffer interface and sources cells to the buffer interface. Below, the SUNI is briefly described.

The SUNI receives SONET/SDH frames via a bit serial interface, and processes section, line, and path overhead. It performs framing (A1, A2), descrambling, detects alarm conditions, and monitors section, line, and path bit interleaved parity (B1, B2, B3), accumulating error counts at each level for performance monitoring purposes. Line and path far end block error indications (FEBE) are also accumulated. The SUNI interprets the received payload pointers (H1, H2) and extracts the synchronous payload envelope which carries the received ATM cell payload.

The SUNI frames to the ATM payload using cell delineation. Header check sequence (HCS) error correction is provided. Idle/unassigned cells may be dropped according to a programmable filter. Cells are also dropped upon detection of an Uncorrectable HCS error. The ATM cell payloads are descrambled. The ATM cells that are passed are written to a four cell FIFO buffer. The received cells are read from the FIFO using a generic 8-bit wide datapath interface. Counts of received ATM cell headers that are erred and uncorrectable, and also those that are erred and correctable, are accumulated independently for performance monitoring purposes.

The SUNI transmits SONET/SDH frames via a bit serial interface, and formats section, line, and path overhead bytes appropriately. It performs framing pattern insertion (A1, A2), scrambling, alarm signal insertion, and inserts section, line, and path bit interleaved parity (B1, B2, B3) as required to allow performance monitoring at the far end. Line and path far end block error indications (FEBE) are also inserted. The SUNI generates the payload pointer (H1, H2) and inserts the synchronous payload envelope which carries the ATM cell payload. The SUNI also supports the insertion of a large variety of errors into the transmit stream, such as framing pattern errors, bit interleaved parity errors, and illegal pointers, which are useful for system diagnostics and tester applications.

Transmit ATM cells are written to an internal four cell FIFO using a generic 8-bit wide datapath interface. Idle/unassigned cells are automatically inserted when the internal FIFO contains less than one cell. The SUNI provides generation of the header check sequence and scrambles the payload of the ATM cells. Each of these transmit ATM cell processing functions can be enabled or bypassed.

The SUNI is configured, controlled and monitored via the UTOPIA interface to the Vicksburg motherboard.

For a complete description of the SUNI, please refer to PMC-Sierra's PM5345 datasheet.

CY7B951

The Cypress SONET/SDH Serial Transceiver is an integrated SONET clock and data recovery/clock synthesis device. The internal receive PLL recovers a 155.52 MHz clock from a incoming NRZ or NRZI data and re-times the data. The receive PLL uses the reference clock (19.44 MHz) to provide a 155.52 MHz clock in the absence of input data. The reference clock is also used to improve PLL lock time. The differential input data is re-timed by the recovered clock and presented as the PECL differential output data.

The transmit section of the SONET/SDH Serial Transceiver contains a PLL that takes a reference clock and multiplies it by 8 to produce a 155.52 MHz PECL differential output clock. The transmit PECL differential input pair are used to buffer the transmit PECL output of the SUNI. This input can also be muxed into the receive side PLL for clock and data recovery (used for diagnostic purposes).

Line Interface

The receive line interface consists of receive optics connected to a clock and data recovery unit. To ensure that there is a clock in the absence of incoming light, the signal detect (SD) output of the optics is used to select between the serial and parallel mode of operation on the receive side of the SUNI device. In normal operation (good incoming signal) the SUNI device is in the serial mode and accepts clock and data from the high speed interface (RSER is high). In loss of signal condition, the SUNI device is switched to the parallel mode and accepts data from the PICLK and PIN[7:0] inputs. The POCLK is switched in to generate the 19.44 MHz PICLK. This technique also guarantees that the SUNI will generate a LOS indication when the optics loses incoming light. This is done due to the CY7B951 not squelching the data in a loss of signal condition.

The transmit line interface consists of the SUNI PECL transmit outputs which are buffered by the Cypress CY7B951 and then fed directly to the transmit optics.

Optical transceivers having a standard 9-pin duplex SC receptacle are used.

The SUNI is configured for bit serial operation. The 155.52 MHz transmit clock source is synthesized by the CY7B951 from a 19.44 MHz oscillator. The receive clock and data recovery is supplied by the Cypress CY7B951 device.

If the loop back select is enabled on the CY7B951 the transmit data is muxed in to the receive PLL and the recovered clock and data are fed back to the SUNI device.

The SUNI can also be configured for loop time operation. When configured for loop time operation, only the receive clock and data are required.

UTOPIA Identification ROM

The upper 32 bytes of the address space is used by the UTOPIA indentification ROM to hold the interface configuration information.

Address	Function	Address	Function
0x1C0-0x1DF	Reserved	0x1E4-0x1EB	64 or 48-bit Address
0x1E0	Protocol Type	0x1EC-0x1EF	Reserved
0x1E1	Media Type	0x1F0-0x1FF	Manufacturer ID, Version
0x1E2-0x1E3	Capability		

Protocol Type:

Contains an identifier for the type of framing/protocol used on this PHY interface. The SAPI board has 0x0C programmed into this location which specifies 155.52 Mbps (SONET/OC-3) ATM Forum standard. The following values are defined:

Value	Framing Type
0x00-0x03	Reserved
0x04	44.736 Mbps (DS-3) ATM Forum Standard
0x05-0x07	Reserved
0x08	100 Mbps (4B/5B block coded) ATM Forum Standard
0x09-0x0B	Reserved
0x0C	155.52 Mbps (SONET/OC-3) ATM Forum Standard
0x0D	155.52 Mbps (8B/10B block coded) ATM Forum Standard
0x0E-0xFE	Reserved
0xFF	Undefined/Unidentified Protocol Type

Media Type:

Contains an identifier for the type of media used on this PHY interface. The SAPI board has 0x05 programmed into this location which specifies a low cost Multimode fiber (LCMF, 500m). The following values are defined:

Value	Media Type
0x00	Category 3 Unshielded Twisted Pair (CAT3-UTP)
0x01	Category 5 Unshielded Twisted Pair (CAT5-UTP)
0x02	Shielded Twisted Pair (STP)
0x03	Reserved
0x04	Very Low-Cost Multimode Fiber (VLCMF, 150 m)
0x05	Low-Cost Multimode Fiber (LCMF, 500 m)
0x06	Multimode Fiber (MF, 2km)
0x07	Reserved
0x08	Single Mode Fiber (SMF)
0x09-0x0B	Reserved
0x0C	Coaxial Cable (COAX)
0x0D	Reserved
0x0F	Undefined/Unidentified Media Type

Capability:

Contains two octets which define the capability of the PHY interface. The SAPI board has 0x21 & 0x0C programmed into octets 1 & 2 respectively. The capabilities include:

1. TxRef, =1 when this interface supports the TxRefB UTOPIA signal.
2. RxRef, =1 when this interface supports the RxRefB UTOPIA signal.
3. TxClav, =1 when this interface supports the TxClav UTOPIA signal.
4. RxClav, =1 when this interface supports the RxClav UTOPIA signal.

5. TxXon, =1 when this interface supports the TxXon UTOPIA signal.

6. Ver[3:0], 4 bits UTOPIA version number, value for this specification =1.

7. D16, =1 to indicate 16-bit datapath, 0 = 8-bit datapath.

8. HEC, =1 to indicate the HEC is carried in the UDF(1) field.

9. HCS, =1 to indicate HCS is carried in the UDF(2) field, for 16-bit mode only.

10. NOTE "rsvd" stands for Reserved.

Assignments of fields are shown below.

rsvd	HCS	HEC	D16	Ver[3]	Ver[2]	Ver[1]	Ver[0]	octet 1
rsvd	rsvd	rsvd	TxXon	RxClav	TxClav	RxRef	TxRef	octet 2

64 or 48-bit Address:

Contains eight octets which define the 64 or 48-bit address of the PHY interface. If a 48-bit address is used, the 2 most significant octets are zero filled. The address is stored in Big-Endian format (MSB is in the LS address). The SAPI board has 0x00 programmed into this location.

Reserved:

Reserved for future expansion.

Manufacturer ID, etc.:

Contains sixteen octets which identify the manufacturer of the PHY interface. Using the ASCII character set (7-bit code) is encouraged. Three octets of ASCII representing the manufacture ID and 13 octets of part number.

M.S L.S	0	1	2	3	4	5	6	7
0	NUL	DLE	SP	0	@	P	\	p
1	SOH	DC1	!	1	A	Q	a	q
2	STX	DC2	"	2	B	R	b	r
3	ETX	DC3	#	3	C	S	c	s
4	EOT	DC4	$	4	D	T	d	t
5	ENQ	NAK	%	5	E	U	e	u

6	ACK	SYN	&	6	F	V	f	v
7	BEL	ETB	'	7	G	W	g	w
8	BS	CAN	(	8	H	X	h	z
9	HT	EM	)	9	I	Y	i	y
A	LF	SUM	*	:	J	Z	j	z
B	VT	ESC	+	;	K	[	k	
C	FF	FS	,	<	L	\	l	|
D	CR	GS	-	=	M	]	m	
E	SO	RS	.	>	N	^	n	~
F	SI	µS	/	?	O	<-	o	DEL

P	M	C	-	P	M	5	9	4	5	-	S	A	P	I	
50	4d	43	2d	50	4d	35	39	34	35	2d	53	41	50	49	20

DAUGHTERBOARD REGISTERS

The SAPI daughterboard has two write only register bits. One bit is a software reset bit and the other is a transmit loopbacd enable bit.

Software Reset

The software reset bit is at binary address 1110xxxxx (the most significant bit is at the far left and the least significant is at the far right). The least significant 5 bits of the address are don't cares. Writing a binary xxxxxxx1 to this address will hold the SUNI, the FIFO, and the PALs reset. Writing a binary xxxxxxx0 to this address will remove the reset. The most significant 7 bits of data are don't cares. This is a write only bit. A hardware reset removes the software reset.

Transmit Loopback Enable

The transmit loopback enable bit is at binary address 1111xxxxx (the most significant bit is at the far left and the least significant is at the far right). The least significant 5 bits of the address are don't cares. Writing a binary xxxxxxx1 to this address will mux the transmit output data going to the optics, into the inputs of the clock and data recovery PLL. This is all done inside the Cypress CY7B951 device.

This allows a diagnostic loopback to be done at the Cypress part which will verify the connections and functionality between the Cypress device and the SUNI device. done. Writing a binary xxxxxxx0 to this address will disable transmit diagnostic loopback. The most significant 7 bits of data are don't cares. This is a write only bit. A hardware reset removes the transmit loopback enable (if it was set).

INTERFACE DESCRIPTION

UTOPIA Interface

The UTOPIA Interface makes the SUNI drop side receive and transmit signals compatible with the UTOPIA 1.04 interface specification. It consists of two high speed 22V10 PALs, two high speed IDT74FCT377C buffers, and a receive IDT72201 clocked FIFO. The 22V10 PALs can be replaced with faster versions if you must run at a higher than 20 MHz TxClk and RxClk clock signals.

The Transmit drop side interface is controlled by the ATM layer through the edge connector. All the transmit signals from the ATM layer change with respect to the TxClk. All the input signals to the ATM layer are sampled on the rising edge of the TxClk.

The SUNI device asserts the TCA signal when it has a complete empty cell available. This signal goes to the PAL (U17) and causes the TxFullB signal to the ATM layer to be de-asserted (high). The ATM layer asserts the TxClavB signal (low) when it has a complete Cell of data to transfer to the PHY device. The TxEnbB signal from the ATM layer (Vicksburg card) is the output of the TxFullB signal from the PHY layer gated with the TxClavB signal from the ATM layer. The way the TxEnbB signal goes active (low) depends on whether the ATM layer is ready to send a cell of data before the PHY layer becomes available to accept the data, or whether the PHY layer is ready to accept a cell of data before the ATM layer is ready to send data.

The case where the ATM layer has a cell available for transmission before the PHY layer is ready to accept the cell is handled as follows; The Vicksburg card drives the TSOC signal active (high) and the TxData bus with valid octet byte zero coincident with the assertion of the TxClavB signal, and waits for the TxFullB signal from the PHY layer to go inactive (high). When the PHY device has a cell available, the TxFullB signal goes inactive (high) and then the TxEnbB signal is immediately asserted (low) (after a delay through a gate). On the next rising edge of the TxClk signal, the second byte of data is driven onto the TxData bus and the TSOC signal is de-asserted (low).

The case where the PHY layer is ready to accept a cell of data before the ATM layer is ready to transmit the cell is handled as follows; The PHY layer de-asserts the TxFullB signal (high) and waits for the TxEnbB signal to go active (low). When the

ATM layer has a cell available for transmission, the TxClavB is set active (low) on the rising edge of the TxClk signal, and drives the TSOC signal active (high) and the TxData bus with valid octet byte zero . The TxClavB signal sets the TxEnbB signal active (low) through a gate delay.

In either case, the TxData bus is continually clocked into the first buffer (U18) by the rising edges of the TxClk signal. The assertion of the TxEnbB signal enables the TWRB signal to the SUNI device. On the falling edge of the TWRB signal (rising edge of TxClk) the data from U18 is clocked into the second buffer (U19). The clock signal to U19 is generated by the PAL (inverted TxClk). The ATM layer updates the TxData with new data on the rising edge of each TxClk signal while TxEnbB is asserted and the TxFullB signal is de-asserted (high). If at the end of the current cell transfer, another cell is available (TCA remains active), the TxFullB will still be asserted (low) on the 51'st byte transferred. This is to accomodate the propagation delay of TCA going inactive (low) at the end of a cell transfer and then being sampled by the PAL (TCA must be sampled as it can go active at any time). This will incur an extra clock delay per cell transfer. The TxClavB signal goes inactive (high) for a minimum of two cycles per cell trasfer. There will be a 3 clock cycle delay per cell transfer as the TxFullB and the TxClavB overlap.

The Receive drop side interface is controlled by the ATM layer through the edge connector. All the receive signals from the ATM layer change with respect to the RxClk. All the input signals to the ATM layer are sampled on the rising edge of the RxClk. The receive side incorporates a external FIFO so that the SUNI device does not overrun due to the latency times between burst cell reads of the ATM layer (Vicksburg mother board).

The SUNI device asserts the RCA signal when it has a complete cell to transfer to the FIFO. The RCA signal goes to the Receive PAL (U16) and the PAL asserts the write enables to the receive FIFO. If the receive FIFO is not full (/FF high), the receive PAL will start clocking the data from the SUNI into the FIFO by generating the RRDB clock signal. The RSOC signal from the SUNI is inserted into bit 9 of the FIFO data inputs. The FIFO enables the /FF (active low FIFO Full) signal when it is full which disables further transfer of data from the SUNI to the FIFO. If the FIFO gets full, the SUNI will have transferred an indeterminate portion of a cell. The rest of the cell will get transferred as soon as the FIFO de-activates the /FF signal. The Receive PAL uses the RxCLK signal from the ATM layer to generate the WClk signal going to the FIFO and the RRDB clock signal to the SUNI. The WEN going to the FIFO is disabled while the /FF is active (low). While the FIFO write enable is disabled, the clock going to the FIFO is the same as the RxCLK. This is done because the FIFO /FF signal will not be disabled (high) untill it gets a rising edge on the WCLK input.

The RxEmptyB signal comes from the Receive FIFO /EF (active low Empty FIFO) signal. The Receive FIFO de-asserts the the RxEmptyB signal (high) upon reception of a single byte of data. On the next rising edge of the RxClk clock signal, the ATM layer samples the RxEmptyB signal and on the following RxClk clock signal, the ATM layer activates the RxEnbB signal (low) if it has an empty cell available. The

RxEnbB signal from the ATM layer goes to the Receive PAL (U16) and to the read enable (/RDEN1) input of the receive FIFO. On the next rising edge of the RxCLK signal after the RxEnbB signal goes active (low) the first byte of data is clocked out of the FIFO along with the RSOC signal. The receive ATM layer ignores the data until it sees a valid RSOC signal. Once cell transfer has commenced, the ATM layer expects a complete cell transfer. If the FIFO is empty (RxEmptyB is active) and then the SUNI starts to transfer data to the FIFO, there might only be one byte in the FIFO before the RxEmptyB signal could go inactive (high). For the FIFO to become empty, the SUNI must not have had any cells to transfer and therefore the first byte in the FIFO would be the first byte of the Cell along with the valid RSOC signal. Since the RxClk clock signal is generating the write and read clock signals to the FIFO as well as the read clock signal to the SUNI, the ATM layer cannot read the data out of the FIFO faster than the SUNI can write the data into the FIFO.

SAPI Board Edge Connector Interface

The SAPI UTOPIA Edge Connector Interface includes all the signals required to connect the SAPI board to a high layer protocol entity (i.e. a AAL processor). Cells can be written to the SUNI transmit FIFO and read from the SUNI receive FIFO using this interface. The edge connector is made up of a 100 pin dual line female connector is shown in table below. It consists of signals appropriate to read and write to the registers of the devices on the daughter board, and it provides the necessary power and ground. TTL signal levels are used on this interface.

Signal Name	Type	PIN	Function
GND	Power	1	Ground
GND	Power	2	Ground
TxDat[0] TxDat[1] TxDat[2] TxDat[3] TxDat[4] TxDat[5] TxDat[6] TxDat[7]	I I I I I I I I	3 5 9 11 4 6 10 12	The SUNI is configured for the 8 bit FIFO interface, TxDat[7:0] corresponds to a cell byte. TxDat[7] corresponds to bit 1, the first bit received. TxDat[0] corresponds to bit 8, the last bit received.
VCC	Power	7	+5 Volts
VCC	Power	8	+5 Volts
GND	Power	13	Ground
TxPrty	I	14	Transmit data bus (TxDat[7:0]) odd parity. Not Used

TxSOC	I	15	Transmit start of cell indication. Identifies the first byte (word) of a cell on inputs TxDAT[7:0]
GND	Power	16	Ground
GND	Power	17	Ground
TxFullB	O	18	Active low signal from the PHY to ATM layer, asserted by the PHY layer 4 cycles before it is no longer able to accept transmit data.
TxClavB	I	19	Active low signal from the ATM layer to the PHY layer, asserted by the ATM layer when it has a full cell to transmit.
GND	Power	20	Ground
GND	Power	21	Ground
TxCLK	I	22	The transmit transfer/synchronization clock provided by the ATM to the PHY layer for synchronizing transfers on the TxDATA bus. (nominally at 20 MHz).
TxRefB	I	23	Transmit Reference. Input for the purposes of synchronization (e.g. 8 KHz frame marker or SONET frame indicator). Not Used
GND	Power	24	Ground
GND	Power	25	Ground
TxXon	O	26	PHY layer flow control. 1= Xon, 0= Xoff. Asserted by the PHY layer for normal transmission. Deasserted by the PHY layer when the ATM link is experiencing congestion. The response of the ATM layer to this signal is user defined. Not Used.
TxEnbB		27	Active low transmit signal asserted by the ATM layer during cycles when the TxDat contains valid cell data.
GND	Power	28	Ground
GND	Power	29	Ground

RxDat[0] RxDat[1] RxDat[2] RxDat[3] RxDat[4] RxDat[5] RxDat[6] RxDat[7]	O O O O O O O O	31 33 37 39 30 32 38 40	RxDat[7:0] corresponds to a cell byte. Please refer to the SUNI datasheet for the byte cell data structure. RxDat[7] corresponds to bit 1, the first bit received. RxDat[0] corresponds to bit 8, the last bit received.
RxPrty	O	34	Receive data bus (RxDat[7:0]) odd parity. Not Used
VCC	Power	35	+5 Volts
VCC	Power	36	+5 Volts
GND	Power	41	Ground
Undefined		42	
RxSOC	O	43	Receive start of cell indication. Identifies the first byte (word) of a cell on outputs RxDat[7:0]
GND	Power	44	Ground
GND	Power	45	Ground
RxEmptyB	0	46	Active low empty signal to indicate that in the current cycle there is no valid data for delivery to the ATM layer.
RxEnbB	I	47	Active low signal asserted by the ATM layer to indicate that the RxDat[7:0] will be sampled at the start of the next cycle. Sampling occurs on cycles following those with RxENB asserted and RxEmptyB Deasserted.
GND	Power	48	Ground
GND	Power	49	Ground
RxClk	I	50	Transfer/synchronization clock provide by the ATM layer for synchronizing transfers on RxDat (nominally 20 MHz).
RxRefB	O	51	Receive Reference. Output for the purposes of synchronization (e.g. 8 KHz frame marker or SONET frame indicator). Not Used.
GND	Power	52	Ground
GND	Power	53	Ground

RxClav	O	54	Receive Cell Available Signal. Active high signal from the PHY layer to the ATM layer, asserted to indicate that there is a complete cell available for transfer to the ATM layer.
RxFlush		55	Not Used
GND	Power	56	Ground
GND	Power	57	Ground
A[4]	I	58	Address bus bit 7.
A[0]	I	59	Address bus bit 6.
A[5]	I	60	Address bus bit 5.
A[1]	I	61	Address bus bit 4.
Undefined		62	
VCC	Power	63	+5 Volts
VCC	Power	64	+5 Volts
A[2]	I	65	Address bus bit 3.
A[6]	I	66	Address bus bit 2.
A[3]	I	67	Address bus bit 1.
A[7]	I	68	Address bus bit 0.
GND	Power	69	Ground
GND	Power	70	Ground
D[0]	I/O	71	Data bus bit 0.
A[8]	I	72	Address bit used to read the Standard PHY registers.
D[1]	I/O	73	Data bus bit 1.
D[4]	I/O	74	Data bus bit 4.
GND	Power	75	Ground
GND	Power	76	Ground
D[2]	I/O	77	Data bus bit 2.
D[5]	I/O	78	Data bus bit 5.
D[3]	I/O	79	Data bus bit 3.
D[6]	I/O	80	Data bus bit 6.

GND	Power	81	Ground
GND	Power	82	Ground
Prty	I/O	83	Data bus D[7:0] odd parity. Not Used.
D[7]	I/O	84	Data bus bit 7.
VCC	Power	85	+5 Volts
VCC	Power	86	+5 Volts
Undefined		87	
INTB	O	88	Active low, open-drain interrupt signal.
CSB	I	89	The SUNI active low chip select signal.
GND	Power	90	Ground
GND	Power	91	Ground
RSTB	I	92	Active low H/W reset.
RDB	I	93	Active low read signal asserted to enable data from the addressed location onto the D[7:0] bus.
GND	Power	94	Ground
GND	Power	95	Ground
RDY		96	Not Used
WRB	I	97	Active low write signal asserted to write data to the addressed location from the D[7:0] bus.
ALE	I	98	Address latch enable. When high, identifies that address is valid on D[7:0]. Not Used.
GND	Power	99	Ground
GND	Power	100	Ground

SUNI REGISTER ADDRESS MAP

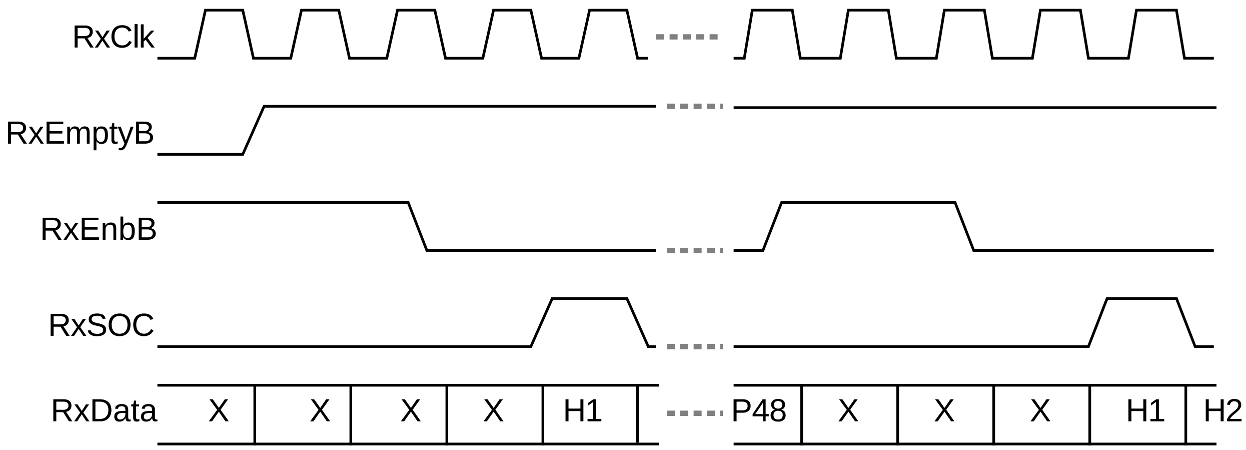
The microprocessor interface provides access to the SUNI device registers via the 100 pin UTOPIA connector. The SUNI address space extends from 00H to FFH. Address bit 8 (A8 being the most significant bit and A0 being the least signifcant bit) is set low to access the SUNI register space . Below is a list of the SUNI device registers. For further details, please refer to the "Saturn User Network Interface Device Datasheet".

Address	Register
0x00	SUNI Master Reset and Identity
0x01	SUNI Master Configuration
0x02	SUNI Master Interrupt Status
0x04	SUNI Master Clock Monitor
0x05	SUNI Master Control
0x06-0x07	Reserved
0x08-0x0B	Reserved
0x0C-0x0F	Reserved
0x10	RSOP Control/Interrupt Enable
0x11	RSOP Status/Interrupt Status
0x12	RSOP Section BIP-8 LSB
0x13	RSOP Section BIP-8 MSB
0x14	TSOP Control
0x15	TSOP Diagnostic
0x16-0x17	TSOP Reserved
0x18	RLOP Control/Status
0x19	RLOP Interrupt Enable/Status
0x1A	RLOP Line BIP-24 LSB
0x1B	RLOP Line BIP-24
0x1C	RLOP Line BIP-24 MSB
0x1D	RLOP Line FEBE LSB
0x1E	RLOP Line FEBE
0x1F	RLOP Line FEBE MSB
0x20	TLOP Control
0x21	TLOP Diagnostic
0x22-0x23	TLOP Reserved
0x24-0x27	Reserved
0x28-0x2B	Reserved
0x2C-0x2F	Reserved
0x30	RPOP Status/Control
0x31	RPOP Interrupt Status
0x32	RPOP Reserved
0x33	RPOP Interrupt Enable

0x34	RPOP Reserved
0x35	RPOP Reserved
0x36	RPOP Reserved
0x37	RPOP Path Signal Label
0x38	RPOP Path BIP-8 LSB / Load Meters
0x39	RPOP Path BIP-8 MSB
0x3A	RPOP Path FEBE LSB
0x3BH	RPOP Path FEBE MSB
0x3C-0x3F	RPOP Reserved
0x40	TPOP Control/Diagnostic
0x41	TPOP Pointer Control
0x42	TPOP Source Control
0x43	TPOP Reserved
0x44	TPOP Reserved
0x45	TPOP Arbitrary Pointer LSB
0x46	TPOP Arbitrary Pointer MSB
0x47	TPOP Reserved
0x48	TPOP Path Signal Label
0x49	TPOP Path Status
0x4A	TPOP Reserved
0x4B-0x4F	TPOP Reserved
0x50	RACP Control/Status
0x51	RACP Interrupt Enable/Status
0x52	RACP Match Header Pattern
0x53	RACP Match Header Mask
0x54	RACP Correctable HCS Error Count
0x55	RACP Uncorrectable HCS Error Count
0x56-0x5F	RACP Reserved
0x60	TACP Control/Status
0x61	TACP Idle/Unassigned Cell Header Pattern
0x62	TACP Idle/Unassigned Cell Payload Octet Pattern
0x63-0x67	TACP Reserved
0x68-0x7F	Reserved
0x80	SUNI Master Test
0x81-0xFF	Reserved for Test

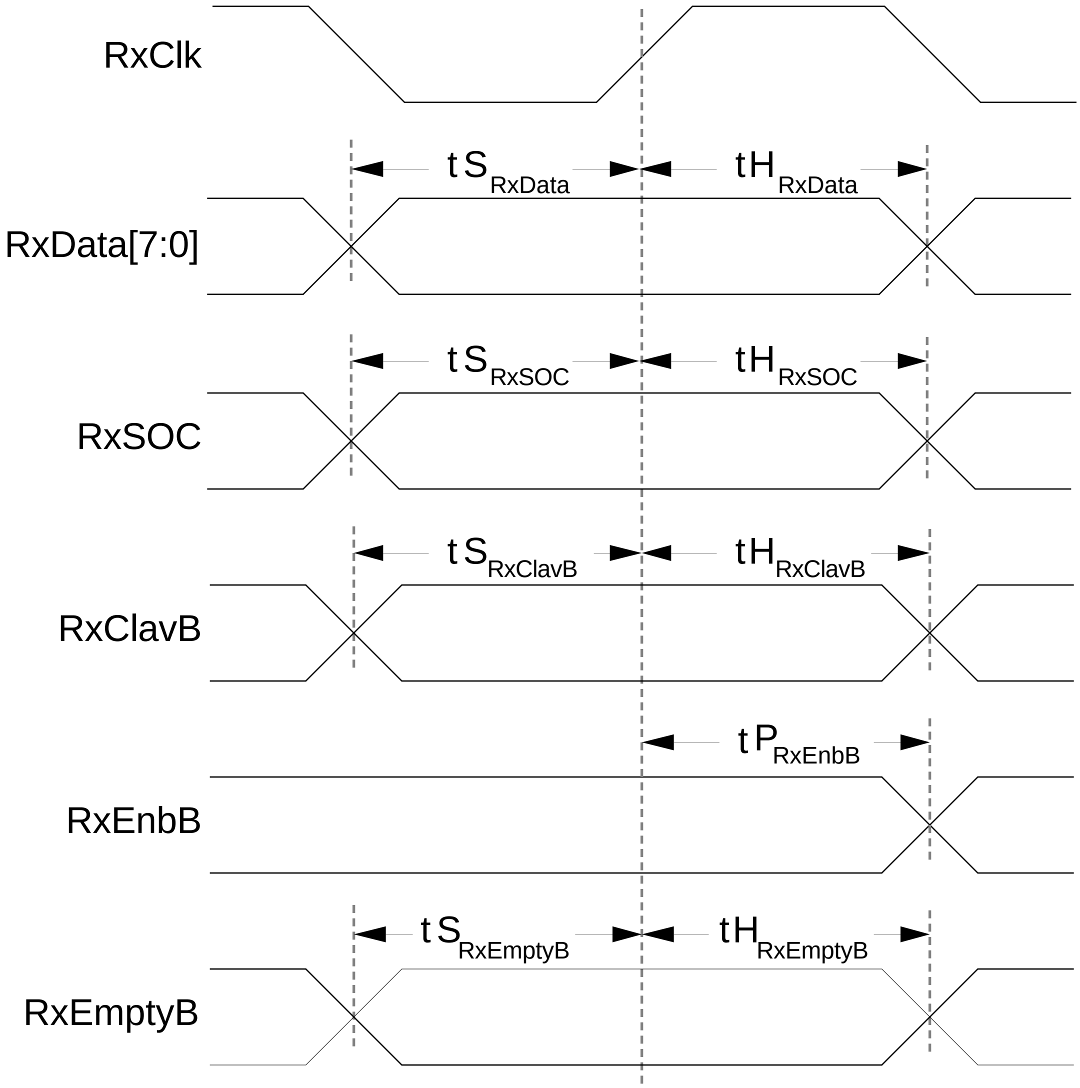
RECEIVE DROP SIDE TIMING

Receive Functional Timing



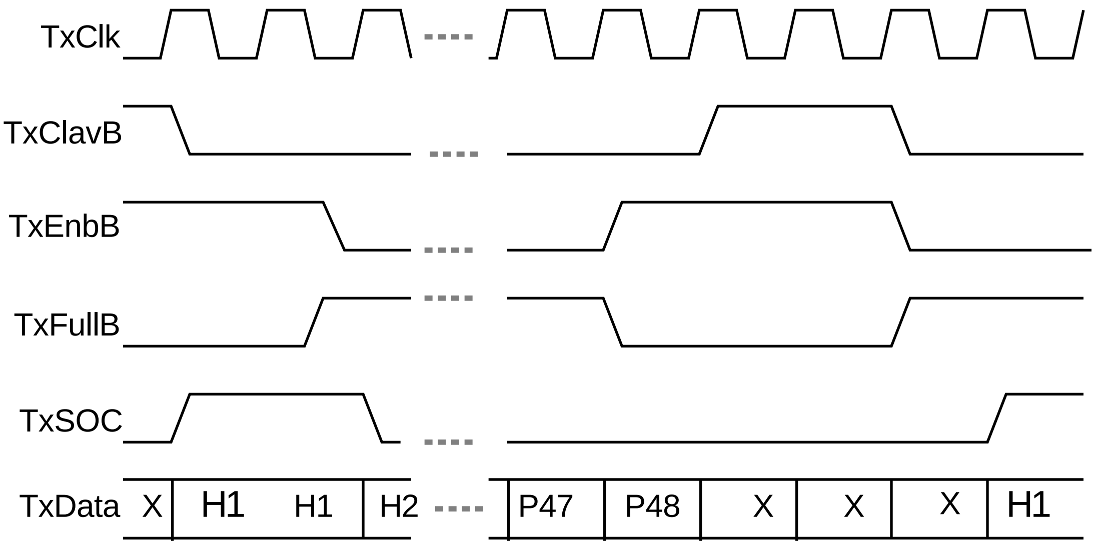
Receive Interface Timing

Symbol	Parameter	Min	Max	Units
	RxClk Frequency (nominaly 20 MHz)		20	MHz
	RxClk Duty Cycle	40	60	%
tS_{RxData}	RxData[7:0] Set-up Time to RxClk	10		ns
tH_{RxData}	RxData[7:0] Hold Time to RxClk	1		ns
tS_{RxSOC}	RxSOC Set-up Time to RxClk	10		ns
tH_{RxSOC}	RxSOC Hold Time to RxClk	1		ns
$tS_{RxClavB}$	RxClavB Set-up Time to RxClk	10		ns
$tH_{RxClavB}$	RxClavB Hold Time to RxClk	1		ns
tP_{RxEnbB}	RxClk high to RxEnbB Valid	1	20	ns
tS_{RxData}	RxData[7:0] Set-up Time to RxClk	10		ns
tH_{RxData}	RxData[7:0] Hold Time to RxClk	1		ns


RxClk
tS RxData
tH RxData
RxData[7:0]
tS RxSOC
tH RxSOC
RxSOC
tS RxClavB
tH RxClavB
RxClavB
tP RxEnbB
RxEnbB
tS RxEmptyB
tH RxEmptyB
RxEmptyB

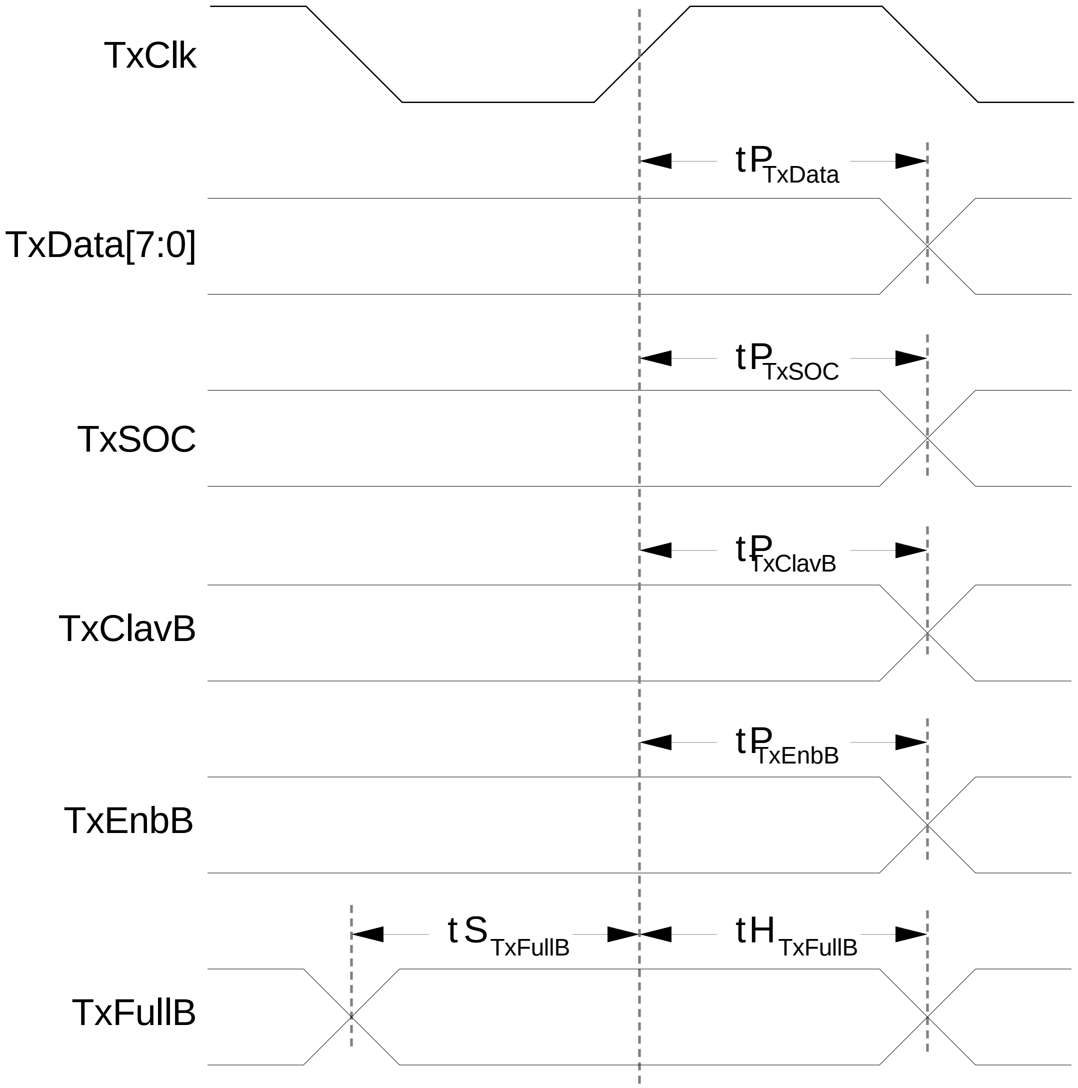
TRANSMIT DROP SIDE TIMING

Transmit Functional Timing



Transmit Interface Timing

Symbol	Parameter	Min	Max	Units
	TxClk Frequency (nominaly 20 MHz)		20	MHz
	TxClk Duty Cycle	40	60	%
tP_{TxData}	TxClk high TxData[7:0] Valid	1	20	ns
tP_{TxSOC}	TxClk high TxSOC Valid	1	20	ns
$tP_{TxClavB}$	TxClk high TxClavB Valid	1	20	ns
tP_{TxData}	TxClk high TxData[7:0] Valid	1	20	ns
tP_{TxEnbB}	TxClk high TxEnbB Valid	1	20	ns
$tS_{TxFullB}$	TxFullB Set-up Time to TxClk	10		ns
$tH_{TxFullB}$	TxFullB Hold Time to TxClk	1		ns


TxClk
tP_TxData
TxData[7:0]
tP_TxSOC
TxSOC
tP_TxClavB
TxClavB
tP_TxEnbB
TxEnbB
tS_TxFullB
tH_TxFullB
TxFullB

CHARACTERISTICS

Symbol	Parameter	Min	Max	Units	Test Conditions
V_{5DC}	+5V DC Power Supply Voltage	4.90	5.25	V	
I_{5DC}	+5V DC Power Supply Current		1.00	A	V_{5DC} = 5.0 V ± 5%
T_A	Ambient Temperature	0	50	°C	V_{DC} = 5.0 V ± 5%

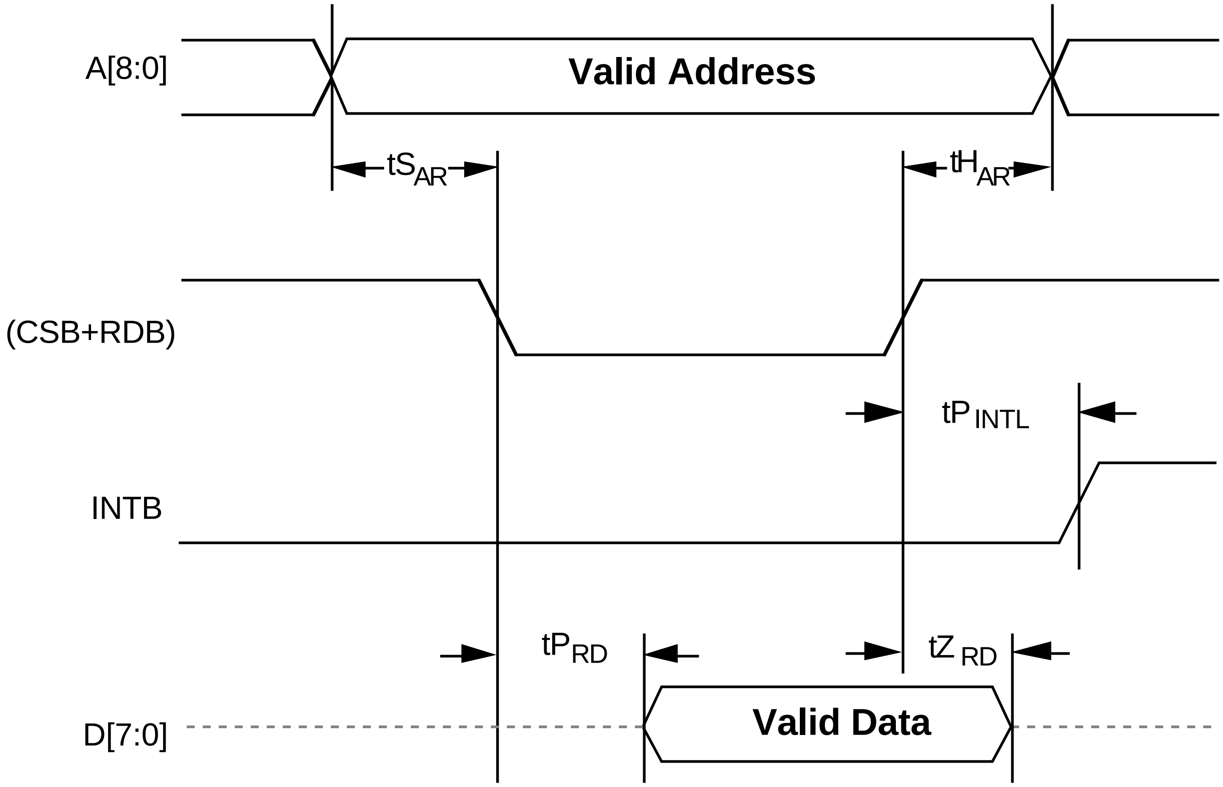
MICROPROCESSOR INTERFACE TIMING CHARACTERISTICS

(T_A = 0°C to +70°C, V_{DD} = 5 V ±10%)

Microprocessor Interface Read Access (Fig. xx)

Symbol	Parameter	Min	Max	Units
tH_{AR}	Address to Valid Read Hold Time	20		ns
tS_{AR}	Address to Valid Read Set-up Time	25		ns
tP_{RD}	Valid Read to Valid Data Propagation Delay		80	ns
tZ_{RD}	Valid Read Negated to Output Tri-state		20	ns
tP_{INTH}	Valid Read Deasserted to INTB High		50	ns

Microprocessor Interface Read Timing



Notes on Microprocessor Interface Read Timing:

1. Output propagation delay time is the time in nanoseconds from the 50% point of the reference signal to the 30% or 70% point of the output.

2. A valid read cycle is defined as a logical OR of the CSB and the RDB signals.

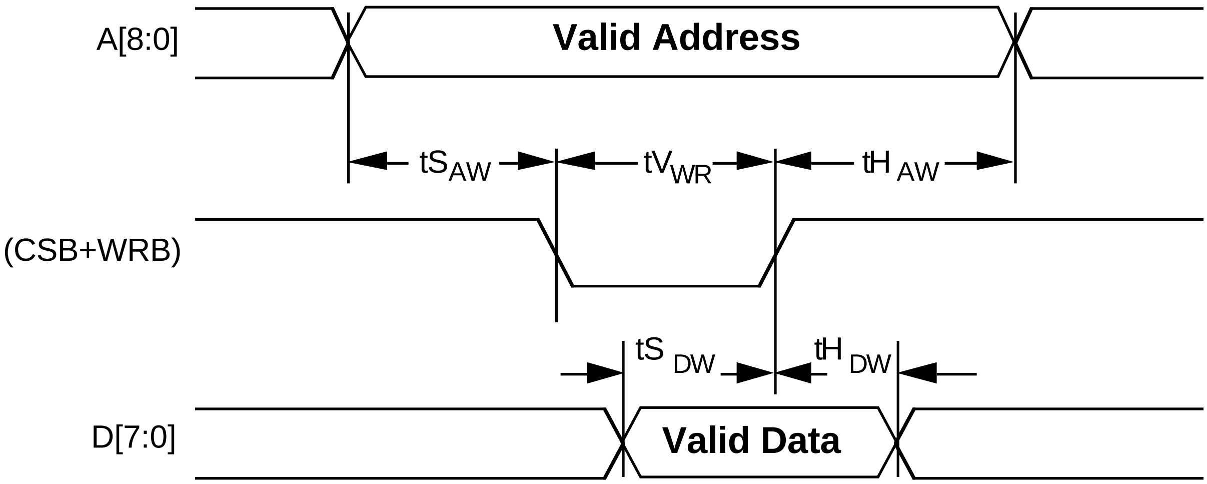
3. When a set-up time is specified between an input and a clock, the set-up time is the time in nanoseconds from the 1.4 Volt point of the input to the 1.4 Volt point of the clock.

4. When a hold time is specified between an input and a clock, the hold time is the time in nanoseconds from the 1.4 Volt point of the input to the 1.4 Volt point of the clock.

Microprocessor Interface Write Access

Symbol	Parameter	Min	Max	Units
tS_{DW}	Data to Valid Write Set-up Time	20		ns
tS_{AW}	Address to Valid Write Set-up Time	25		ns
tH_{AW}	Address to Valid Write Hold Time	20		ns
tS_{DW}	Data to Valid Write Set-up Time	20		ns
tH_{DW}	Data to Valid Write Hold Time	20		ns
tV_{WR}	Valid Write Pulse Width	40		ns

Microprocessor Interface Write Timing



Notes on Microprocessor Interface Write Timing:

1 A valid write cycle is defined as a logical OR of the CSB and the WRB signals.

2. Microprocessor Interface timing applies to normal mode register accesses only.

3. When a set-up time is specified between an input and a clock, the set-up time is the time in nanoseconds from the 1.4 Volt point of the input to the 1.4 Volt point of the clock.

4. When a hold time is specified between an input and a clock, the hold time is the time in nanoseconds from the 1.4 Volt point of the input to the 1.4 Volt point of the clock.

APPENDIX A: PAL EQUATIONS

```
-- UTOPIA interface PAL U12
-- Used to generate the LOS and Chip Select Signals
--    to the SUNI receive FIFOs


USE work.bv_math.all;      -- necessary for inc_bv();
USE work.rtlpkg.all;
USE work.cypres.all;

ENTITY los_cs_pal IS
        PORT   (poclk0, poclk1, csb, rdb, wrb, a8, a6, a5,
                rstb, a7, d0, sd: IN BIT;
                rser, csbo, loopb,
                prom_enb, brstb : OUT BIT;
                 piclk: INOUT x01z);

ATTRIBUTE order_code of los_cs_pal:ENTITY is "PAL22V10D-10PC";
ATTRIBUTE part_name of los_cs_pal:ENTITY IS "C22V10";
ATTRIBUTE pin_numbers of los_cs_pal:ENTITY IS
        "poclk0:1  " &
        "poclk1:2  " &
        "csb:3     " &
        "wrb:4     " &
        "rdb:5     " &
        "a8:6      " &
        "a6:7      " &
        "a5:8     " &
        "rstb:9    " &
        "a7:10     " &
        "d0:11     " &
        "sd:13     " &
        "csbo:17   " &
        "loopb:18  " &
        "rser:19   " &
        "prom_enb:21 " &
        "brstb:22 " &
        "piclk:23";

END los_cs_pal;

ARCHITECTURE behavior OF los_cs_pal IS
SIGNAL set_reset,piclk_b,hold, grst,rser_din,oe_d: BIT;
SIGNAL  loopb_d,oe, loopb_en,loopb_dis,sd_sample: BIT;
SIGNAL high  :BIT := '1';
BEGIN
```

```
proc1:          PROCESS
        BEGIN
        WAIT UNTIL (poclk0 = '1');
-- Sample the SD input
                IF ( sd = '1' ) THEN
                        sd_sample <= '1';
                ELSE
                        sd_sample <= '0';
                END IF;
-- Set RSER low if loss of signal occurs
                IF ( sd_sample = '1') THEN
                        rser_din <= '1';
                ELSE
                        rser_din <= '0';
                END IF;
        END process;



proc2:          PROCESS
        BEGIN
-- Enable PICLK
                IF ( rser_din = '0' AND sd_sample = '0'
                AND rstb ='1' and set_reset = '0') THEN
                        oe <= '1';
                ELSE
                        oe <= '0';
                END IF;

-- Enable CSB
                IF ( csb = '0' AND a8 = '0' )  THEN
                        csbo <= '0';
                ELSE
                        csbo <= '1';
                END IF;

-- Enable UTOPIA ID PROM
                IF ( csb = '0' AND a8 = '1' AND a7 = '1' AND
                a6 = '1' AND a5 = '1')  THEN
                        prom_enb <= '0';
                ELSE
                        prom_enb <= '1';
                END IF;

-- Set reset
```

```
                IF rstb = '0' THEN
                        set_reset <= '0';
                ELSIF   (a8 = '1' AND a7 ='1' AND a6 = '1' AND
                a5 = '0' AND d0 = '1' AND csb = '0' AND wrb = '0') THEN
                        set_reset <= '1';
-- Clear reset
                ELSIF (a8 = '1' AND a7 ='1' AND a6 = '1' AND
                 a5 = '0' AND d0 = '0' AND csb = '0' AND wrb = '0') THEN
                        set_reset <= '0';
                END IF;
-- BRSTB
                IF (rstb = '0' OR set_reset ='1') THEN
                        brstb <= '0';
                ELSIF (rstb = '1' and set_reset = '0' ) THEN
                        brstb <= '1';
                END IF;
-- Disable LOOPB
                IF  rstb = '0' OR (a8 = '1' AND a7 ='1' AND
                a6 = '1' AND a5 = '1' AND d0 = '0' AND csb = '0'
                AND wrb = '0')
                OR (a8 = '1' AND a7 ='1' AND a6 = '1' AND
                a5 = '0' AND d0 = '1' AND csb = '0' AND wrb = '0') THEN
                        loopb_dis <= '1';
                        loopb_en <= '0';
-- Enable LOOPB
                ELSIF (rstb = '1' AND a8 = '1' AND a7 ='1' AND
                a6 = '1' AND a5 = '1' AND d0 = '1' AND csb = '0'
                AND wrb = '0') THEN
                        loopb_en <= '1';
                        loopb_dis <= '0';
                END IF;

        END process;
          b1:bufoe port map (poclk1,oe,piclk,piclk_b);
          b2:buf port map (rser_din,rser);
          b3:srl port map (loopb_dis,loopb_en,loopb);
END behavior;
```

DESIGN EQUATIONS (06:44:11)
These equations were extracted from the LOS_CS1.RPT report file. They can be used or the above VHDL code can be used to generate the proper .JED files. The LOS_CS1.JED files are available on request.

```
/csbo =
     /csb * /a8

loopb =
     /loopb_en * loopb
   + loopb_dis * /loopb_en

rser.D =
     sd_sample_BEH_i1_0_DFF.Q

rser.C =
     poclk0

/prom_enb =
     /csb * a8 * a7 * a6 * a5

brstb =
     rstb * /set_reset

piclk =
     poclk1

piclk.OE =
     rstb * /set_reset * /sd_sample_BEH_i1_0_DFF.Q * /rser.Q

sd_sample_BEH_i1_0_DFF.D =
     sd

sd_sample_BEH_i1_0_DFF.C =
     poclk0

set_reset =
     rstb * /csb * a8 * a7 * a6 * /a5 * d0 * /wrb
   + rstb * wrb * set_reset
   + rstb * a5 * set_reset
   + rstb * /a6 * set_reset
   + rstb * /a7 * set_reset
   + rstb * /a8 * set_reset
   + rstb * csb * set_reset
```

```
loopb_en =
     rstb * /csb * a8 * a7 * a6 * a5 * d0 * /wrb
   + rstb * /a5 * /d0 * loopb_en
   + rstb * wrb * loopb_en
   + rstb * /a6 * loopb_en
   + rstb * /a7 * loopb_en
   + rstb * /a8 * loopb_en
   + rstb * csb * loopb_en

/loopb_dis =
     rstb * /csb * a8 * a7 * a6 * a5 * d0 * /wrb
   + rstb * /a5 * /d0 * /loopb_dis
   + rstb * wrb * /loopb_dis
   + rstb * /a6 * /loopb_dis
   + rstb * /a7 * /loopb_dis
   + rstb * /a8 * /loopb_dis
   + rstb * csb * /loopb_dis
```

```
-- UTOPIA interface PAL U16
-- Used to interface the Vicksburg Motherboard F-FRED chip --
to the SUNI receive FIFOs


USE work.bv_math.all;      -- necessary for inc_bv();
USE work.rtlpkg.all;

ENTITY rx_pal IS
PORT   (rxclk, resetb, rsoc, rca, RxenbB, low, paeb, pafb, ffb: IN BIT;
                        rrdb, wclk, wen1b: OUT BIT);


ATTRIBUTE order_code of rx_pal:ENTITY is "PAL22V10D-10PC";
ATTRIBUTE part_name of rx_pal:ENTITY IS "C22V10";
ATTRIBUTE pin_numbers of
          rx_pal:ENTITY IS
          "rxclk:1   " &
          "paeb:5      " &
          "RxenbB:6  " &
          "rsoc:7      " &
          "rca:8       " &
          "pafb:9      " &
          "ffb:10      " &
          "resetb:11 " &
          "low:13      " &
          "rrdb:14 " &
          "wclk:21     " &
          "wen1b:23";
END rx_pal;

ARCHITECTURE behavior OF rx_pal IS
SIGNAL count:bit_vector(5 downto 0);
SIGNAL rca_sample: BIT;
SIGNAL high  :BIT := '1';
SIGNAL wclk_d,wen1b_d,rrdb_d:BIT;   -- dummy bits

BEGIN

proc1: PROCESS
- -       VARIABLE CountEnable: BIT;
         BEGIN
```

```
        WAIT UNTIL (rxclk = '1');
-- Reset
                IF resetb = '0'  THEN
                        rca_sample <= '0';
                        Count <= "111111";
-- SET counter to 0 if RSOC goes high
                ELSIF ( rsoc = '1' ) THEN
                        Count <=
                        "000000";
-- Continue putting out data
                  ELSIF  rsoc = '0' AND ffb ='1'  AND
                Count /= "111111" AND rca_sample = '1' THEN
                        Count <= inc_bv(Count); -- increment bit vector
                END IF;

                -- Counter rolls over when count = 53
                        IF Count = "110011" AND rsoc = '0' THEN
                                Count <= "111111";
                         END IF;
                         IF rca = '1' THEN
                        rca_sample <= '1';
                ELSE
                        rca_sample <= '0';
                END IF;
        END process;

proc2: PROCESS
        BEGIN
-- Enable WEN1B to FIFO
                IF ( ffB = '0' ) THEN
                        wen1b_d <= '1';
               ELSE
                        wen1b_d <= '0';
                END IF;
-- Enable RRDB to SUNI
                IF ( (rca = '0' AND Count /= "110011")  OR resetb = '0'
                OR wen1b_d ='1'  OR rxclk = '1')  THEN
                        rrdb <= '1';
                ELSIF ( rca_sample = '1' AND resetb = '1' AND
                wen1b_d ='0'  AND rxclk = '0' ) THEN
                        rrdb <= '0';
                END IF;
-- Enable WCLK to FIFO
                IF ( wen1b_d = '1' AND rxclk = '1' ) THEN
                        wclk <= '1';
                ELSIF ( wen1b_d = '1' AND rxclk = '0' ) THEN
                        wclk <= '0';
                ELSIF ( (rca = '0' AND Count /= "110011")  OR
                resetb = '0'  OR rxclk = '1')  THEN
                        wclk <= '1';
                ELSIF ( rca_sample = '1' AND resetb = '1' AND
                wen1b_d  ='0'  AND rxclk = '0' ) THEN
                        wclk <= '0';
                END IF;
        END process;
          b1:buf port map (wen1b_d,wen1b);
END behavior;
```

DESIGN EQUATIONS (13:27:08)
These equations were extracted from the RX.RPT report file. They can be used or the above VHDL code can be used to generate the proper .JED files. The RX.JED files are available on request.

```
/rrdb =
    ffb * /rxclk * resetb * count_0_.Q * count_1_.Q * /count_2_.Q *
    /count_3_.Q * count_4_.Q * count_5_.Q * rca_sample.Q
  + ffb * /rxclk * resetb * /rrdb * count_0_.Q * count_1_.Q *
    /count_2_.Q * /count_3_.Q * count_4_.Q * count_5_.Q
  + ffb * /rxclk * rca * resetb * rca_sample.Q
  + ffb * /rxclk * rca * resetb * /rrdb

/wclk =
    /rxclk * resetb * count_0_.Q * count_1_.Q * /count_2_.Q *
    /count_3_.Q * count_4_.Q * count_5_.Q * rca_sample.Q
  + /rxclk * resetb * count_0_.Q * count_1_.Q * /count_2_.Q *
    /count_3_.Q * count_4_.Q * count_5_.Q * /wclk
  + /rxclk * rca * resetb * rca_sample.Q
  + /rxclk * rca * resetb * /wclk
  + /ffb * /rxclk

wen1b =
   /ffb

rca_sample.D =
   rca

rca_sample.C =
   rxclk

count_5_.D =
    ffb * count_0_.Q * count_1_.Q * count_2_.Q * count_3_.Q *
    count_4_.Q * rca_sample.Q * /rsoc
  + count_5_.Q * /rsoc
  + /resetb

count_5_.C =
   rxclk

/count_4_.D =
    ffb * resetb * count_0_.Q * count_1_.Q * count_2_.Q * count_3_.Q *
    count_4_.Q * /count_5_.Q * rca_sample.Q
  + resetb * /count_4_.Q * /rca_sample.Q
  + resetb * /count_3_.Q * /count_4_.Q
```

```
    + resetb * /count_2_.Q * /count_4_.Q
    + resetb * /count_1_.Q * /count_4_.Q
    + resetb * /count_0_.Q * /count_4_.Q
    + /ffb * resetb * /count_4_.Q
    + resetb * rsoc

count_4_.C =
     rxclk

count_3_.D =
      ffb * count_0_.Q * count_1_.Q * count_2_.Q * /count_3_.Q *
      rca_sample.Q * /rsoc
    + count_0_.Q * count_1_.Q * /count_2_.Q * count_4_.Q * count_5_.Q *
     /rsoc
    + count_3_.Q * count_4_.Q * count_5_.Q * /rsoc
    + /count_2_.Q * count_3_.Q * /rsoc
    + /count_1_.Q * count_3_.Q * /rsoc
    + /count_0_.Q * count_3_.Q * /rsoc
    + count_3_.Q * /rca_sample.Q * /rsoc
    + /ffb * count_3_.Q * /rsoc
    + /resetb

count_3_.C =
     rxclk

count_2_.D =
      count_0_.Q * count_1_.Q * /count_2_.Q * /count_3_.Q * count_4_.Q *
      count_5_.Q * /rsoc
    + ffb * count_0_.Q * count_1_.Q * /count_2_.Q * rca_sample.Q *
     /rsoc
    + count_2_.Q * count_3_.Q * count_4_.Q * count_5_.Q * /rsoc
    + count_2_.Q * /rca_sample.Q * /rsoc
    + /ffb * count_2_.Q * /rsoc
    + /count_1_.Q * count_2_.Q * /rsoc
    + /count_0_.Q * count_2_.Q * /rsoc
    + /resetb

count_2_.C =
     rxclk

count_1_.D =
      count_1_.Q * /count_2_.Q * /count_3_.Q * count_4_.Q * count_5_.Q *
     /rsoc
    + count_1_.Q * count_2_.Q * count_3_.Q * count_4_.Q * count_5_.Q *
     /rsoc
    + ffb * count_0_.Q * /count_1_.Q * rca_sample.Q * /rsoc
```

```
     + count_1_.Q * /rca_sample.Q * /rsoc
     + /ffb * count_1_.Q * /rsoc
     + /count_0_.Q * count_1_.Q * /rsoc
     + /resetb

  count_1_.C =
      rxclk

  count_0_.D =
       count_0_.Q * count_1_.Q * /count_2_.Q * /count_3_.Q * count_4_.Q *
       count_5_.Q * /rsoc
     + count_0_.Q * count_1_.Q * count_2_.Q * count_3_.Q * count_4_.Q *
       count_5_.Q * /rsoc
     + ffb * /count_0_.Q * rca_sample.Q * /rsoc
     + count_0_.Q * /rca_sample.Q * /rsoc
     + /ffb * count_0_.Q * /rsoc
     + /resetb

  count_0_.C =
      rxclk
```

```
-- UTOPIA interface PAL U17
-- Used to interface the Vicksburg Motherboard F-FRED chip
--     to the SUNI transmit FIFOs


USE  work.bv_math.all;                          -- necessary for inc_bv();
USE  work.rtlpkg.all;

ENTITY tx_pal IS
          PORT    (txclk, resetb, tsoc, tca, TxenbB, low, TxClavB: IN BIT;
                    twrb, bufclk, tsoc_out, TxFullB: OUT BIT);

ATTRIBUTE order_code of tx_pal:ENTITY is "PAL22V10D-10PC";
ATTRIBUTE part_name of tx_pal:ENTITY IS "C22V10";
ATTRIBUTE pin_numbers of tx_pal:ENTITY IS
          "txclk:1    " &
          "TxenbB:3   " &
          "TxClavB:6  " &
          "tsoc:7     " &
          "tca:9      " &
          "resetb:11  " &
          "low:13     " &
          "twrb:15    " &
          "bufclk:22  " &
          "TxFullB:23";
END tx_pal;

ARCHITECTURE behavior OF tx_pal IS
SIGNAL CountTemp: BIT_VECTOR(5 DOWNTO 0);
SIGNAL  TxEnbB_sample,twrb_en:  BIT;
BEGIN

proc1:  PROCESS
- -       VARIABLE CountEnable: BIT;
          BEGIN
          WAIT UNTIL (txclk = '1');
-- Sample TxEnbB
                    IF (TxEnbB = '1' OR TxClavb = '1' )
                    AND CountTemp = "111111" THEN
                              TxEnbB_sample <= '1';
                    ELSE
```

```
                                  TxEnbB_sample
                          <= '0'; END IF;
-- Resetb = 0
                          IF resetb = '0' THEN
                                  CountTemp <= "111111";
                                  TxEnbB_sample <= '1';
-- SET counter to 0 if TSOC goes high AND TxEnbB is low
                          ELSIF ( tsoc = '1' AND TxEnbB_sample = '0') THEN
                                  CountTemp <= "000000";
-- Put out only the first byte of data if TxClavB is active (0) ELSIF
                          TxClavB = '0'  AND CountTemp /= "111111" AND tca = '1'
                          AND TxEnbB_sample = '0' THEN
                                  CountTemp <= inc_bv(CountTemp);
                          END IF;
-- Counter rolls over when count = 53
                          IF CountTemp = "110100" THEN
                                  CountTemp <= "111111";
                          END IF;
                  END process;
proc2:  PROCESS
                  BEGIN
                          IF (CountTemp = "110010" OR CountTemp = "110011" OR
                          CountTemp = "110100" OR CountTemp = "110100" OR
                          resetb = '0'   OR tca = '0' ) THEN
                                TxFullB <= '0';
                          ELSE
                                TxFullB <= '1';
                          END IF;
-- Enable TWRB for the rest of the cell
                           IF (tca = '1' AND TSOC = '0' AND resetb = '1' AND
                           CountTemp /= "111111" AND TxEnbB_sample ='0') THEN
                                twrb_en <= '1';
                          ELSE
                                twrb_en <= '0';
                          END IF;
                          IF txclk = '0' AND twrb_en = '1'  THEN
                                  twrb <= '0';
                           ELSE
                                  twrb <= '1';
                          END IF;
```

```
            IF txclk = '0' THEN
                bufclk <= '1';
            ELSE
                bufclk <= '0';
            END IF;
    END process;
END behavior;
```

DESIGN EQUATIONS (19:56:20)

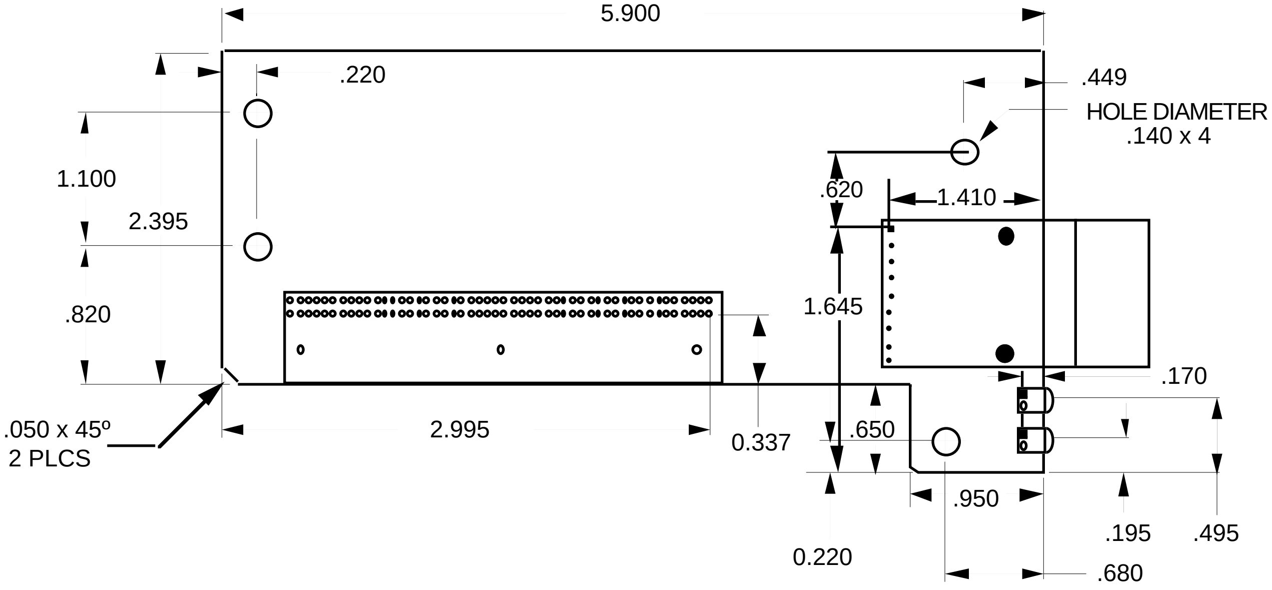
These equations were extracted from the TX.RPT report file. They can be used or the above VHDL code can be used to generate the proper .JED files. The TX.JED files are available on request.

```
   twrb =
        counttemp_0_.Q * counttemp_1_.Q * counttemp_2_.Q *
        counttemp_3_.Q * counttemp_4_.Q * counttemp_5_.Q
      + txenbb_sample.Q
      + txclk
      + tsoc
      + /tca
      + /resetb

   bufclk =
       /txclk

   /txfullb =
        /counttemp_0_.Q * /counttemp_1_.Q * counttemp_2_.Q *
        /counttemp_3_.Q * counttemp_4_.Q * counttemp_5_.Q
      + counttemp_1_.Q * /counttemp_2_.Q * /counttemp_3_.Q *
        counttemp_4_.Q * counttemp_5_.Q
      + /tca
      + /resetb

   counttemp_5_.D =
        tca * /tsoc * counttemp_0_.Q * counttemp_1_.Q * counttemp_2_.Q *
        counttemp_3_.Q * counttemp_4_.Q * /txenbb_sample.Q * /txclavb
      + /counttemp_0_.Q * /counttemp_1_.Q * counttemp_2_.Q *
        /counttemp_3_.Q * counttemp_4_.Q * counttemp_5_.Q
      + /tsoc * counttemp_5_.Q
      + counttemp_5_.Q * txenbb_sample.Q
      + /resetb

   counttemp_5_.C =
       txclk

   counttemp_4_.D =
        tca * /tsoc * counttemp_0_.Q * counttemp_1_.Q * counttemp_2_.Q *
        counttemp_3_.Q * /counttemp_4_.Q * /txenbb_sample.Q * /txclavb
      + /counttemp_0_.Q * /counttemp_1_.Q * counttemp_2_.Q *
        /counttemp_3_.Q * counttemp_4_.Q * counttemp_5_.Q
      + /tsoc * counttemp_4_.Q * counttemp_5_.Q
      + /tsoc * /counttemp_3_.Q * counttemp_4_.Q
      + /tsoc * /counttemp_1_.Q * counttemp_4_.Q
      + /tsoc * /counttemp_0_.Q * counttemp_4_.Q
```

```
     + /tsoc * /counttemp_2_.Q * counttemp_4_.Q
     + /tsoc * counttemp_4_.Q * txclavb
     + /tca * /tsoc * counttemp_4_.Q
     + counttemp_4_.Q * txenbb_sample.Q
     + /resetb

 counttemp_4_.C =
     txclk

 counttemp_3_.D =
      tca * /tsoc * counttemp_0_.Q * counttemp_1_.Q * counttemp_2_.Q *
      /counttemp_3_.Q * /txenbb_sample.Q * /txclavb
     + /counttemp_0_.Q * /counttemp_1_.Q * counttemp_2_.Q *
      /counttemp_3_.Q * counttemp_4_.Q * counttemp_5_.Q
     + /tsoc * counttemp_3_.Q * counttemp_4_.Q * counttemp_5_.Q
     + /tsoc * /counttemp_2_.Q * counttemp_3_.Q
     + /tsoc * /counttemp_1_.Q * counttemp_3_.Q
     + /tsoc * /counttemp_0_.Q * counttemp_3_.Q
     + /tsoc * counttemp_3_.Q * txclavb
     + /tca * /tsoc * counttemp_3_.Q
     + counttemp_3_.Q * txenbb_sample.Q
     + /resetb

 counttemp_3_.C =
     txclk

 counttemp_2_.D =
      tca * /tsoc * counttemp_0_.Q * counttemp_1_.Q * /counttemp_2_.Q *
      /txenbb_sample.Q * /txclavb
     + /counttemp_0_.Q * /counttemp_1_.Q * counttemp_2_.Q *
      /counttemp_3_.Q * counttemp_4_.Q * counttemp_5_.Q
     + /tsoc * counttemp_2_.Q * counttemp_3_.Q * counttemp_4_.Q *
      counttemp_5_.Q
     + /tsoc * /counttemp_1_.Q * counttemp_2_.Q
     + /tsoc * /counttemp_0_.Q * counttemp_2_.Q
     + /tsoc * counttemp_2_.Q * txclavb
     + /tca * /tsoc * counttemp_2_.Q
     + counttemp_2_.Q * txenbb_sample.Q
     + /resetb

 counttemp_2_.C =
     txclk

 counttemp_1_.D =
      /tsoc * counttemp_1_.Q * counttemp_2_.Q * counttemp_3_.Q *
      counttemp_4_.Q * counttemp_5_.Q
```

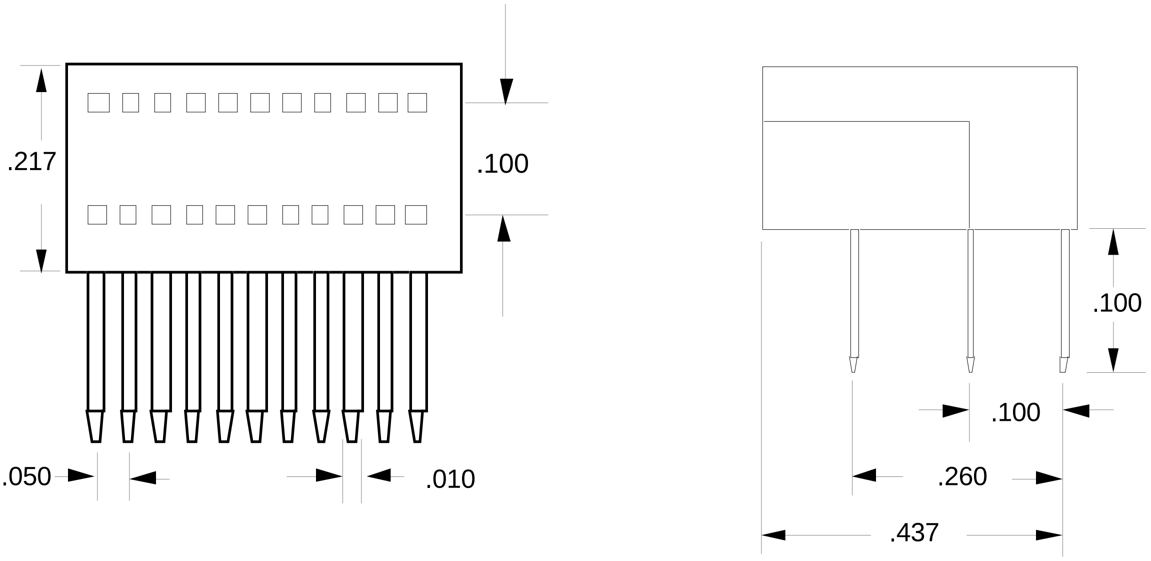
```
    + tca * /tsoc * counttemp_0_.Q * /counttemp_1_.Q *
     /txenbb_sample.Q * /txclavb
    + /counttemp_0_.Q * /counttemp_1_.Q * counttemp_2_.Q *
     /counttemp_3_.Q * counttemp_4_.Q * counttemp_5_.Q
    + /tsoc * /counttemp_0_.Q * counttemp_1_.Q
    + /tsoc * counttemp_1_.Q * txclavb
    + /tca * /tsoc * counttemp_1_.Q
    + counttemp_1_.Q * txenbb_sample.Q
    + /resetb

counttemp_1_.C =
     txclk

counttemp_0_.D =
     /tsoc * counttemp_0_.Q * counttemp_1_.Q * counttemp_2_.Q *
     counttemp_3_.Q * counttemp_4_.Q * counttemp_5_.Q
    + /counttemp_0_.Q * /counttemp_1_.Q * counttemp_2_.Q *
     /counttemp_3_.Q * counttemp_4_.Q * counttemp_5_.Q
    + tca * /tsoc * /counttemp_0_.Q * /txenbb_sample.Q * /txclavb
    + /tsoc * counttemp_0_.Q * txclavb
    + /tca * /tsoc * counttemp_0_.Q
    + counttemp_0_.Q * txenbb_sample.Q
    + /resetb

counttemp_0_.C =
     txclk

txenbb_sample.D =
     counttemp_0_.Q * counttemp_1_.Q * counttemp_2_.Q *
     counttemp_3_.Q * counttemp_4_.Q * counttemp_5_.Q * txclavb
    + counttemp_0_.Q * counttemp_1_.Q * counttemp_2_.Q *
     counttemp_3_.Q * counttemp_4_.Q * counttemp_5_.Q * txenbb
    + /resetb

txenbb_sample.C =
     txclk
```

APPENDIX B: MECHANICAL DRAWINGS



Unit: inches

NSC_SAPI MECHANICAL DRAWING



AMP 101911-8 Edge Connector

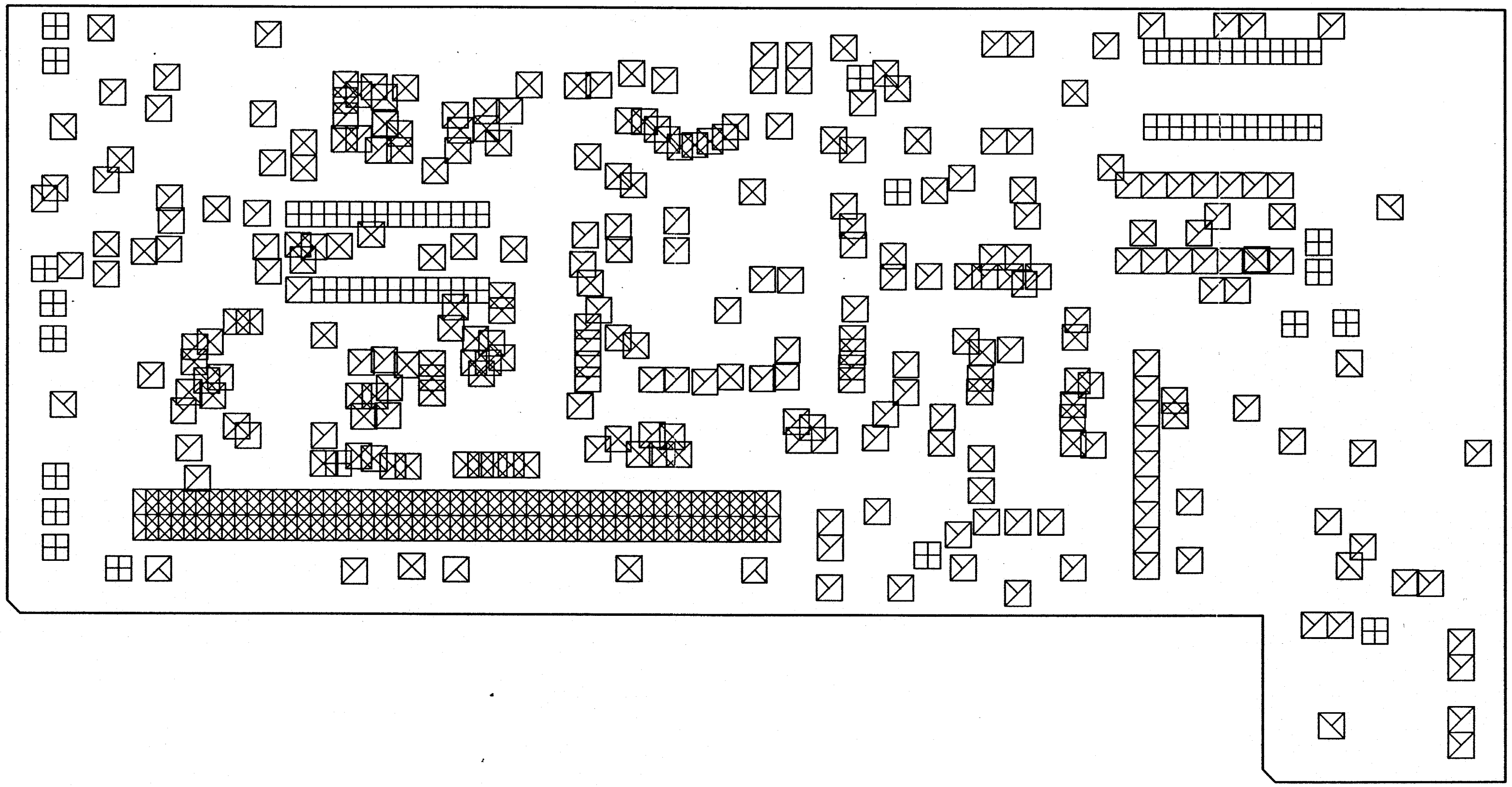
Note: 100 pin, 100 position

APPENDIX C: MATERIAL LIST

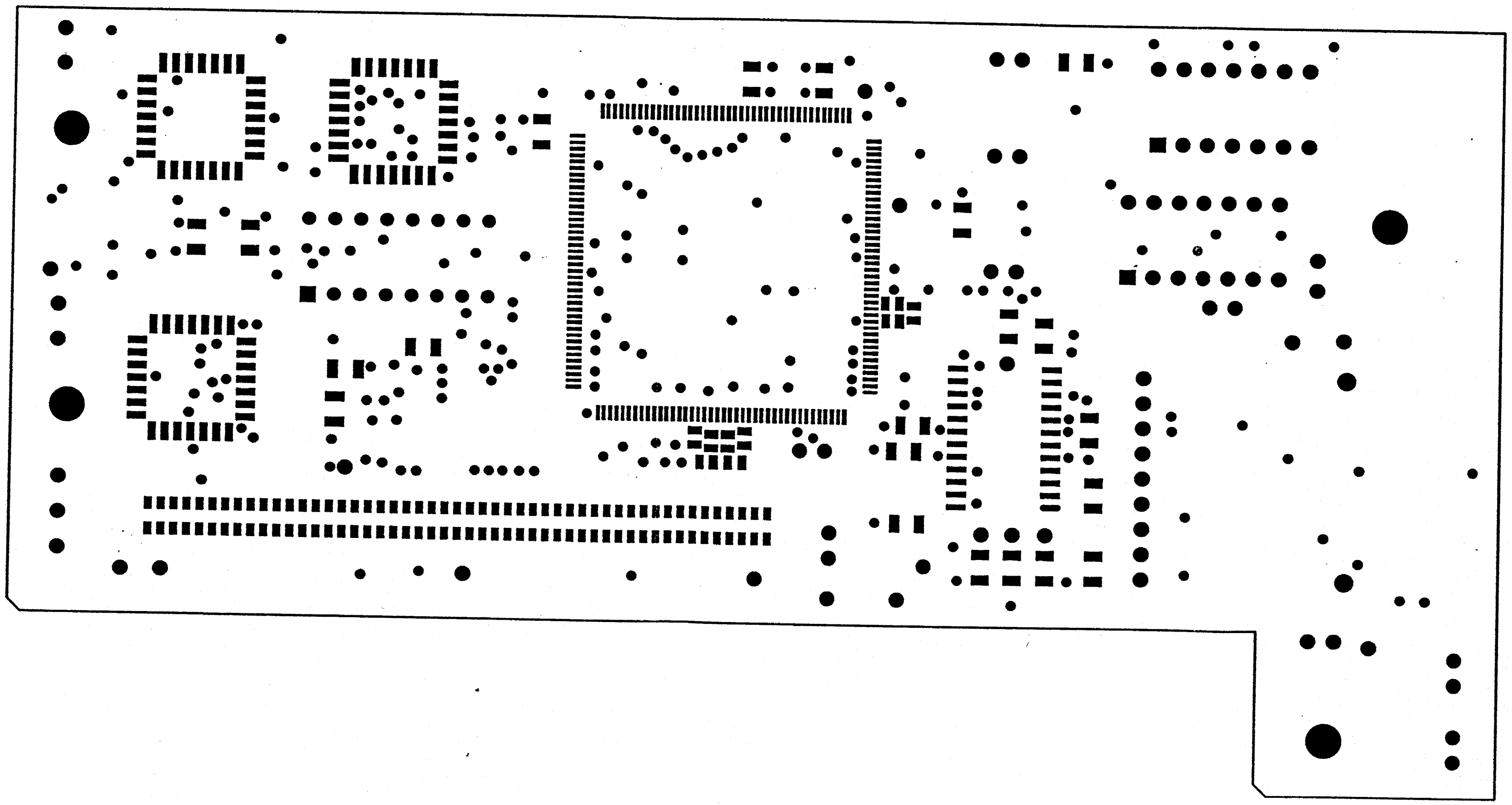
Item	Qty	Reference	Description
1	1	E1	19.44 MHz 10ppm DIP Osc, .5" case, PECL levels, Connor-Winfield ECLFP5Q-19.44 MHz
2	1	U10	Saturn User Network Interface, 160 QFP, 0.025" pitch PMC-Sierra PM5345-RC
3	1	U2	SONET/SDH Serial Transceiver, clock and data recovery, 24-pin SOIC, Cypress CY7B951
4	3	U12, U16, U17	CMOS PALs, 10ns prop, 28-pin PLCC, Cypress, PAL22CV10D-10JC
5	2	U18, U19	CMOS bus interface register, 10 bit, 24-pin SOIC J-bend, IDT74FCT821Y
6	1	U1	parallel synchronous FIFO, 1024x9 bit, 20 Mhz, 32-pin PLCC, IDT72221L20J for PLCC
7	1	U4	octal 3-state inverting buffer, 20-pin SOIC, Motorola 74HCT240DW
8	1	U11	745288 ROM, 32x8 ROM, 16pin DIP, AMD Am27S19, Or TBP18S030, or equivalent DIP ROM
9	1	U3	Fibre Optics transceiver, 9 pin, AT&T 1408A
10	1	J1	edge connector, 100 pin, 100 position, 0.050" pitch, AMP 103911-8
11	5	L1, L2, L4, L5, L6	ferrite beads, 0.2", SMT, Fair-Rite #2743019446
12	1	D1	LED, yellow, 0.1" spacing, right angle
13	1	D2	LED, green, 0.1" spacing, right angle
14	6	C45, C46, C47, C48, C49, C50	capacitors, 0.01 pF ceramic 50V, surface mount 805
15	1	C53	capacitor, 0.01 uF ceramic 50V, surface mount 1206
16	27	C1, C2, C3, C4, C5, C6, C7, C10, C11, C13, C16, C17, C19, C28, C29, C30, C31, C32, C33, C34, C36, C37, C40, C41, C42, C44, C54	capacitors, 0.1 uF ceramic 100V, 1206

17	6	C20, C21, C22, C23, C51, C52	capacitors, 10uF solid tantalum 25V, radial leads, 0.1" spacing
18	1	C25	capacitor, 100uF electrolytic 25V, radial leads, 0.1 spacing
19	2	R19, R21	resistors, 75 Ohm, 1/4 Watt, MF 1%, type 1206 SMT
20	2	R10, R11	resistors, 59 Ohm, 1/4 Watt, MF 1%, type 1206 SMT
21	3	R35, R36, R37	resistors, 200 Ohm, MF 1%, type 805 SMT
22	3	R22, R27, R30	resistors, 200 Ohm, 1/4 Watt, MF 1%, type 1206 SMT
23	13	R1, R2, R3, R4, R5, R6, R7, R8, R9, R23, R24, R28, R29	resistors, 330 Ohm, 1/4 Watt, MF 1%, type 1206 SMT
24	2	R12, R13	resistors, 312 Ohm, 1/4 Watt, MF 1%, type 1206 SMT
25	2	R14, R15	resistors, 1.2K Ohm, 1/4 Watt, MF 1%, type 1206 SMT
26	1	R34	resistors, 630 Ohm, 1/4 Watt, MF 1%, type 1206 SMT
27	1	R33	resistors, 3.3K Ohm, 1/4 Watt, MF 1%, type 1206 SMT
28	8	R16, R17, R18, R20, R31, R32, R38, R39	resistors, 4.7K Ohm, 1/4 Watt, MF 1%, type 1206 SMT

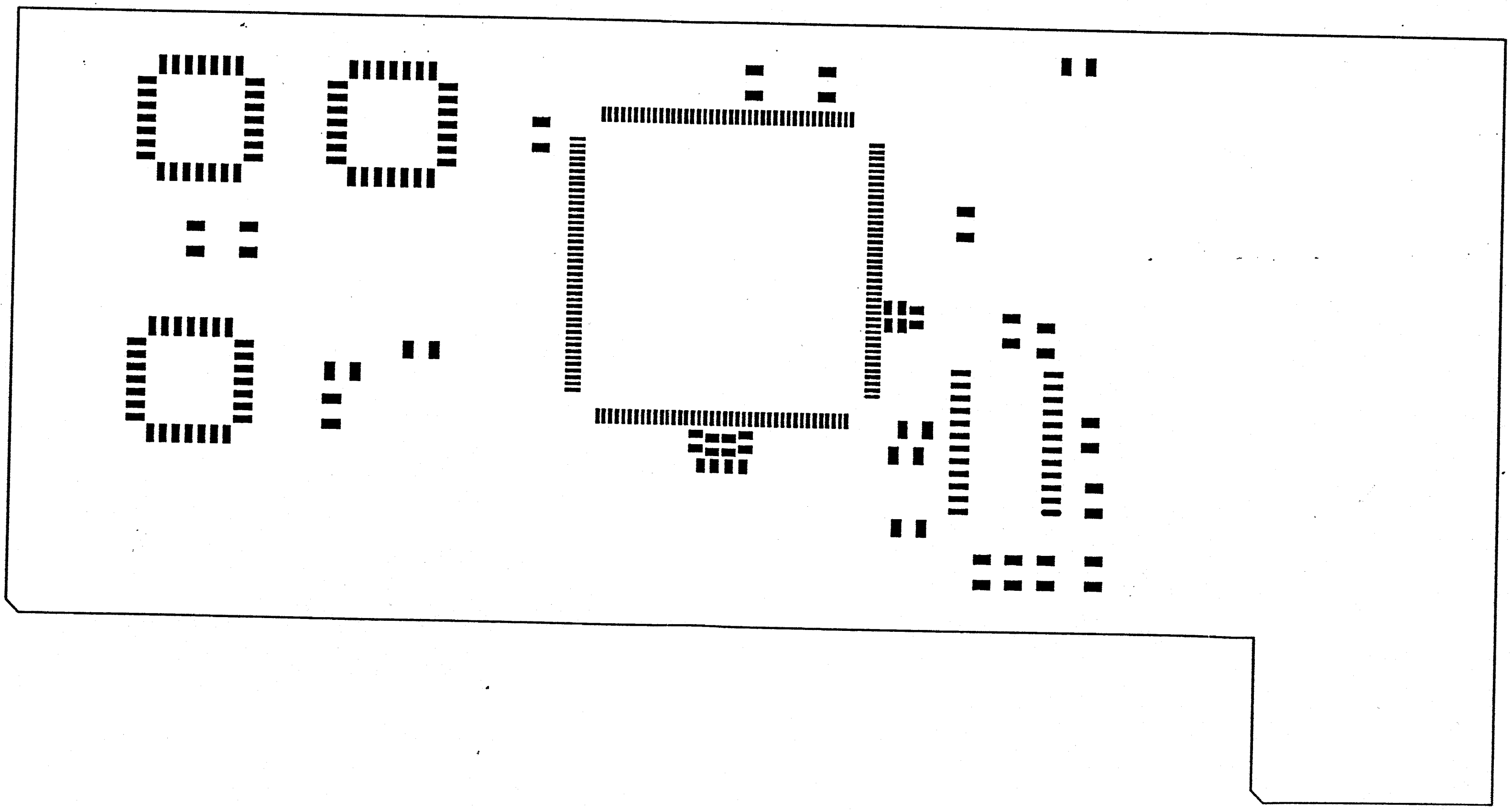
APPENDIX D: COMPONENT PLACEMENT



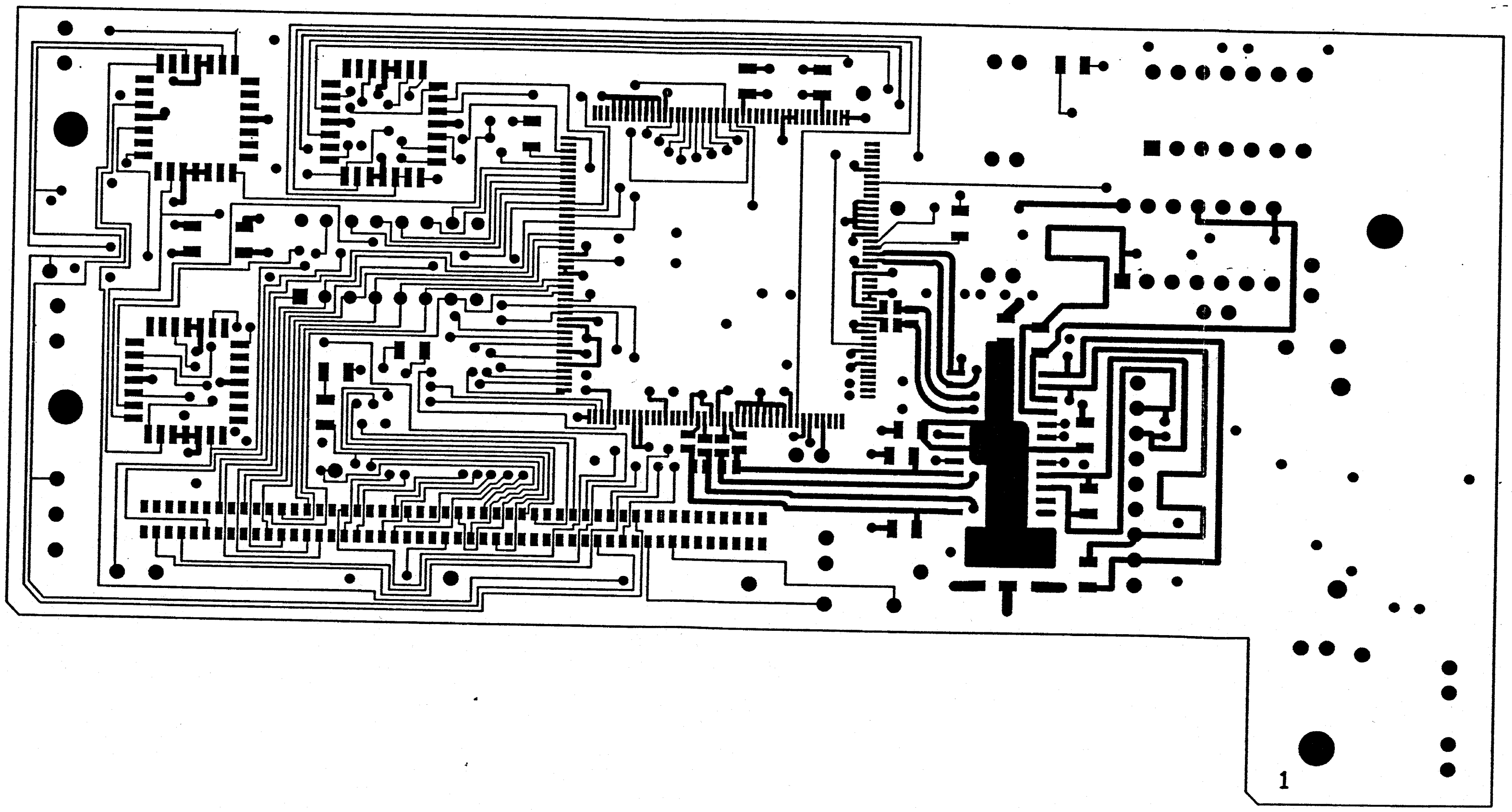
SAPI_1-1 Drill Drawing



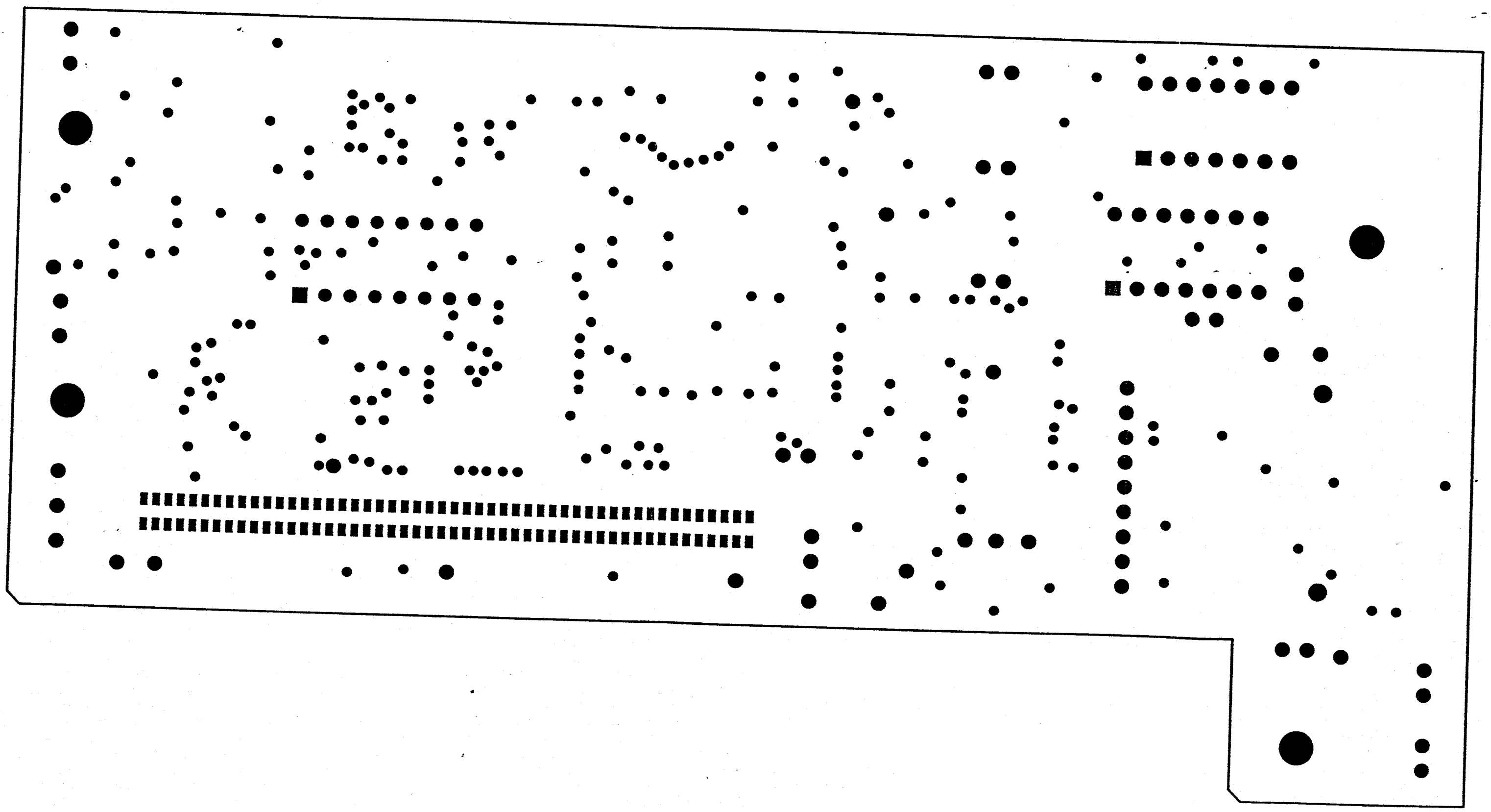
SAPI_1-1 Top Solder Mask



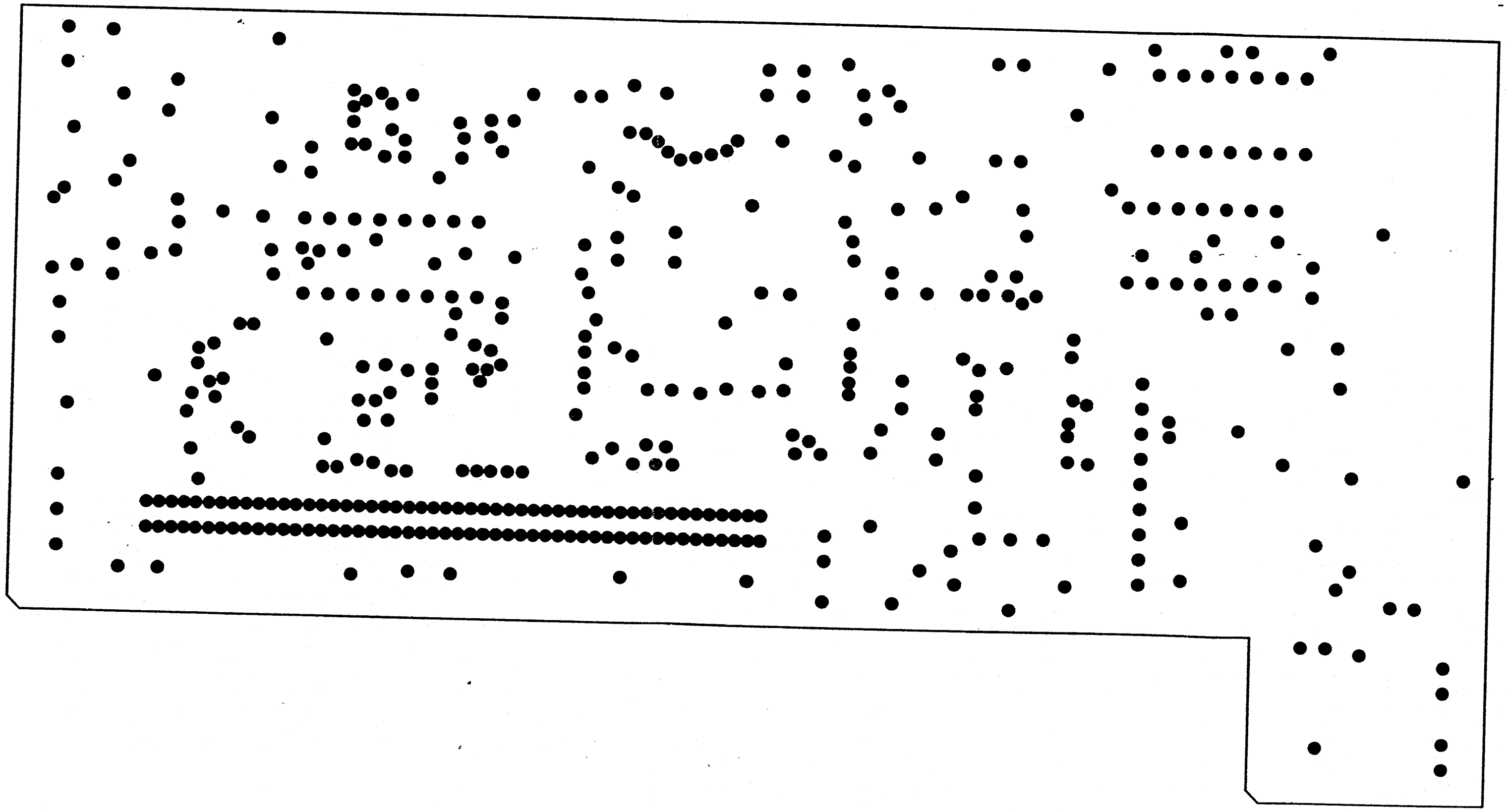
SAPI_1-1 Top Paste Mask



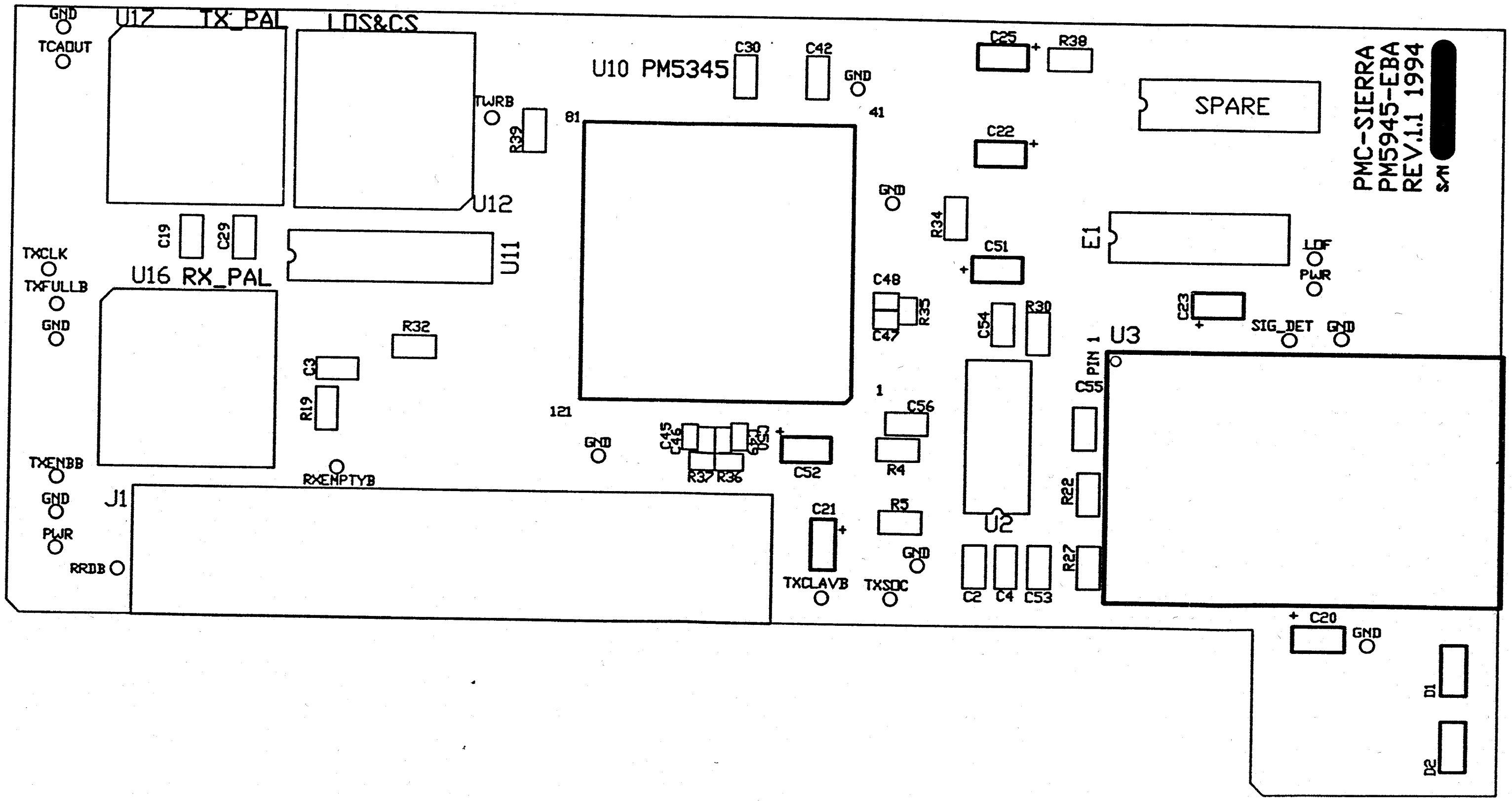
SAPI_1-1 Top Layer



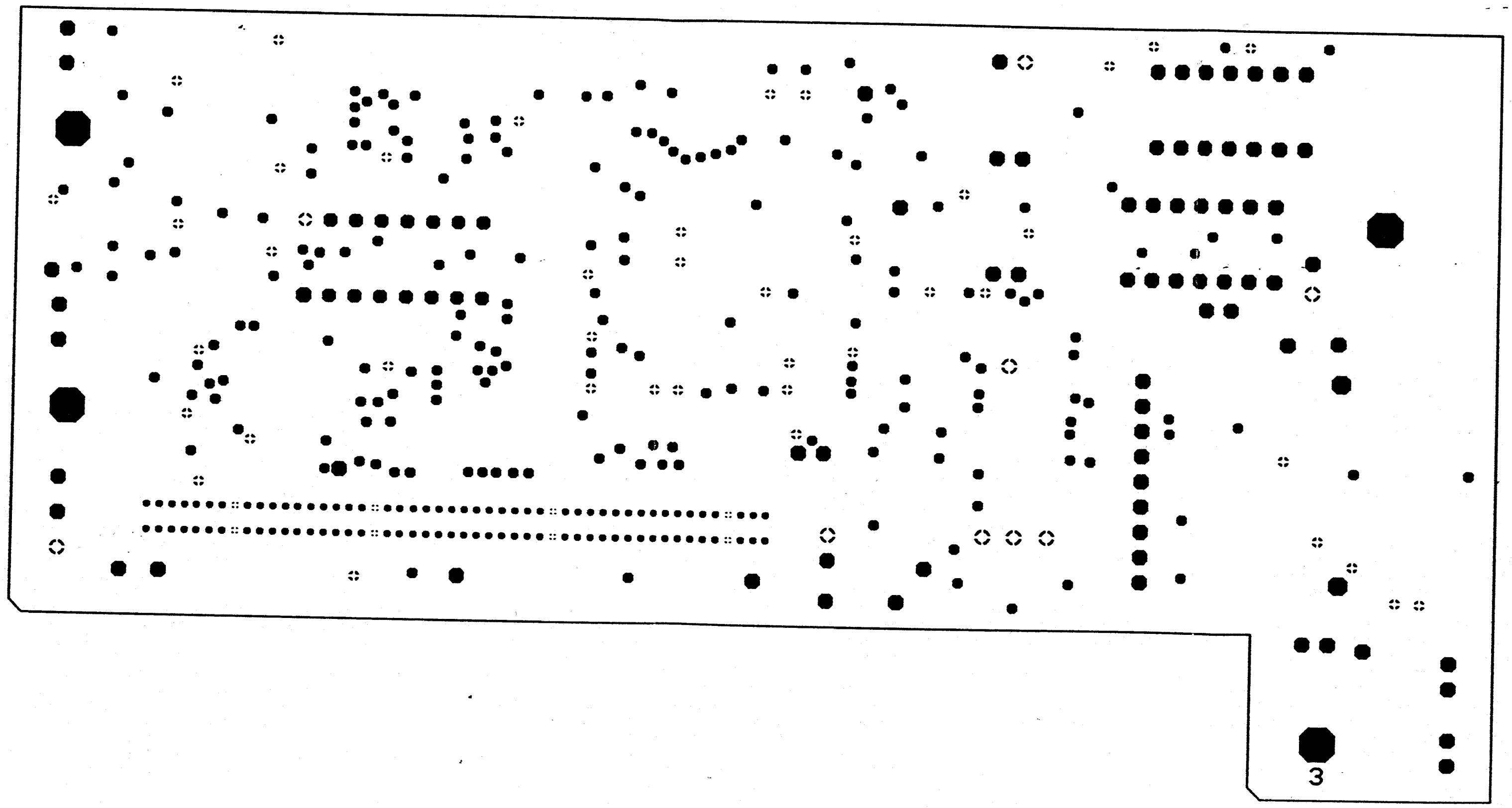
SAPI_1-1 Pad Master



SAPI_1-1 Drill Guide



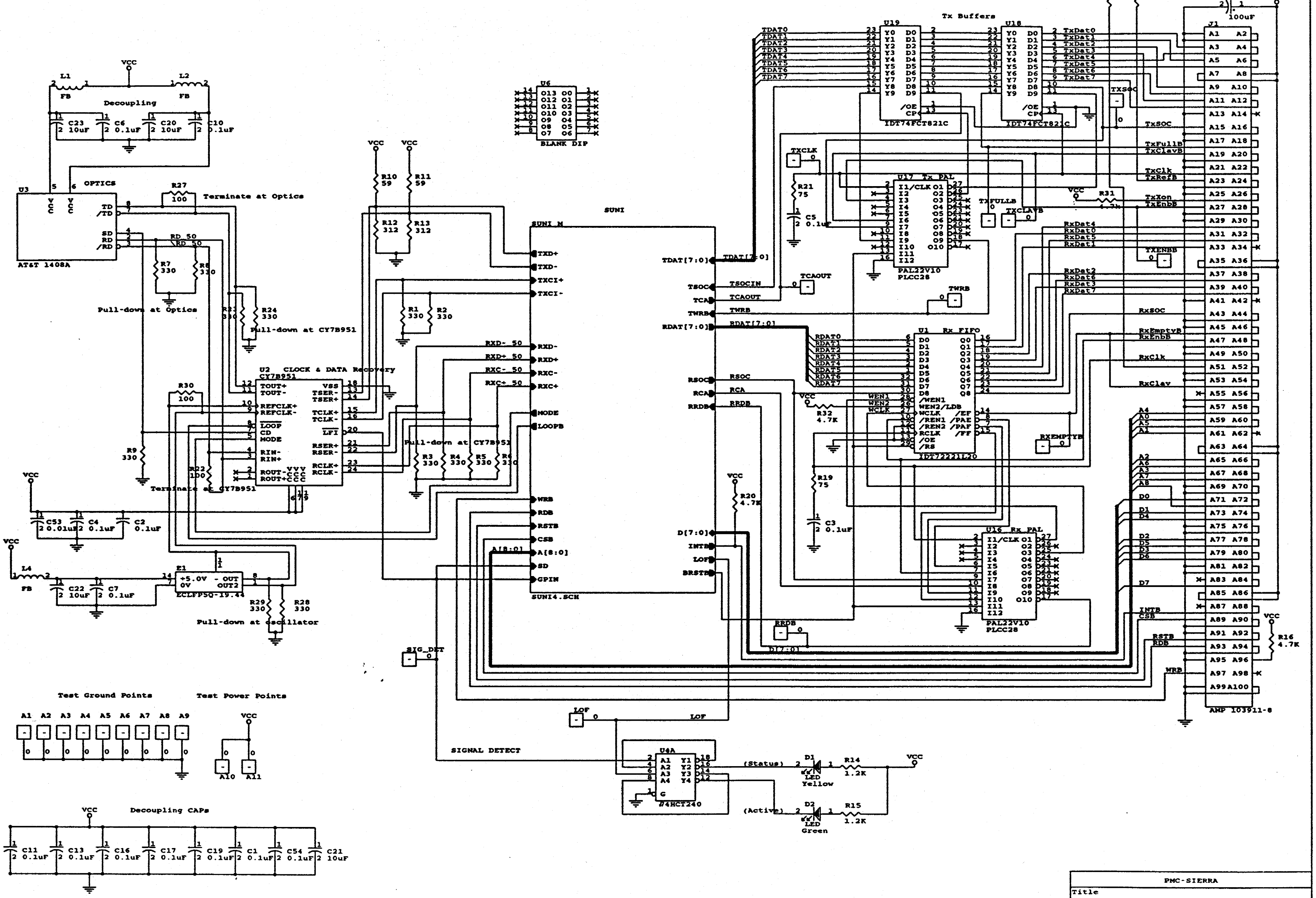
SAPI_1-1 Top Overlay



SAPI_1-1 Power Plane

APPENDIX E: SCHEMATICS

1. Place all decoupling capacitors on the bottom side of PCB.
2. Use only surface mount inductors, resistors and capacitors.
3. Place termination resistors and capacitors as close as possible to the terminating side.
4. Place the pull-down resistors as close as possible to the sourcing device and on the bottom side.
5. Place the power supply decoupling capacitors as close a possible to the VCC pins.
6. The 0.1uF capacitors should be high-quality ceramic devices rated for RF applications.
7. Traces labeled with NAME_50 should have a characteristic impedance of 50 ohms.
8. Keep all 50 ohm traces as short as possible.
9. All inductors are Fair-Rite Products Corp # 2743002111

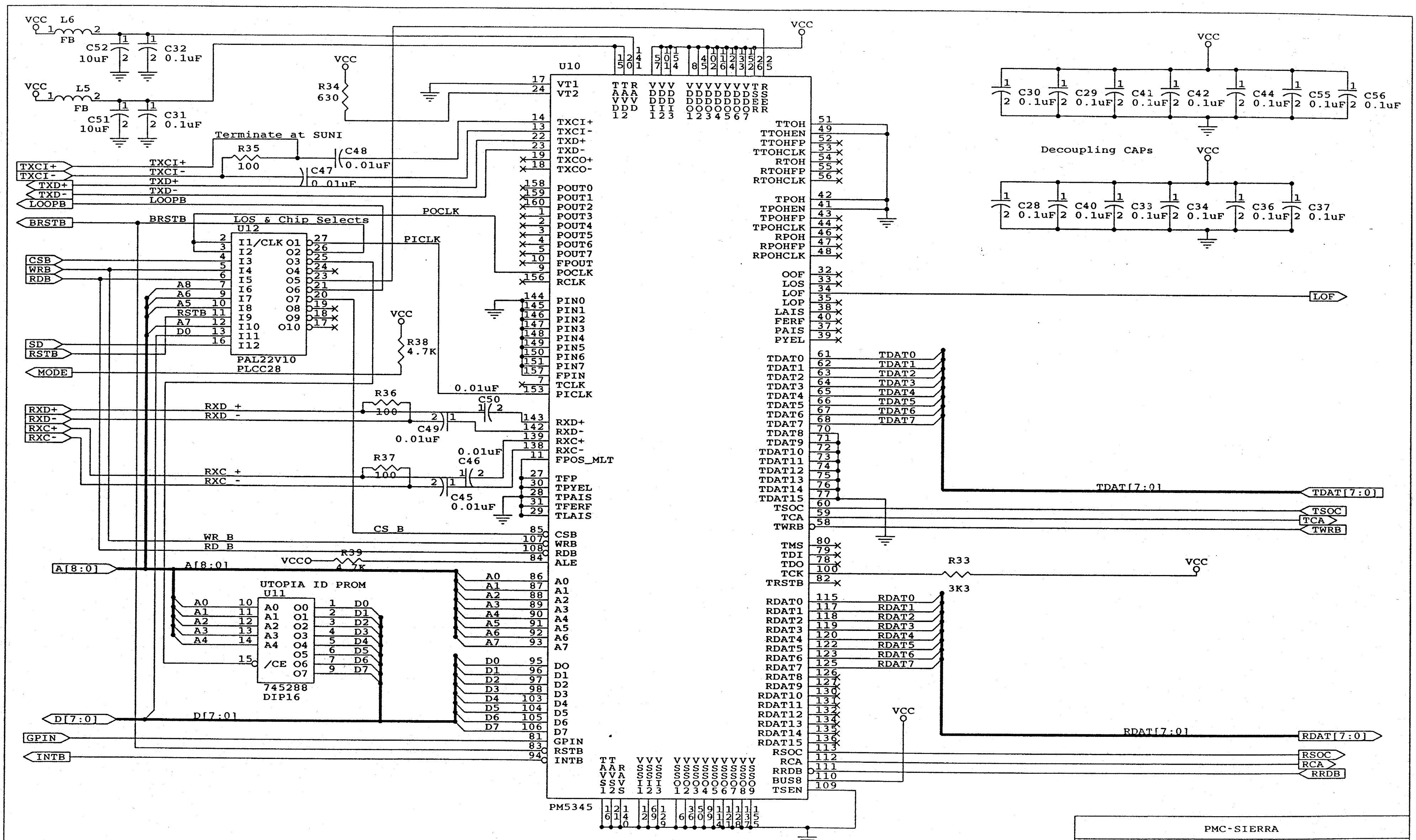


PMC-SIERRA

Title
SONET ATM PHY INTERFACE (SAPI) BOARD

Size	Document Number		REV
C	PMC-940106	PM5945	1.1

Date: August 8, 1994 Sheet 1 of 2



PMC-SIERRA

Title		
	SUNI	
Size B	Document Number	REV 1.1
Date: August 8, 1994	Sheet 2 of 2	

APPENDIX F: LAYOUT NOTES

Background

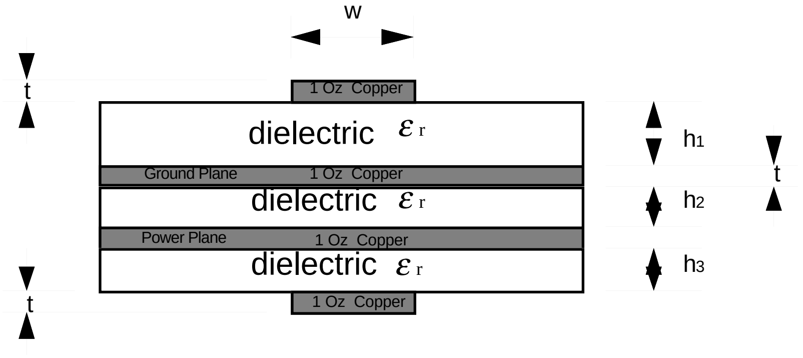
The SAPI board is a 4-layer board that has both throughole and surfacemount components. Protel's Autotrax version 2.0 for DOS is used to layout the board. The schematics is done using OrCAD. Layer 1 and 4 are signal layers. Layer 2 and 3 are ground and power respectively..

Trace Impedance Control

To reduce signal degradation due to reflection and radiation, the impedance of the traces that carry high speed signals such as transmitted and received data should be treated as microstrip transmission lines and terminated with matching impedance. The calculation of the trace width is calculated using the formula

$$Z_o = \frac{87}{\sqrt{\varepsilon_r + 1.41}} \times \ln\left(\frac{5.98 \times h}{0.8 \times w + t}\right)$$

and based on the following layer setup:


w
t
1 Oz Copper
dielectric ε_r
Ground Plane
1 Oz Copper
dielectric ε_r
Power Plane
1 Oz Copper
dielectric ε_r
1 Oz Copper
t
h1
t
h2
h3

where

ε_r = relative dielectric constant, nominally 5.0 for G-10 fibre-glass epoxy

t = thickness of the copper, fixed according to the weight of copper selected. For 1 oz copper, the thickness is 1.4 mil. This thickness can be ignored if w is great enough.

h1, h2, h3 = thickness of dielectric.

w = width of copper

The parameters h1, h2, and h3 can be specified. For example, if a 20 mil (including the copper thickness on both sides of the board) two layer core is selected, dielectric material that has the same relative dielectric constant can be added to the both sides of the core to construct a 4 layer board.

Since all the controlled impedance traces are on the component side, only h1 is relevant in calculating the trace width. The calculation for the reference design is shown in the tables below:

Parameters	Min	Nominal	Max
Board Thickness (mil)		62.5 (including copper thickness)	
Separataion between layers 1 and 2 (mil)		14	
Separation between layers 2 and 3 (mil)		28	
Separation between layers 3 and 4 (mil)		14	
Relative dielectric constant	4.8		5.4

Parameter	Data			
ε_r	4.8	5.4	4.8	5.4
h (mil)	14	14	14	14
t (mil)	1.4	1.4	1.4	1.4
Zo (Ohm)	50	50	100	100
W (mil)	23.2	21.6	4.2	3.5

Since h1 is directly proportional to the width of the traces, a small h1 will result in the traces being too thin to be accurately fabricated. Wider traces can be more precisely manufactured, but they take up too much board space. Therefore, the thickness of the board should be chosen so that the traces take up as little board space as possible yet still leaving enough margin to allow accurate fabrication.

The low speed signals use 8 to 10 mil traces. Power and ground traces are all as wide as the pads they connect to, up to a maximum width of 24 mil. All 50 Ohm traces are 24 mil wide.

Routing

Routing is based on the design considerations as well as manufacturability. Several suggestions are listed below:

- Turns and corners should be rounded to curves to avoid discontinuity in the signal path.
- Allow at least 10 mil clearance among vias, traces, and pads to prevent short and reduce crosstalk. If possible, allow 20 mil or more clearance around vias as manufacturers may have minimum clearance requirements. For the traces that run between pads of the 100 pin edge connector, clearance of 6 mil and trace width of 8 mil can be used. However, the number and lengths such traces should be kept to a minimum.
- The differential signal pairs should be of equal length so that both signals arrive at the inputs at the same time. They should also run parallel and close to one another for as long as possible so that noise will couple onto both lines and become common mode noise which is ignored by the differential inputs. Even though single ended inputs should not run parallel to one another in close proximity, since all of the single ended signals that run parallel to one another on the UTOPIA interface side are low speed signals and are sampled after they have all settled down, they should not cause any concern.
- All power and ground traces should be made as wide as possible, up to 24 mil to provide low impedance paths for the supply current as well as to allow quick noise dissipation.
- The oscillator used is a 14 pin DIP package. The connections to the oscillator is setup so that an oscillator with a smaller footprint (8 pin) can also be plugged in to save board space.

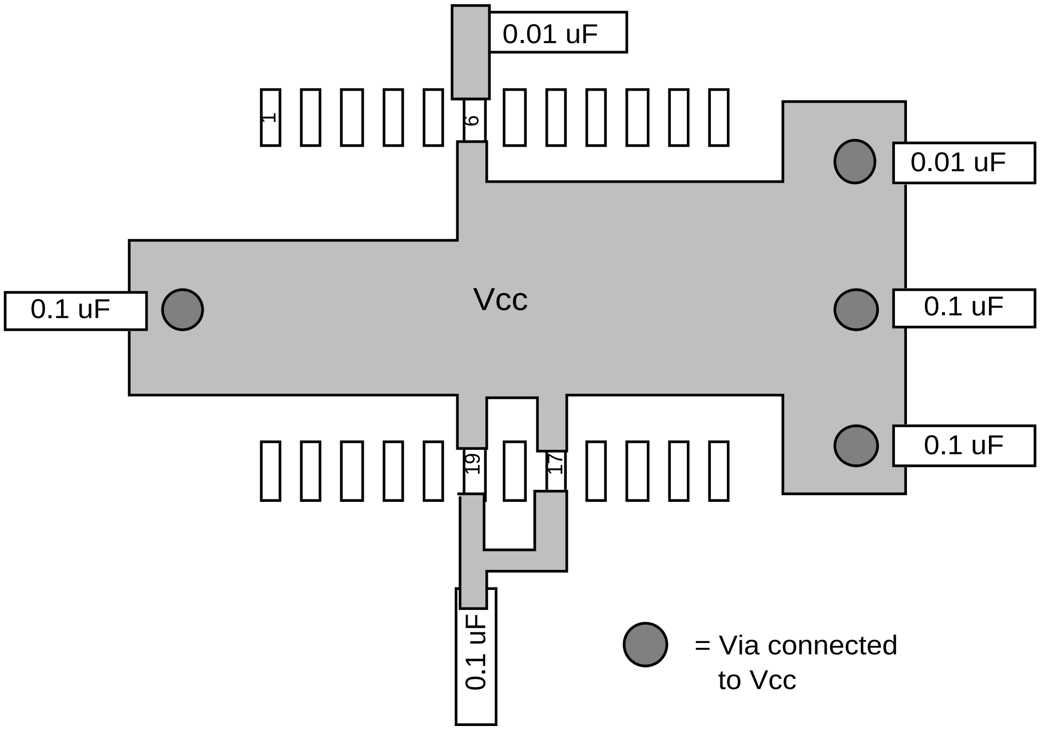
Power, Ground, and Decoupling Capacitors

Only one supply voltage, nominally +5 Volts, is used by all devices on the board and referenced to by all PECL signals. One solid ground plane is also used. Ferrite beads are deployed to prevent digital noise from entering analog circuits of the SUNI, the PECL oscillator, and the optic transceiver.

Bypass capacitors can supply transient current and help filter out power and ground noise. They are placed as close to the pins as possible. Minimum of one 0.1 uF bypass capacitor per device is used. Wherever possible, one 0.1 uF bypass capacitor is placed at each power pin of each IC. For high speed IC's, such as the CY7B951, an additional 0.01 uF bypass capacitor is added to each power pin. A 10 uF electrolytic bypass capacitor is also deployed by the SUNI, the oscillator, and the CY7B951 devices. A large electrolytic bypass capacitor (47 to 100 uF) should be placed as near the power supply as possible.

Special Power and Ground Requirements of CY7B951

A special power plane is provided on the component side for the Cypress CY7B951 device. The power plane under the IC provides a low impedance path connecting pin 6, 17, and 19.



Power Plane and Decoupling of CY7B951

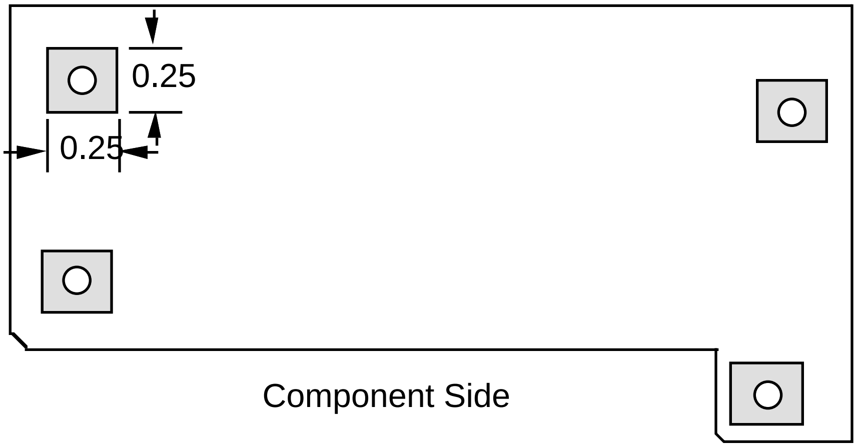
Pin 6 of the CY7B951 provides current for all output pins and is internally connected to pin 17 and 19. Its voltage fluctuates as the outputs switch. When the voltage difference between pin 6 and pins 17 and 19 will be amplified, causing the voltage fluctuation on pin 6 to increase. When the voltage at pin 6 fluctuates, the outputs it drives will start to draw more current which causes the voltage on pin 6 to fluctuate further. Testing has shown this fluctuation can reach 2 V p-p.

The low impedance power plane puts pin 6, 17, and 19 at the same voltage level so that if pin 6 fluctuates due to outputs switching, pin 17 and 19 will follow, preventing any voltage difference to be established between them.

Mounting Hole Clearance Requirements

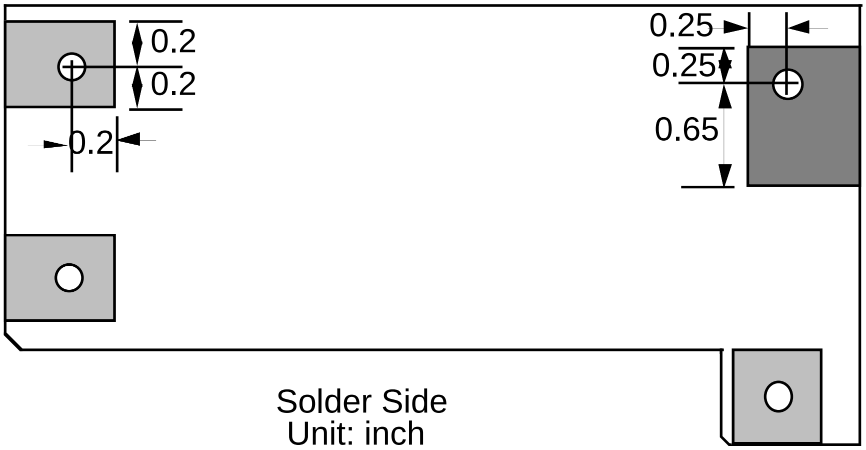
The following clearances are required in order for the board to be mounted onto the Vicksburg Motherboard:

- On the component side, each mounting hole should have 0.25"x0.25" square clearance centered at the center of the mounting hole.



Component Side

- One the solder side, each of the three mounting holes for the Vicksburg Motherboard has a rectangular clearance. The clearance of the mounting hole for the bracket is also outlined in the following diagram.



Solder Side
Unit: inch

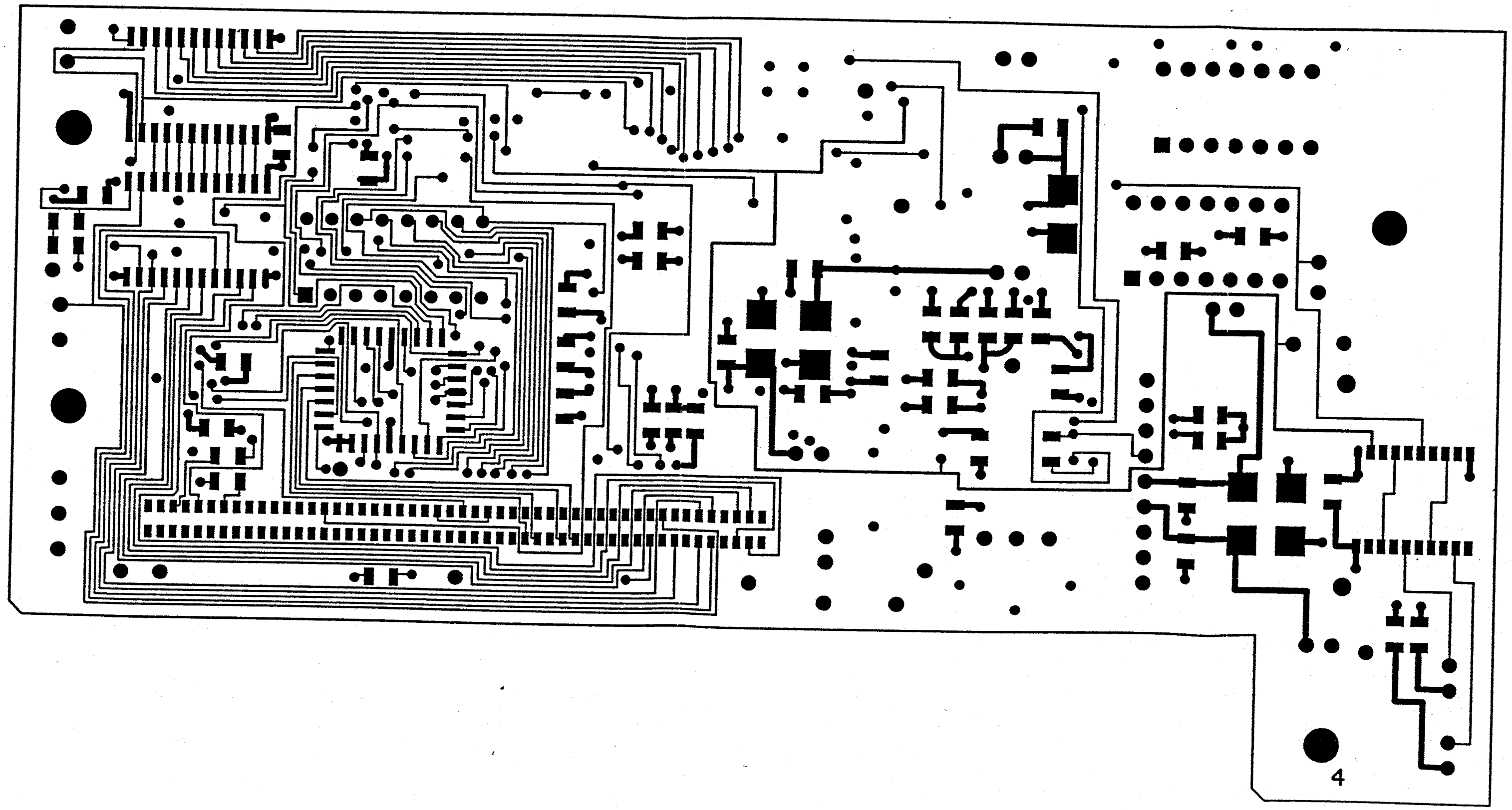
Misc

Following suggestions may be useful:

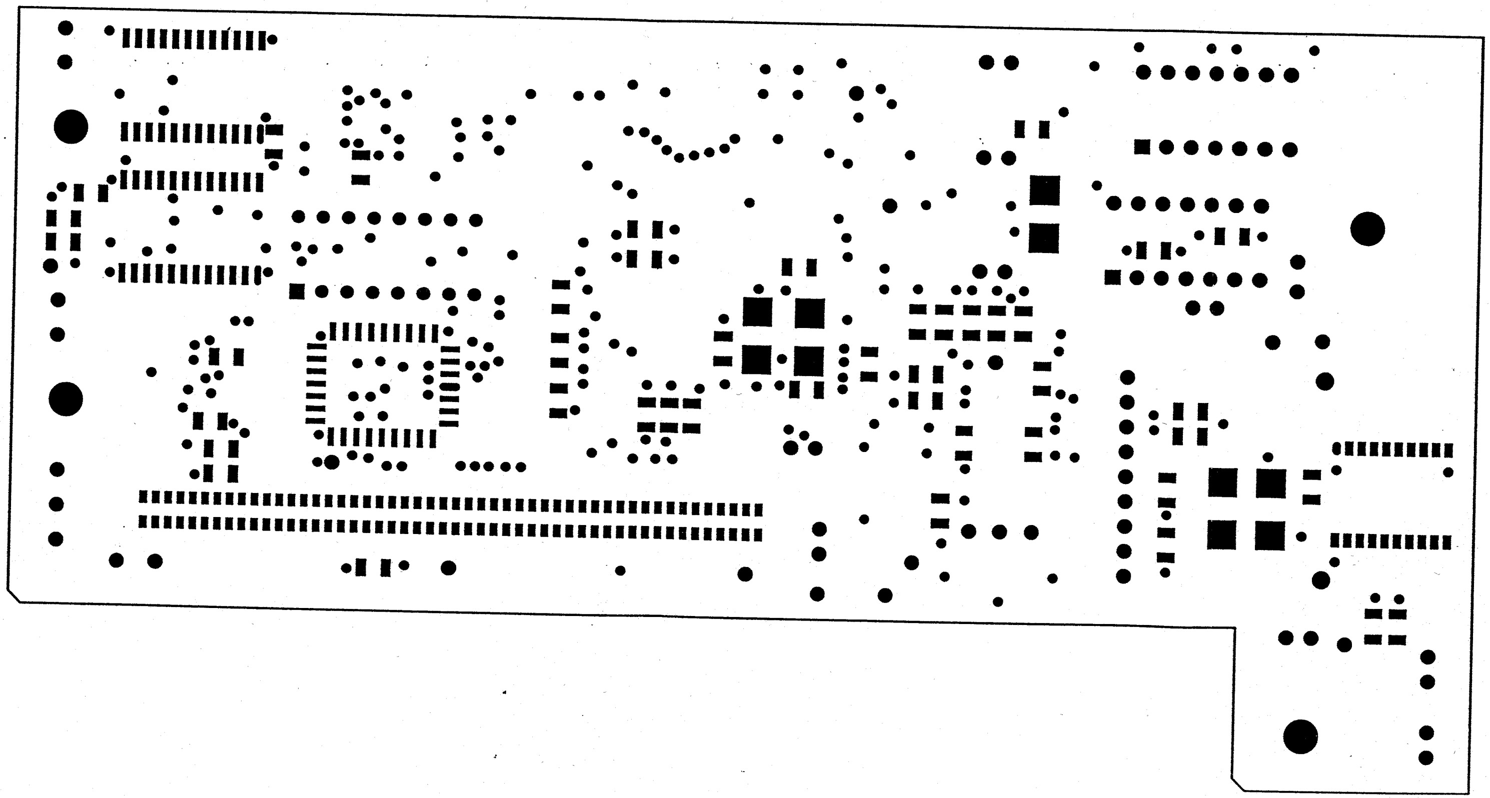
- Due to the high speed of the signals, ground leads of probe scopes should be kept as short as possible. To aid signal probing, all ground and power vias should be marked in some consistent fashion.
- All surfacemount capacitors are ceramic. RF rated capacitors are not essential.
- Label the positive terminals of polarized capacitors such as tantalum capacitors.

APPENDIX G: LAYOUT

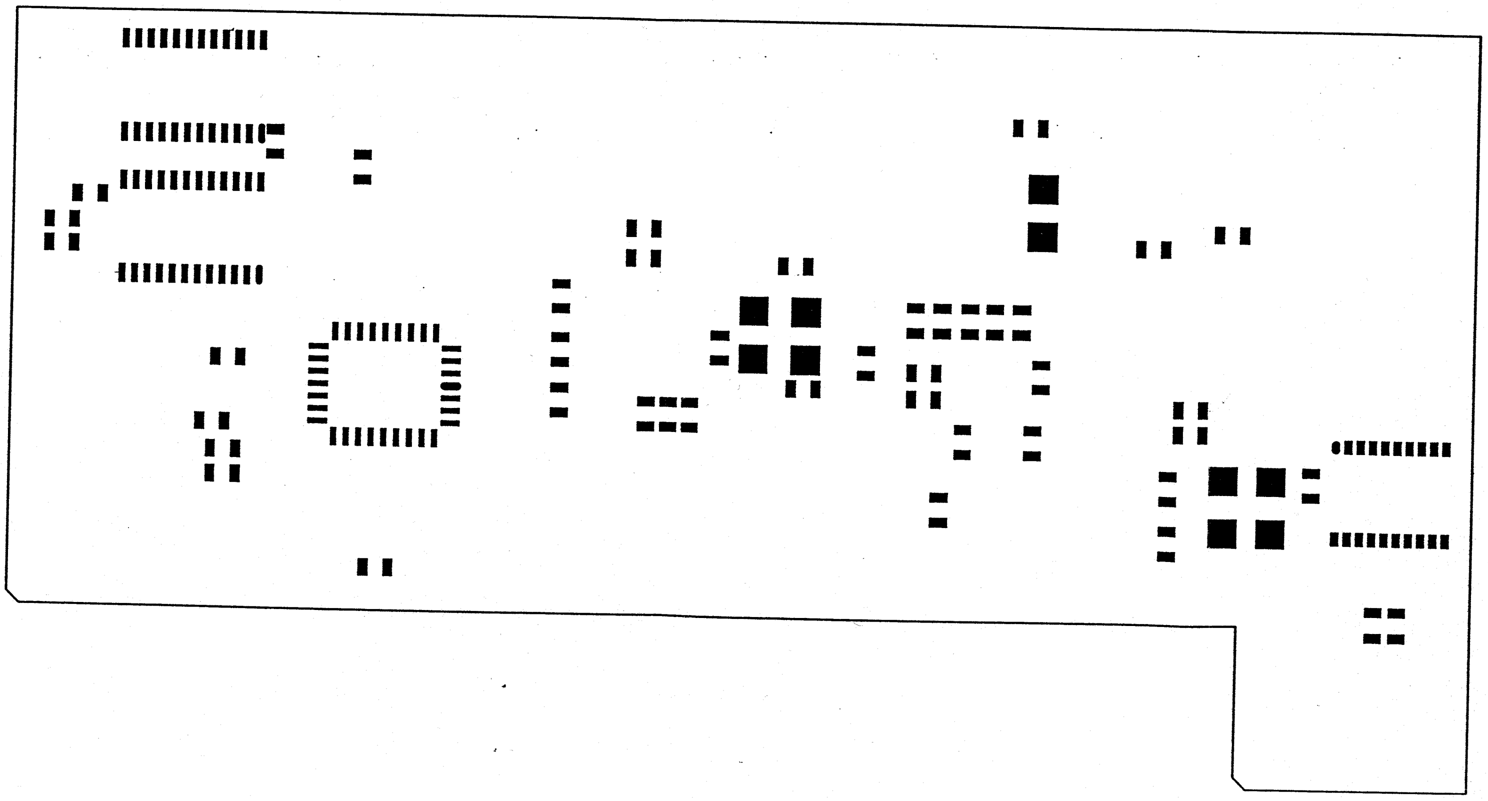
[illegible]



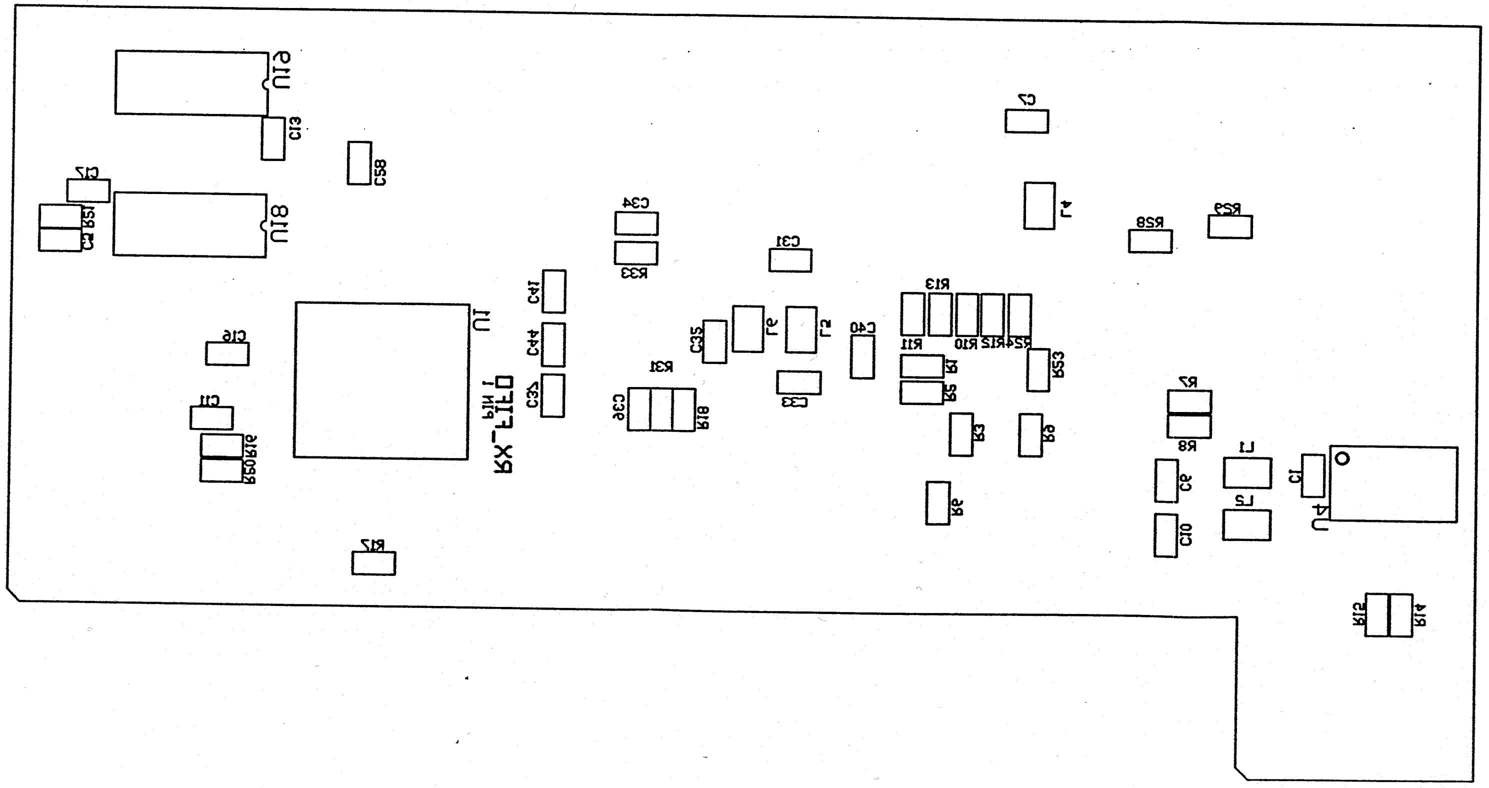
SAPI_1-1 Bottom Layer



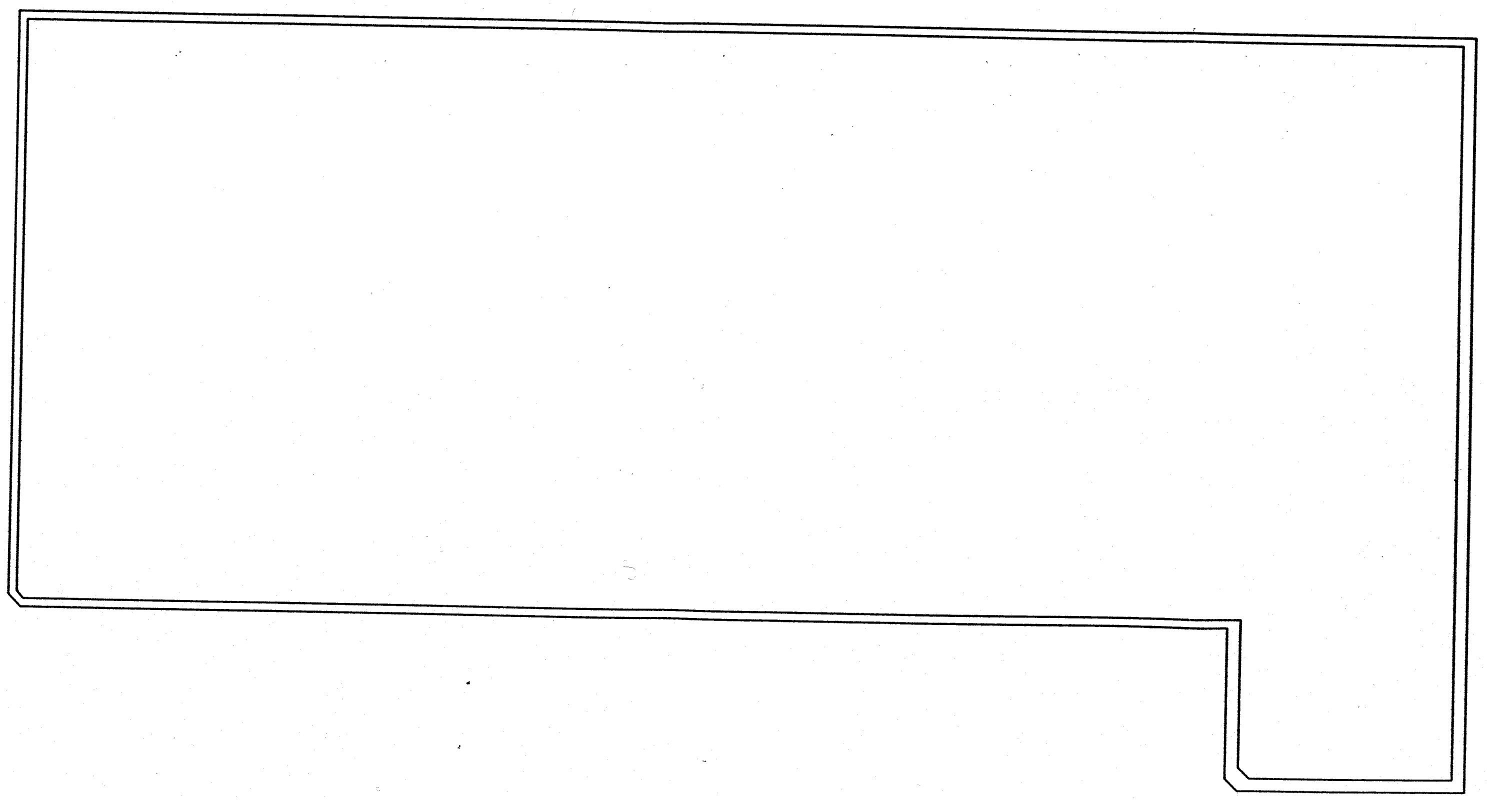
SAPI_1-1 Bottom Solder Mask



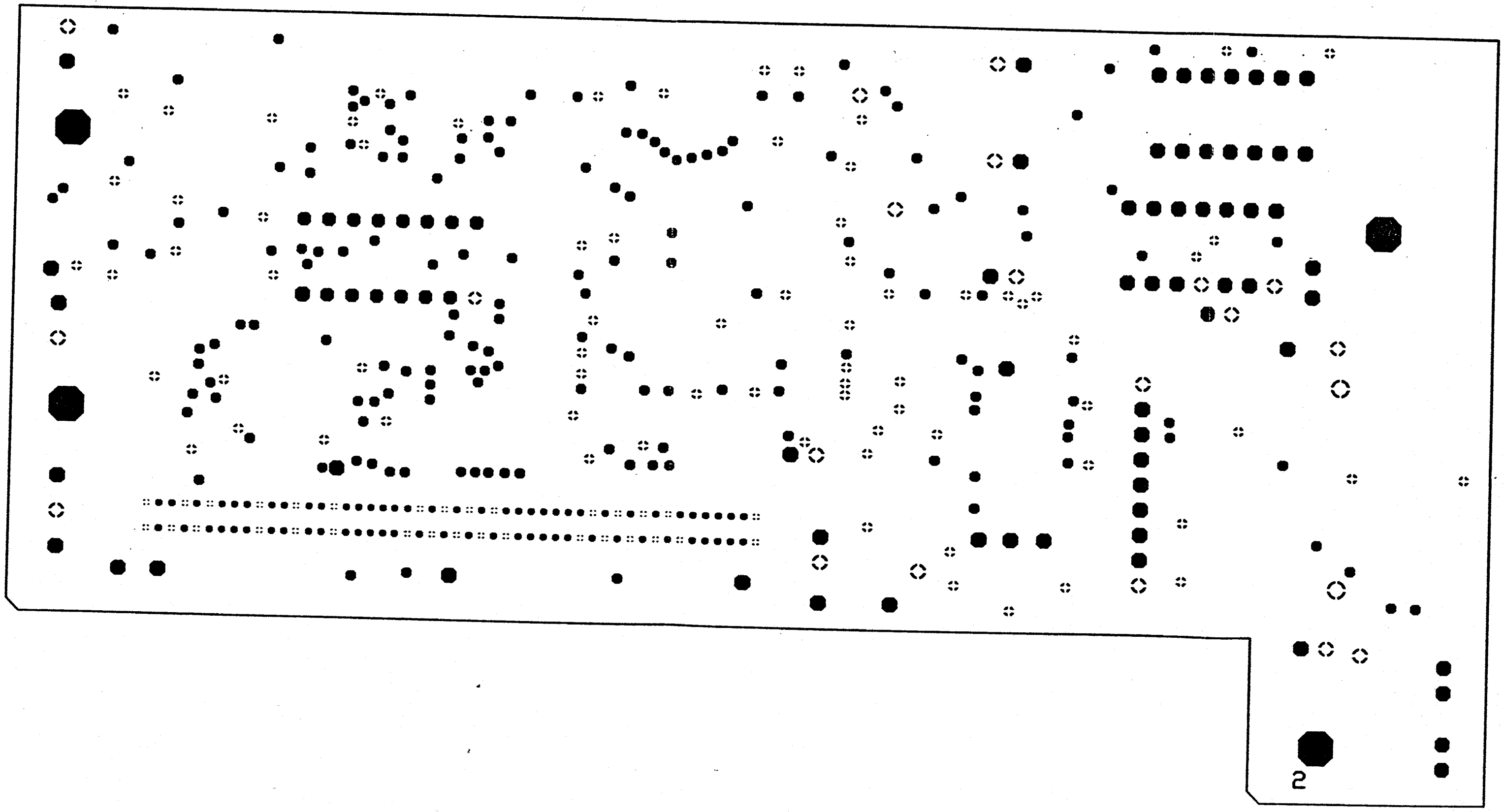
SAPI_1-1 Bottom Paste Mask



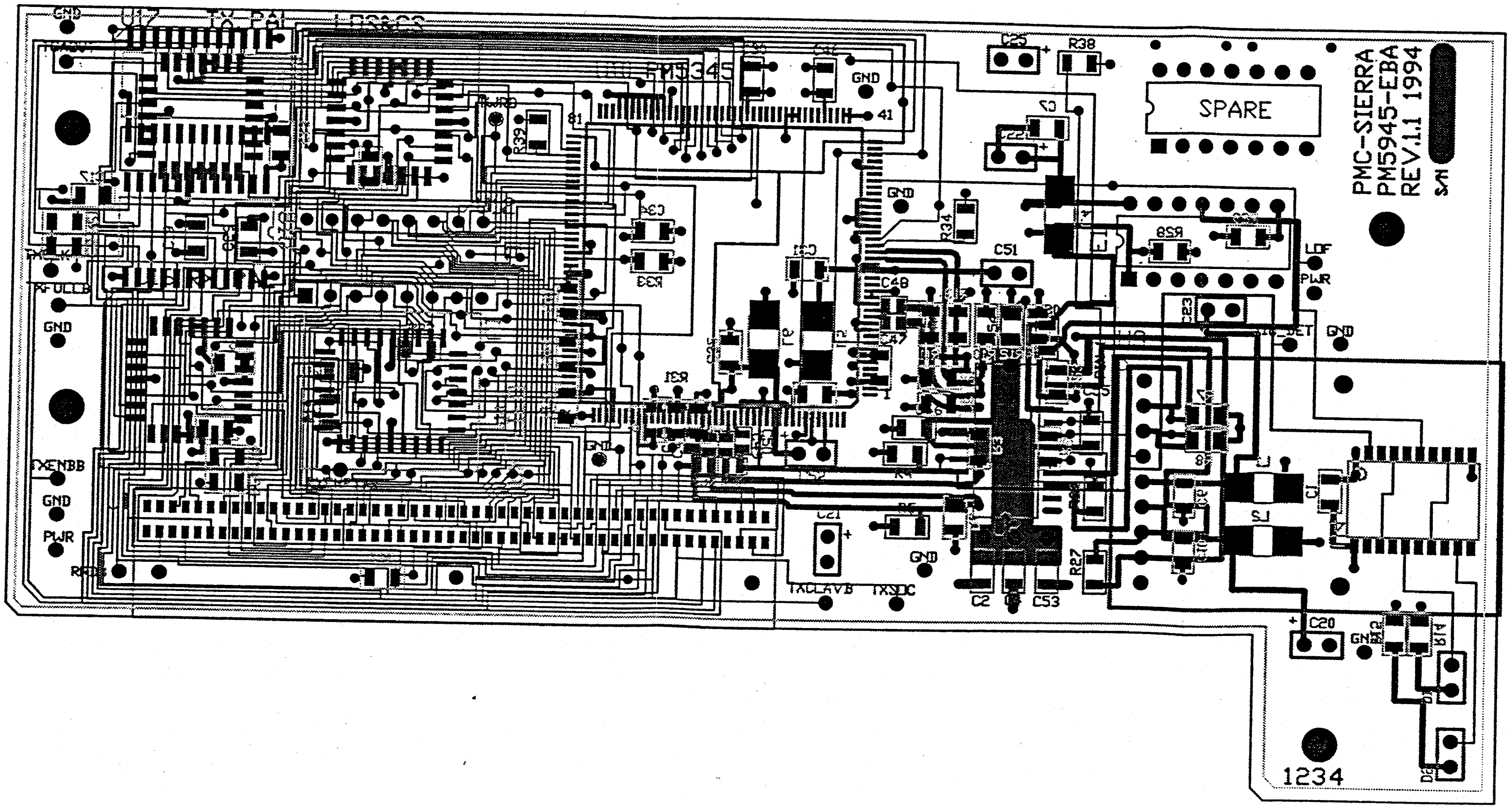
SAPI_1-1 Bottom Overlay



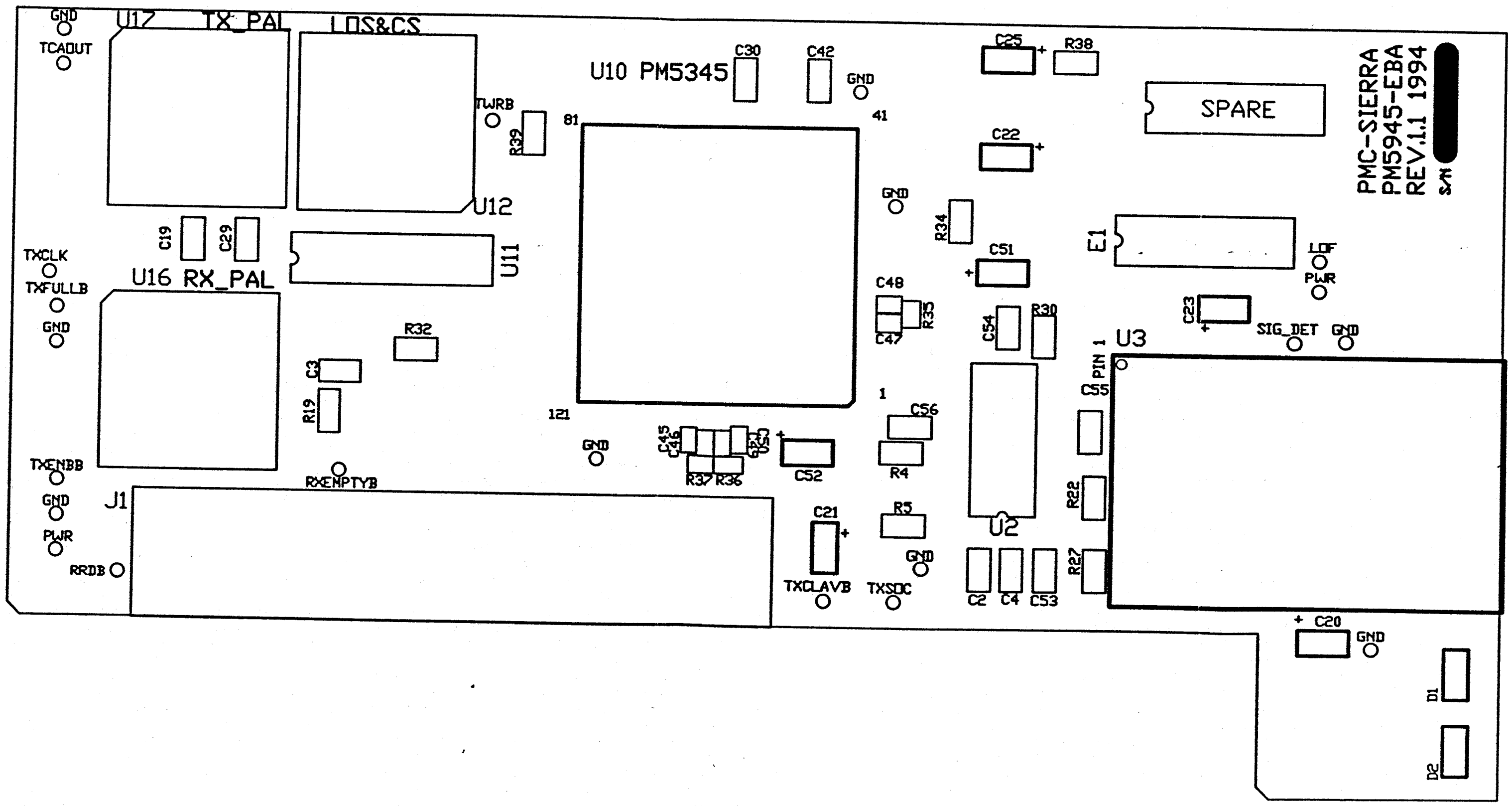
SAPI_1-1 Keep Out Layer



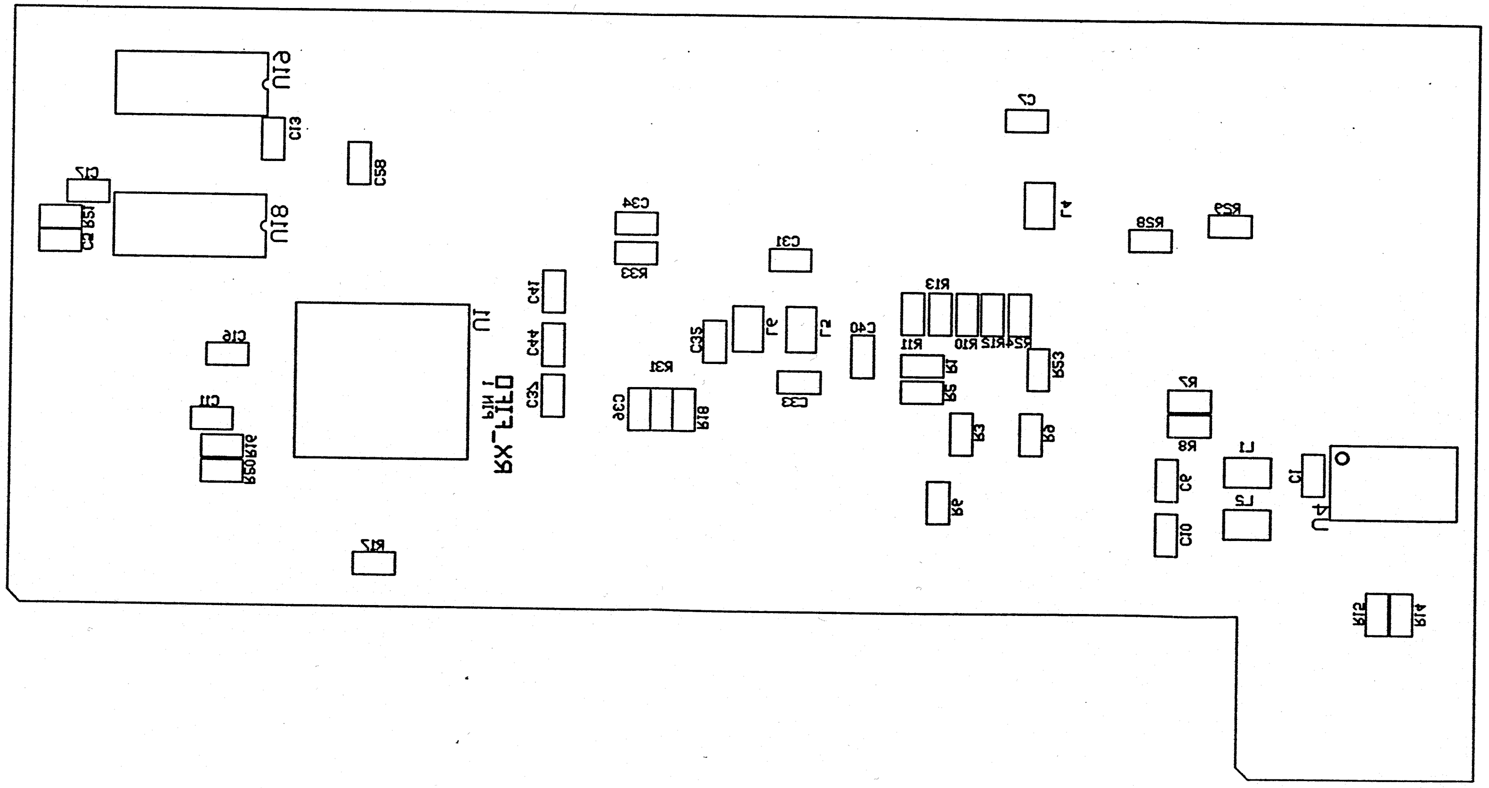
SAPI_1-1 Ground Plane



SAPI_1-1 Check Plot



SAPI_1-1 Top Overlay



SAPI_1-1 Bottom Overlay