JUN 6 1991

LSI/CSI
Manufacturers of Custom and Standard LSI Circuits
1235 Walt Whitman Road, Melville, NY 11747-3086 • Tel.: (516) 271-0400 • Fax: (516) 271-0405 • TWX: (510) 226-7833

LS7260/LS7261 LS7262

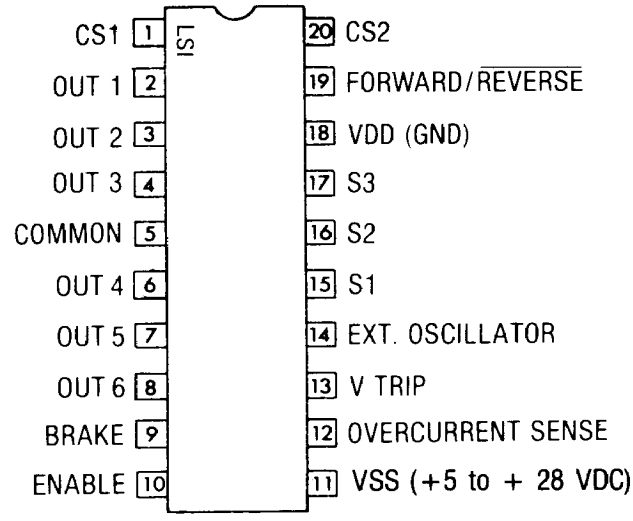
Revised October, 1990

BRUSHLESS DC MOTOR COMMUTATOR/CONTROLLER

FEATURES:

- Direct drive of P channel and N channel FETs (LS7260)
- Direct drive of PNP and NPN transistors (LS7261/LS7262)
- Open or closed loop motor speed control
- 5 to 28 volt operation
- Externally selectable input to output code for 60°, 120°, 240°, or 300° electrical sensor spacing
- Three or four phase operation
- Analog speed control input
- Forward/Reverse control
- Output enable control
- Positive static braking
- Overcurrent sensing
- Six outputs drive switching bridge directly

CONNECTION DIAGRAM — TOP VIEW
STANDARD 20 PIN PLASTIC DIP



DESCRIPTION:

The LS7260/LS7261/LS7262 are monolithic, ion implanted MOS circuits designed to generate the signals necessary to control a three phase or four phase brushless D.C. motor. They are the basic building blocks of a brushless D.C. motor controller. The circuits respond to changes at the sense inputs, originating at the motor position sensors, to provide electronic commutation of the motor windings. Duty cycle modulation of outputs for motor speed control is accomplished through either the Enable Input or through the Analog Input (VTRIP) in conjunction with the oscillator input. Overcurrent circuitry is provided to protect the windings, associated drivers and power supply. The LS7261 overcurrent circuitry causes the external output drivers to switch on and off directly from the overcurrent sense input. The LS7260 and LS7262 circuitry causes the external output drivers to switch off immediately upon sensing the overcurrent condition, and on again only when the overcurrent condition disappears and the positive edge of either the enable input or the sawtooth oscillator occurs. This limits the overcurrent sense cycling to the chopping rate of the enable input or the sawtooth oscillator. A positive braking feature is provided to effect rapid deceleration. While the LS7261/LS7262 are designed for driving NPN and PNP transistors (see Figure 2), the LS7260 is designed to drive both NMOS and PMOS Power FETs and develops a full 12 volts drive for both the N Channel and P Channel devices (see Figure 1) when using a 12 volt power supply.

INPUT/OUTPUT DESCRIPTION:

COMMUTATION SELECTS (Pins 1, 20)

These inputs are used to select the proper sequence of outputs based on the electrical separation of the motor position sensors. With both inputs low (logic zero), the sequence is adjusted for 60° electrical separation, with CS2 high and CS1 low 120° separation sequence is selected, with CS1 high and CS2 low 240° separation sequence is selected and with CS1 and CS2 high the 300° separation sequence is selected. Note that in all cases the external output drivers are disabled for invalid sense input codes. Internal pull down resistors are provided at pins 1 and 20 causing a logic zero when these pins are left open.

FORWARD/$\overline{\text{REVERSE}}$ (Pin 19)

This pin acts to modify the input to output sequence such that when brought from high to low or low to high the direction of rotation will reverse. An internal pull up resistor is provided at pin 19 causing a logic one when left open.

SENSE INPUTS (Pins 15, 16, 17)

These inputs provide control of the output commutation sequence as shown in Table III. S1, S2, S3 originate in the position sensors of the motor and must sequence in cycle code order. Hall switch "pull-up" resistors are provided at pins 15, 16 and 17. The positive supply of the Hall devices should be common to the chip Vss.

BRAKE (Pin 9)

For the LS7261 and LS7262, a high level applied to this input unconditionally turns off outputs 1, 2 and 3 and turns on outputs 4, 5 and 6. (See Figure 2). For the LS7260, the high level at this input turns ON outputs 1, 2, and 3 and outputs 4, 5 and 6. (See Figure 1). In both cases, transistors Q_{101},

Q_{102} and Q_{103} cut off and transistors Q_{104}, Q_{105} and Q_{106} turn on, shorting the windings together. The brake has priority over all other inputs. An internal pull down resistor is provided at pin 9 causing no braking when left open. (Center tapped motor configuration requires a power supply disconnect transistor controlled brake signal — See Figure 2A)

ENABLE (Pin 10)
A high level on this input permits the output to sequence as in Table III, while a low disables all external output drivers. An internal "pull up" resistor is provided at pin 10, enabling when left open. Positive edges at this input will reset the overcurrent flip flop of the LS7260 and LS7262.

OVERCURRENT SENSE (PIN 12)
This input provides the user a way of protecting the motor winding, drivers and power supply from an overload condition. The user provides a fractional ohm resistor between the negative supply and the common emitters of the NPN drivers or common sources of N-Channel FET drivers. This point is connected to one end of a potentiometer (e.g. 100K ohms), the other end of which is connected to the positive supply. The wiper pickoff is adjusted so that all outputs are disabled for currents greater than the limit. The action of the input is to disable all external output drivers. When brake exists, the overcurrent will be overridden. The LS7260 and LS7262 overcurrent circuitry latches the overcurrent condition. The latch may be reset by the positive edge of either the sawtooth oscillator or the ENABLE input. When using the ENABLE input as a chopped input, the oscillator pin should be held at VSS. When the ENABLE input is held high, the oscillator must be used to reset the overcurrent latch.

V TRIP (Pin 13)
This pin is used in conjunction with the sawtooth oscillator provided on the circuit. When the voltage level applied to V TRIP is more negative than the level at the OSC pin, the outputs will be enabled in Table III. If V TRIP is more positive than the OSC then all external output drivers are disabled.

The sawtooth waveform at the oscillator pin typically varies from .4 VSS to VSS-2 volts (assuming VDD is at ground potential). The purpose of this input in conjunction with the oscillator is to provide variable speed adjustment for the motor by means of duty cycle modulation.

OSCILLATOR (Pin 14)
A resistor and capacitor connected to this pin (See Figures 6 and 7) provide the timing components for a sawtooth oscillator. The signal generated is used in conjunction with V TRIP to provide duty cycle modulation for variable speed applications and, in the LS7260 and LS7262, to reset the overcurrent condition.

OUTPUTS 1, 2, 3 (Pins 2, 3, 4)
For the LS7261/LS7262, these open drain outputs are enabled as shown in Table II and provide base current to PNP transistors or gate drive to P-Channel FET drivers when COMMON (Pin 5) is floating. If COMMON is held at VSS potential, then these outputs provide drive to NPN or N-Channel FET drivers. For the LS7260, these outputs provide drive to P-Channel FET drivers if COMMON is held at VSS potential.

OUTPUT 4, 5, 6 (Pins 6, 7, 8)
These open drain outputs are enabled as in Table II and provide base current to NPN transistors or gate drive to N-channel FET drivers.

COMMON (Pin 5)
For the LS7261/LS7262, the COMMON may be connected to VSS when using center tapped motor configuration or when using all NPN or N-Channel drivers. For the LS7260, the COMMON is tied to VSS.

VSS (Pin 11)
Supply voltage positive terminal (+5 to +28 VDC).

VDD (Pin 18)
Supply voltage negative terminal (ground)

MAXIMUM RATINGS:

PARAMETER	SYMBOL	VALUE	UNITS
Storage Temperature	Tstg	−65 to +150	°C
Operating Temperature			
1. Plastic	Tap	−25 to +70	°C
2. Ceramic	Tac	−55 to +125	°C
Voltage (any pin to Vss)	Vmax	−30 to +.5	VOLTS

DC ELECTRICAL CHARACTERISTICS:
(All Voltages Referenced to V_{DD})

	SYMBOL	MIN	TYP	MAX	UNITS
SUPPLY VOLTAGE	VSS	5	—	28	Volts
SUPPLY CURRENT (Excluding Outputs)	I_{DD}	—	4.5	6	mA
INPUT SPECIFICATIONS: BRAKE, ENABLE, CS1, CS2, S1, S2, S3, FORWARD/REVERSE	R_{IN}	—	150	—	KΩ
VOLTAGE (Logic "1")	V_{IH}	VSS-1.5	—	VSS	Volts
(Logic "0")	V_{IL}	0		VSS-4.0	Volts
*OVERCURRENT SENSE VOLTAGE (Logic "1")	VIH	(VSS÷2)+0.25	—	VSS	Volts
(Logic "0")	V_{IL}	0	—	(VSS÷2)-0.25	Volts

OSCILLATOR:					
FREQUENCY RANGE	FOSC	0	1/RC	100	kHZ
EXTERNAL RESISTOR RANGE	ROSC	22	—	1000	kΩ

*Theoretical switching point for the OVERCURRENT SENSE Input is one half of the power supply determined by an internal bias network in manufacturing. Tolerances cause the switching point to vary plus or minus .25 volts. After manufacture, the switching point remains fixed within 10mv over time and temperature. The input switching sensitivity is a maximum of 50mV. There is no hysteresis on the OVERCURRENT SENSE input.

TYPICAL CIRCUIT OPERATION:

The oscillator is used for motor speed control as explained under VTRIP. Both upper and lower motor drive transistors are pulse width modulated (see Fig. 1 or Fig. 2) during speed control.

For the LS7261 or LS7262, the outputs turn on in pairs (see Table III). For example (see dotted line, fig. 2): Q8 and Q4 are on, thus enabling a path from the positive supply through the emitter-base junction of Q101, Q8, Q4, R5, the base emitter junction of Q105 and the fractional ohm resistor to ground. The current in the above described path is determined by the power supply voltage, the value of R1, the voltage drops across the base-emitter junctions of Q101 and Q105 (1.4 volts for single transistor or 2.8V for Darlington pairs), the impedance of Q8 and Q4 and the value of R5. Table I provides the recommended value for R5. R4 and R6 are the same value.

For the LS7260, (See Fig. 1) the external drivers also turn on in pairs. Internal operation is somewhat different than the LS7261 or LS7262. For example, external transistors Q101 and Q105 will turn on when internal transistor Q8 turns off and Q4 turns on enabling full power supply drive on Q101 and Q105. Since Pin 5 is tied to VSS, the gate of P-channel Driver Q101 is brought to ground potential by R1 and the Gate of N-Channel driver Q105 is brought to VSS potential by Q4. Other external output pairs turn on similarly and the commutation sequence is identical to that of the LS7261/LS7262 (Table III). Table II indicates the minimum value of R1 (=R2=R3=R4=R5=R6) needed as a function of output drive voltage for Figure I.

TABLE I

OUTPUT CURRENT LIMITING RESISTOR SELECTION TABLE

POWER SUPPLY (VOLTS)	OUTPUT CURRENT 20	15	10	7.5	5	2.5	mA
6	**	**	**	**	**	1.5	
9	**	**	**	.68	1.3	2.7	
12	.1	.25	.56	.86	1.5	3.3	
15	.33	.51	.92	1.3	2.1	4.6	Resistance
18	*	.76	1.3	1.7	2.8	5.8	(KΩ)
21	*	*	1.6	2.2	3.3	7.0	
24	*	*	1.9	2.6	4.0	8.3	
28	*	*	*	3.2	4.9	9.9	

*causes excessive power dissipation

**exceeds max current possible for this voltage

TABLE II

For Power Supply 5-28 Volts

R1 (K ohms)	Output Voltage
10	VSS -0.5
5.1	VSS -1.0
2.7	VSS -2.0

TABLE III

OUTPUT COMMUTATION SEQUENCE

THREE PHASE OPERATION

SEQUENCE SELECT	CS1 CS2 0 0	CS1 CS2 0 1	CS1 CS2 1 0	CS1 CS2 1 1	FORWARD/$\overline{\text{REVERSE}}$=1 OUTPUTS* ENABLED	DRIVERS* A	B	C	FORWARD/$\overline{\text{REVERSE}}$=0 OUTPUTS* ENABLED	DRIVERS* A	B	C
ELECTRICAL SEPARATION	(−60°−)	(−120°−)	(−240°−)	(−300°−)								
SENSE INPUTS	S1 S2 S3	S1 S2 S3	S1 S2 S3	S1 S2 S3								
	0 0 0	0 0 1	0 1 0	0 1 1	$0_1, 0_5$	+	−	Off	$0_2, 0_4$	−	+	Off
	1 0 0	1 0 1	1 1 0	1 1 1	$0_3, 0_5$	Off	−	+	$0_2, 0_6$	Off	+	−
	1 1 0	1 0 0	1 0 0	1 1 0	$0_3, 0_4$	−	Off	+	$0_1, 0_6$	+	Off	−
	1 1 1	1 1 0	1 0 1	1 0 0	$0_2, 0_4$	−	+	Off	$0_1, 0_5$	+	−	Off
	0 1 1	0 1 0	0 0 1	0 0 0	$0_2, 0_6$	Off	+	−	$0_3, 0_5$	Off	−	+
	0 0 1	0 1 1	0 1 1	0 0 1	$0_1, 0_6$	+	Off	−	$0_3, 0_4$	−	Off	+
	0 1 0	0 0 0	0 0 0	0 1 0	ALL DISABLED				ALL DISABLED			
	1 0 1	1 1 1	1 1 1	1 0 1	ALL DISABLED				ALL DISABLED			

*See fig. 1 and 2

*For the LS7260, Outputs 0_1, 0_2 and 0_3 are the logical inversions of the corresponding outputs of the LS7261 and LS7262.

The Overcurrent Input (Brake Low) enables external output drivers in normal sequence when more negative than VSS/2 and disables all external output drivers when more positive than VSS/2. On the LS7260 and LS7262 the overcurrent is sensed continuously, and sets a flip flop which is reset by the rising edge of the enable input or the sawtooth oscillator. (See description under Overcurrent Sense).

The VTRIP Input (Brake Low) enables the outputs in normal sequence when more negative than the oscillator input and disables all outputs when more positive than the oscillator input. The VTRIP input may be disabled by connecting it to VDD and the oscillator input to VSS. (See description under VTRIP)

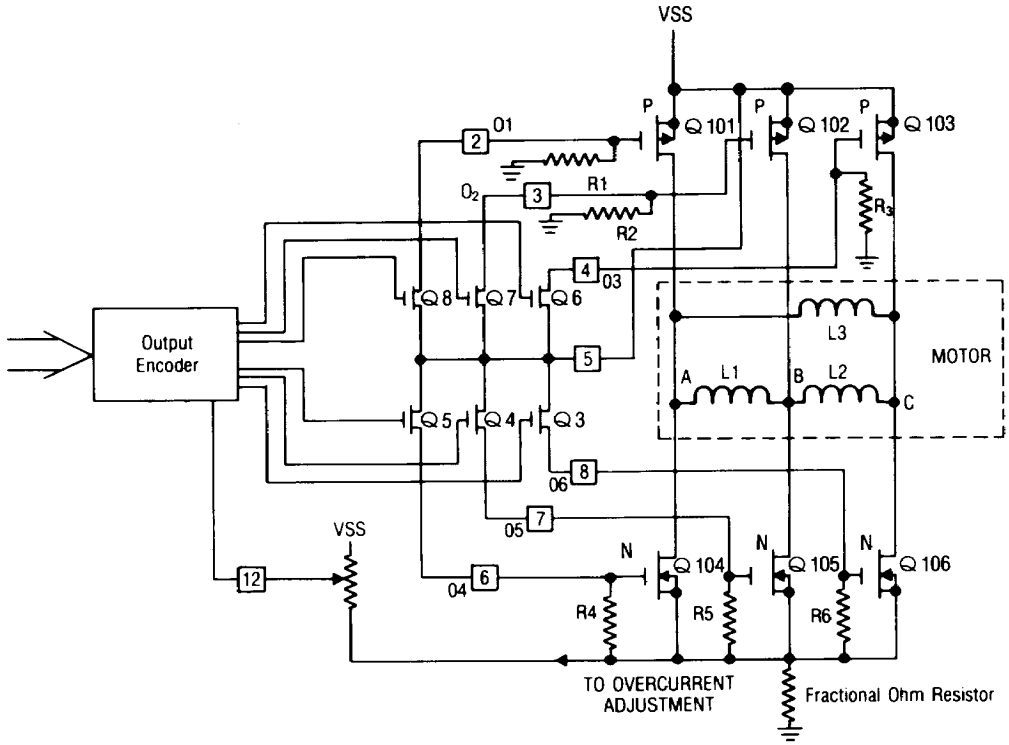


FIGURE 1
LS7260 THREE PHASE OUTPUT DRIVER CIRCUITRY

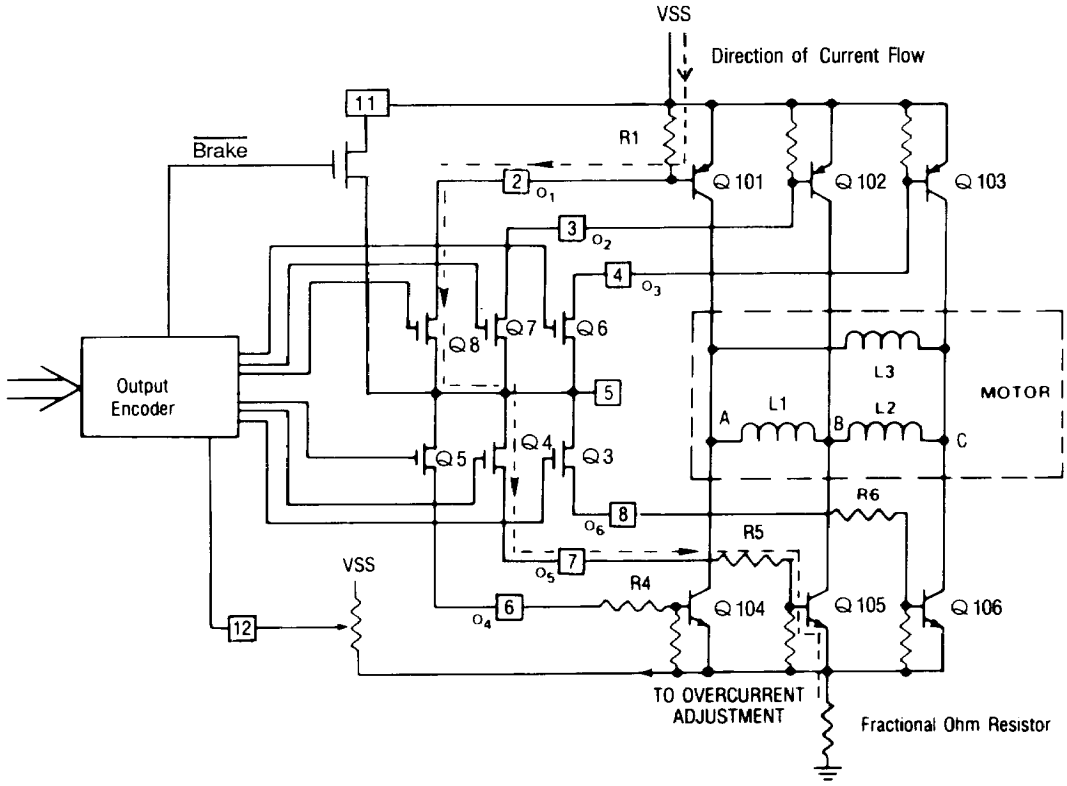


FIGURE 2
LS7261/LS7262 THREE PHASE OUTPUT DRIVER CIRCUITRY

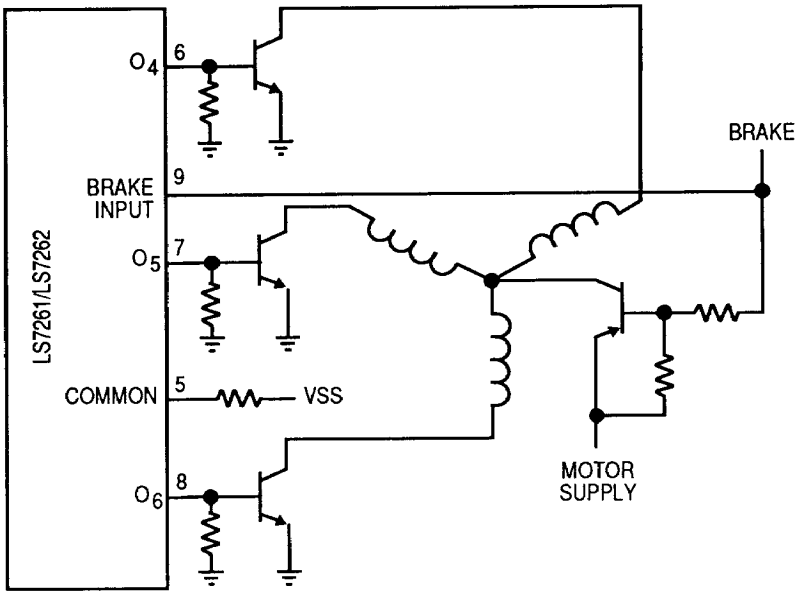


FIGURE 2A
SINGLE ENDED DRIVER CIRCUIT

This configuration requires only one base current limiting resistor connected from the COMMON pin to VSS.

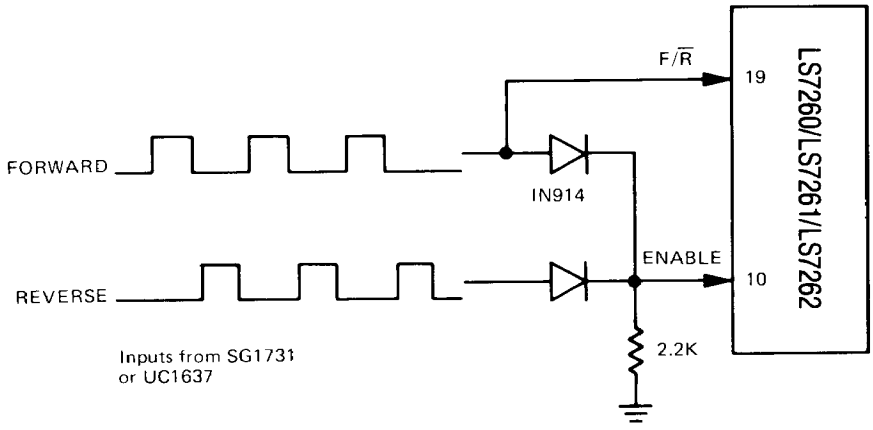


FIGURE 3 — PRECISION CONTROL BRUSHLESS DC MOTOR DRIVE

For controlled acceleration and deceleration of motors in the forward or reverse directions, a motor control pulse width modulator circuit such as the SG1731 or UC1637 can be interfaced with the LS7260/61/62.
The logical OR gate made up of the resistor-diode network permits the LS7260/61/62 to be enabled when either the forward or reverse input is high. By applying the forward input directly to Pin 19, the motor can only operate in the forward direction when the forward input is high and only in the reverse direction when the reverse input is high. Motor direction is determined by relative pulse widths of the forward and reverse inputs while acceleration or deceleration is determined by variations of these widths.

TABLE IV
OUTPUT COMMUTATION SEQUENCE
FOUR PHASE OPERATION
CS1=CS2=0
OUTPUTS ENABLED

S1	S2,S3	FORWARD/$\overline{\text{REVERSE}}$ = 1	FORWARD/$\overline{\text{REVERSE}}$ = 0
0	0	O_1	O_4
1	0	O_3	O_6
1	1	O_4	O_1
0	1	O_6	O_3

For four phase commutation (see fig. 4), the commutation select inputs must both be tied low. The S1 input is driven from one motor position sensor while the S2 and S3 inputs are connected together and driven by the second position sensor. The COMMON input must be connected to VSS. The sensors have an electrical separation of 90°. Figure 4A indicates the use of Bipolar Transistors. Figure 4B indicates the use of FET transistors. In both cases, the LS7261/LS7262 is used.

FIGURE 4 — FOUR PHASE OUTPUT DRIVER CIRCUITRY

FIGURE 4A

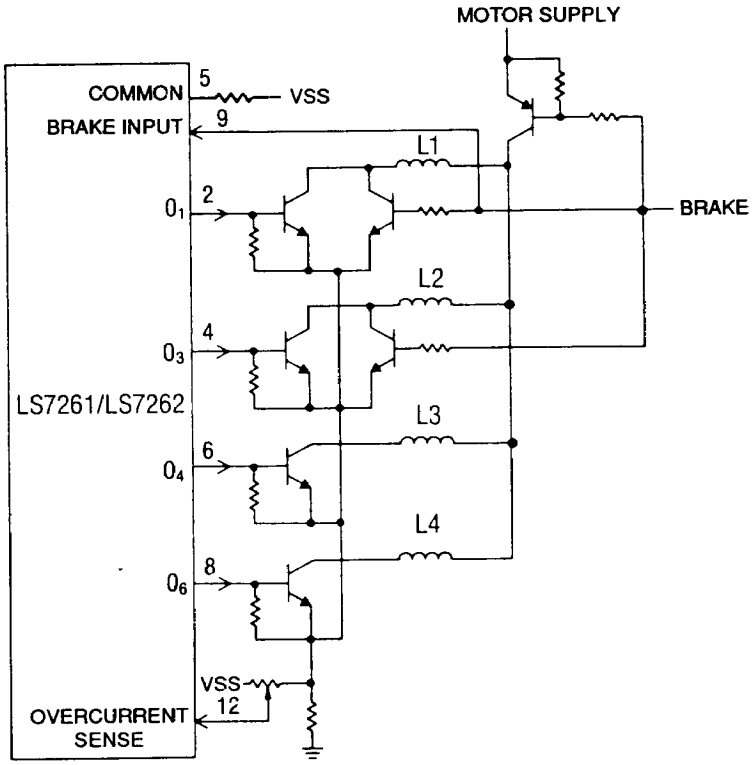
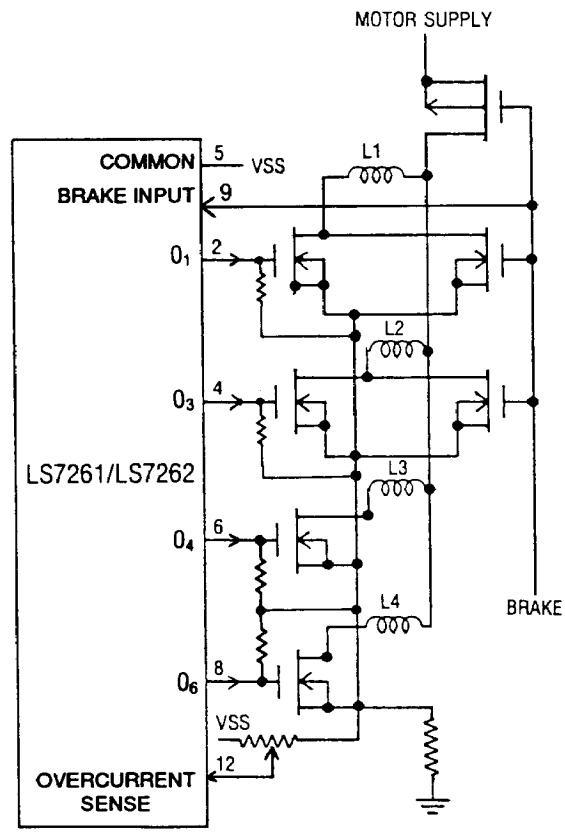


FIGURE 4B



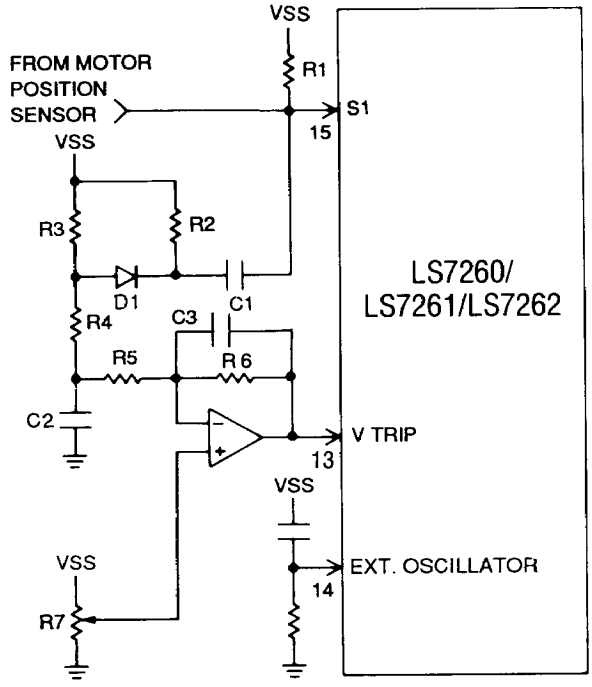


FIGURE 5
CLOSED-LOOP SPEED CONTROLLER

A closed loop system can be configured by differentiating one of the motor position sense inputs and integrating only the negative pulses to form a D.C. voltage that is applied to the inverting input of an op-amp. The non-inverting input voltage is adjusted with a potentiometer until the resultant voltage at VTRIP causes the motor to run at desired speed. The R_2-C_1 differentiator, the R_3-D_1 negative pulse transmitter and the R_4-C_2 integrator form a frequency to voltage converter. An increase in motor speed above the desired speed causes VTRIP to increase which lowers the duty cycle modulaton of the oscillator and the resultant motor speed. A decrease in speed lowers VTRIP and raises the duty cycle modulation and the resultant motor speed. For proper operation, both R_5 and R_6 should be greater than R_4, and R_4 in turn should be greater than both R_2 and R_3. Also the R_4-C_2 should be greater than the R_2-C_1 time constant. C_3 may be added across R_6 for additional VTRIP smoothing.

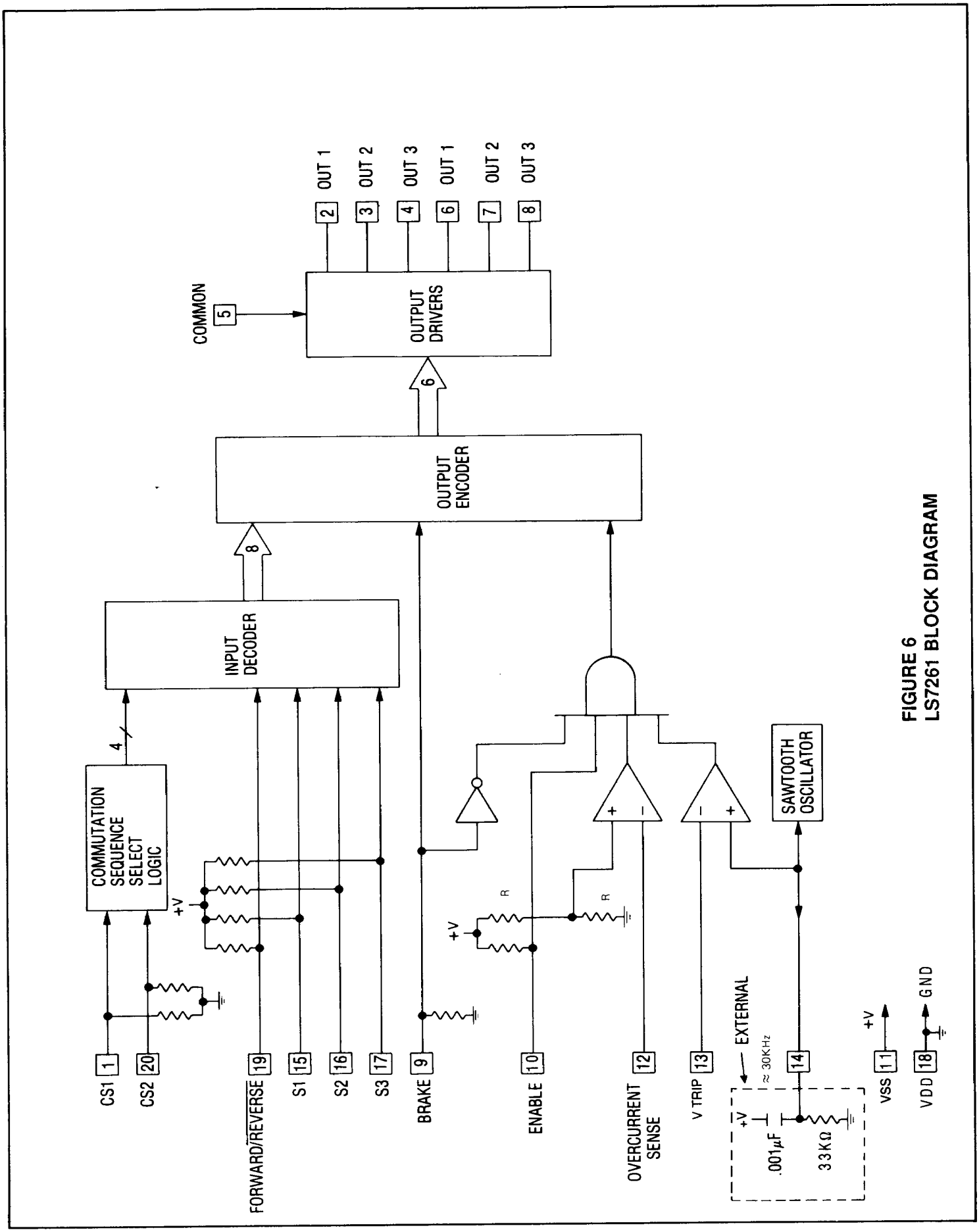


FIGURE 6
LS7261 BLOCK DIAGRAM

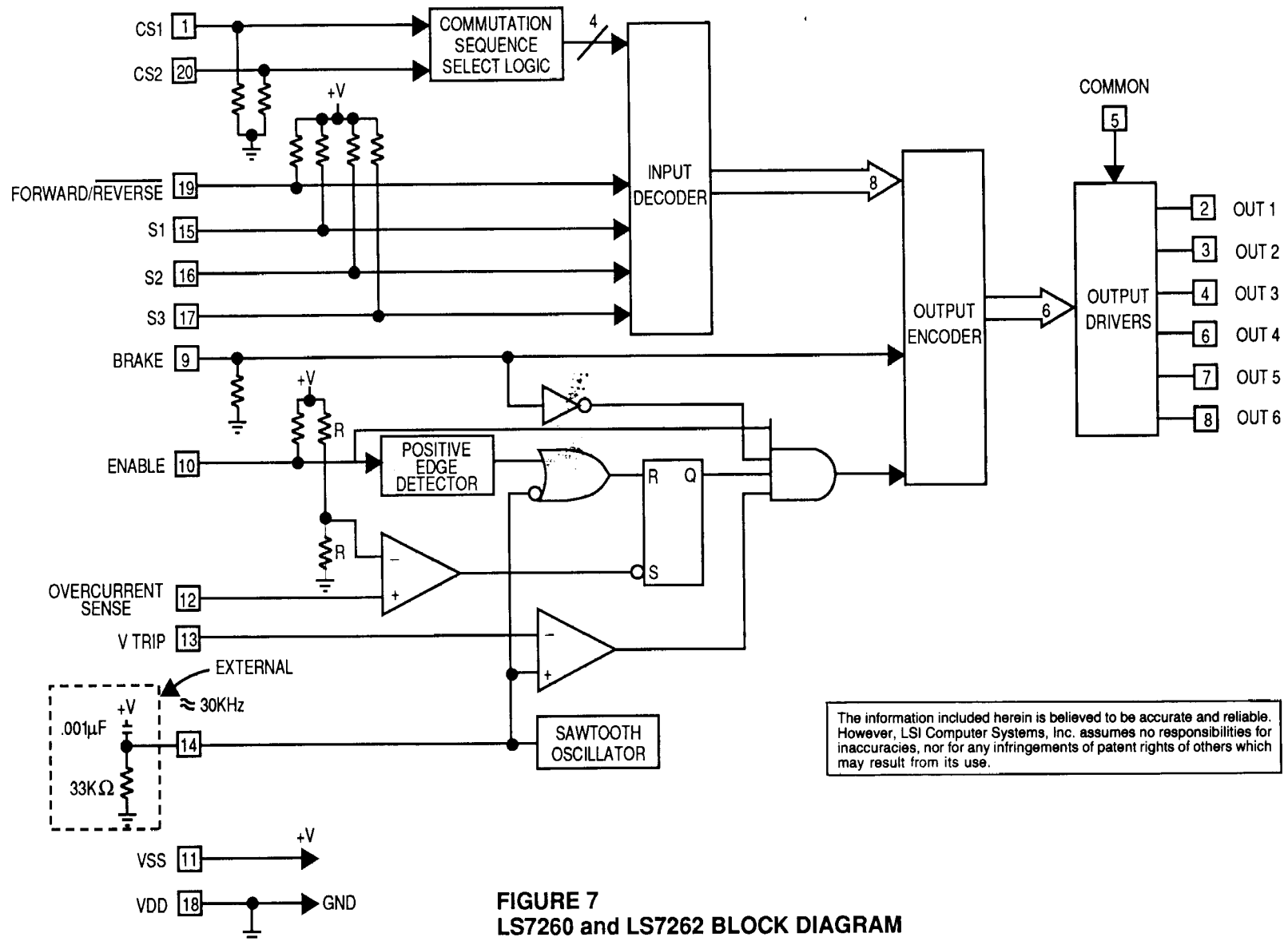


FIGURE 7
LS7260 and LS7262 BLOCK DIAGRAM