Am27C800

8 Megabit (1,048,576 x 8-Bit/524,288 x 16-Bit) ROM Compatible CMOS EPROM

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- **Fast access time**
  - 120 ns
- **Low power consumption**
  - 100 µA maximum CMOS standby current
- **Industry standard pinout:**
  - ROM compatible
  - 42-pin DIP, PDIP and 44-pin LCC and PLCC packages provide easy upgrade to 16 Mbits

- **Single +5 V power supply**
- **±10% power supply tolerance standard on most speeds**
- **100% Flashrite™ programming**
  - Typical programming time of less than 1 minute
- **Latch-up protected to 100 mA from –1 V to Vcc + 1 V**
- **High noise immunity**

GENERAL DESCRIPTION

The Am27C800 is an 8 Mbit ultraviolet erasable programmable read-only memory that is functionally and pinout compatible with 8 Mbit masked ROMs. Under control of the $\overline{BYTE}$ input, the memory can be configured as either a 1 Mbit by 8-bit memory or a 512K by 16-bit memory. It operates from a single +5 V supply, has a static standby mode, and features fast single address location programming. Products are available in windowed ceramic packages as well as plastic one time programmable (OTP) packages.

Typically, any byte can be accessed in less than 120 ns, allowing operation with high-performance microprocessors without any WAIT states. The Am27C800 offers

separate Output Enable ($\overline{OE}$) and Chip Enable ($\overline{CE}$) controls, thus eliminating bus contention in a multiple bus microprocessor system.

AMD's CMOS process technology provides high speed, low power, and high noise immunity. Typical power consumption is only 150 mW in active mode, and 100 µW in standby mode.

All signals are TTL levels, including programming signals. Bit locations may be programmed singly, in blocks, or at random. The Am27C800 supports AMD's Flashrite™ programming algorithm (100 µs pulses) resulting in typical programming times of less than 1 minute.
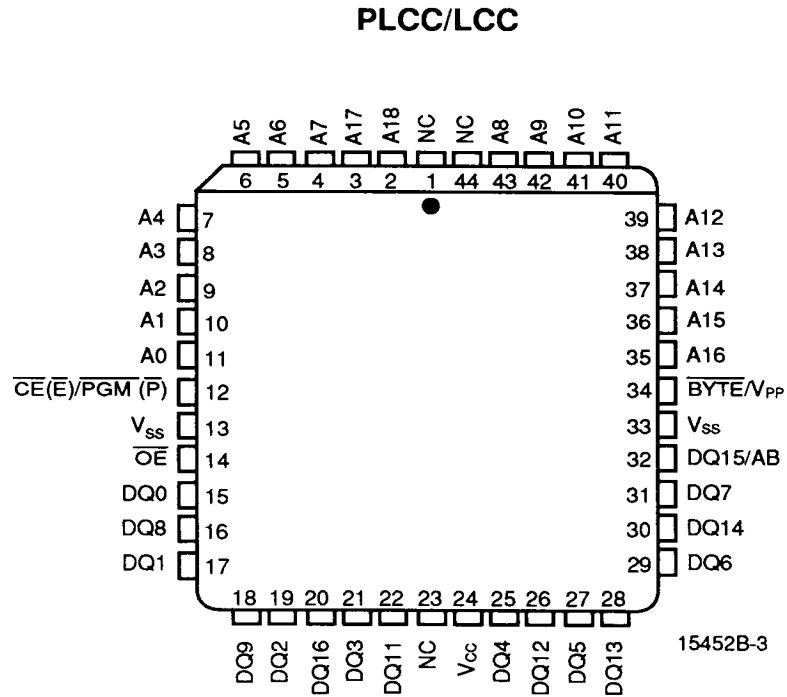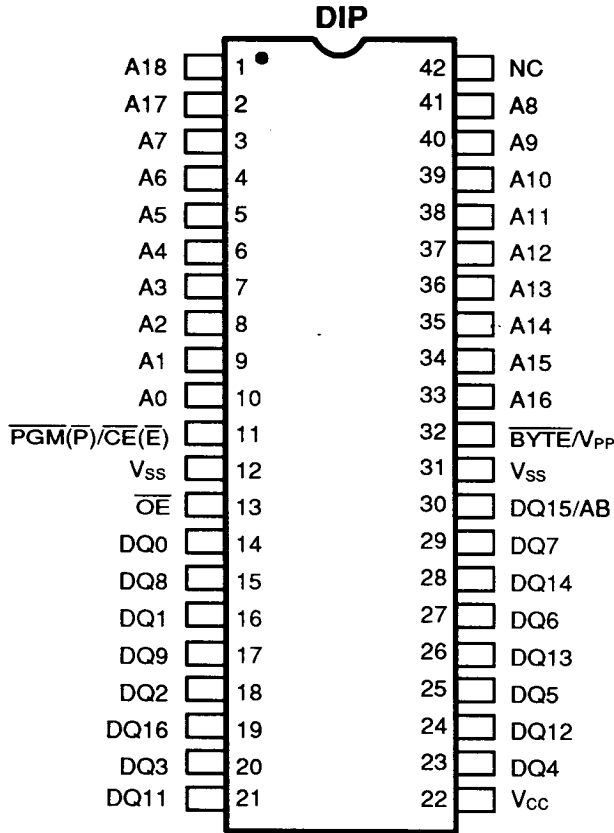

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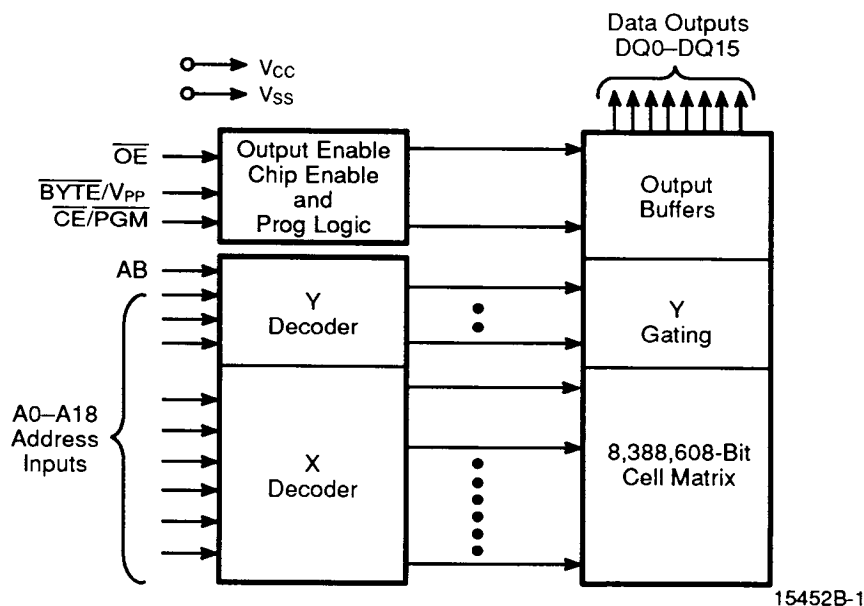
PRODUCT SELECTOR GUIDE

Family Part No.	Am27C800			
Ordering Part No: $V_{CC} \pm 5\%$	**-125**			**-255**
$V_{CC} \pm 10\%$	**-120**	**-150**	**-200**	**-250**
Max Access Time (ns)	120	150	200	250
$\overline{CE}$ (E) Access Time (ns)	120	150	200	250
$\overline{OE}$ (G) Access Time (ns)	50	65	75	100

CONNECTION DIAGRAM

Top View

DIP

A18	1	42	NC
A17	2	41	A8
A7	3	40	A9
A6	4	39	A10
A5	5	38	A11
A4	6	37	A12
A3	7	36	A13
A2	8	35	A14
A1	9	34	A15
A0	10	33	A16
$\overline{PGM}(P)/\overline{CE}(E)$	11	32	$\overline{BYTE}/V_{PP}$
V_{SS}	12	31	V_{SS}
$\overline{OE}$	13	30	DQ15/AB
DQ0	14	29	DQ7
DQ8	15	28	DQ14
DQ1	16	27	DQ6
DQ9	17	26	DQ13
DQ2	18	25	DQ5
DQ16	19	24	DQ12
DQ3	20	23	DQ4
DQ11	21	22	V_{CC}

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PLCC/LCC

Top pins (6 5 4 3 2 1 44 43 42 41 40): A5, A6, A7, A17, A18, NC, NC, A8, A9, A10, A11

Left side:
- A4 — 7
- A3 — 8
- A2 — 9
- A1 — 10
- A0 — 11
- $\overline{CE}(E)/\overline{PGM}(P)$ — 12
- V_{SS} — 13
- $\overline{OE}$ — 14
- DQ0 — 15
- DQ8 — 16
- DQ1 — 17

Right side:
- 39 — A12
- 38 — A13
- 37 — A14
- 36 — A15
- 35 — A16
- 34 — $\overline{BYTE}/V_{PP}$
- 33 — V_{SS}
- 32 — DQ15/AB
- 31 — DQ7
- 30 — DQ14
- 29 — DQ6

Bottom pins (18 19 20 21 22 23 24 25 26 27 28): DQ9, DQ2, DQ16, DQ3, DQ11, NC, V_{CC}, DQ4, DQ12, DQ5, DQ13

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Note:

1. JEDEC nomenclature is in parenthesis.

PIN DESIGNATIONS

AB	=	Address Input ($\overline{BYTE}$ Mode)
A0–A18	=	Address Inputs
$\overline{BYTE}/V_{PP}$	=	Byte/Word Switch or Program Supply Voltage
$\overline{CE}$ (E)/$\overline{PGM}$ (P)	=	Chip Enable
DQ0–DQ15	=	Data Inputs/Outputs
NC	=	No Internal Connection
$\overline{OE}$ (G)	=	Output Enable Input
V_{CC}	=	V_{CC} Supply Voltage
V_{SS}	=	Ground

LOGIC SYMBOL

- AB
- 18 / A0–A18
- DQ0–DQ15 → 16 / or 8
- $\overline{CE}$ (E)/$\overline{PGM}$ (P)
- $\overline{OE}$ (G)
- $\overline{BYTE}/V_{PP}$

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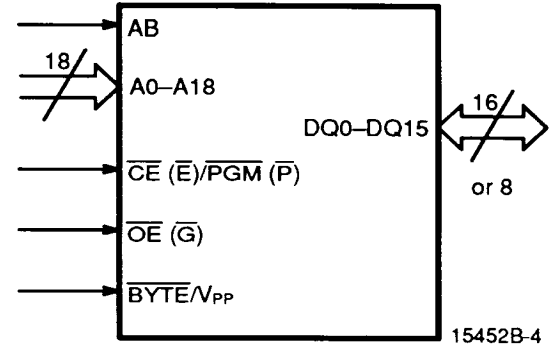
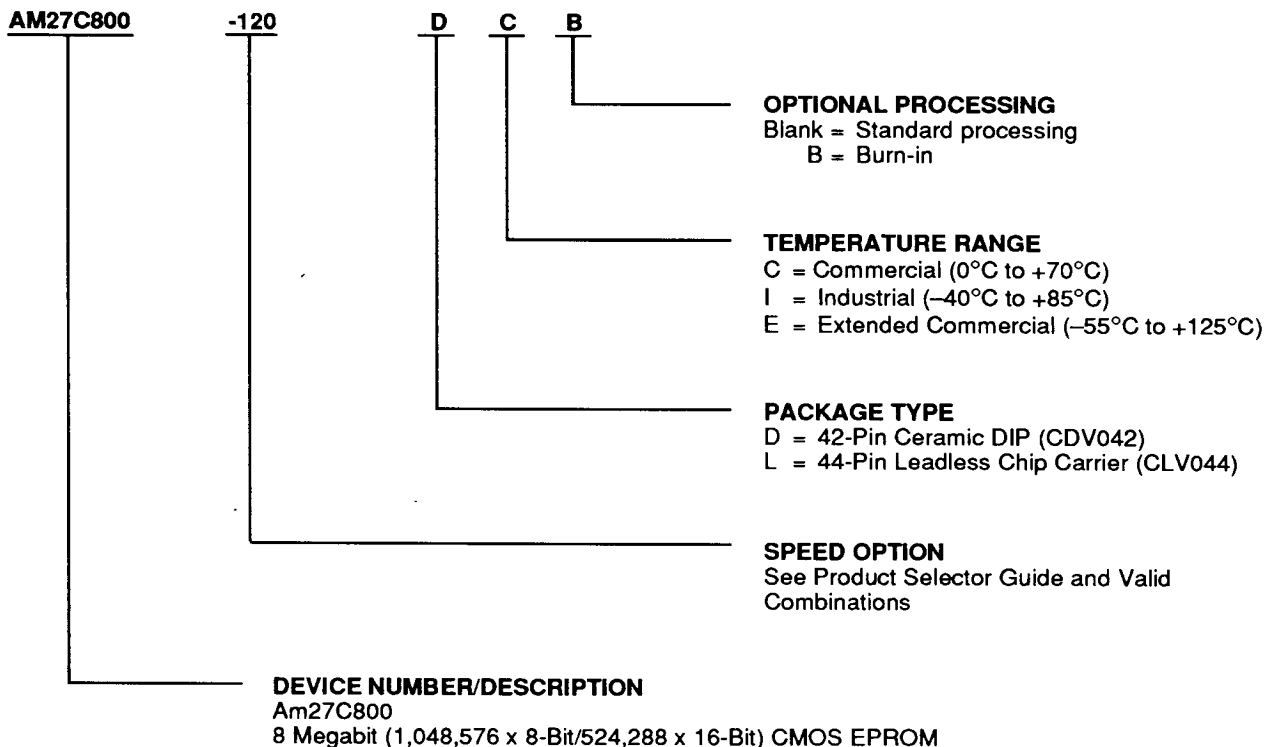## ORDERING INFORMATION

EPROM Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:

AM27C800   -120   D   C   B

OPTIONAL PROCESSING
Blank = Standard processing
B = Burn-in

TEMPERATURE RANGE
C = Commercial (0°C to +70°C)
I = Industrial (–40°C to +85°C)
E = Extended Commercial (–55°C to +125°C)

PACKAGE TYPE
D = 42-Pin Ceramic DIP (CDV042)
L = 44-Pin Leadless Chip Carrier (CLV044)

SPEED OPTION
See Product Selector Guide and Valid Combinations

DEVICE NUMBER/DESCRIPTION
Am27C800
8 Megabit (1,048,576 x 8-Bit/524,288 x 16-Bit) CMOS EPROM

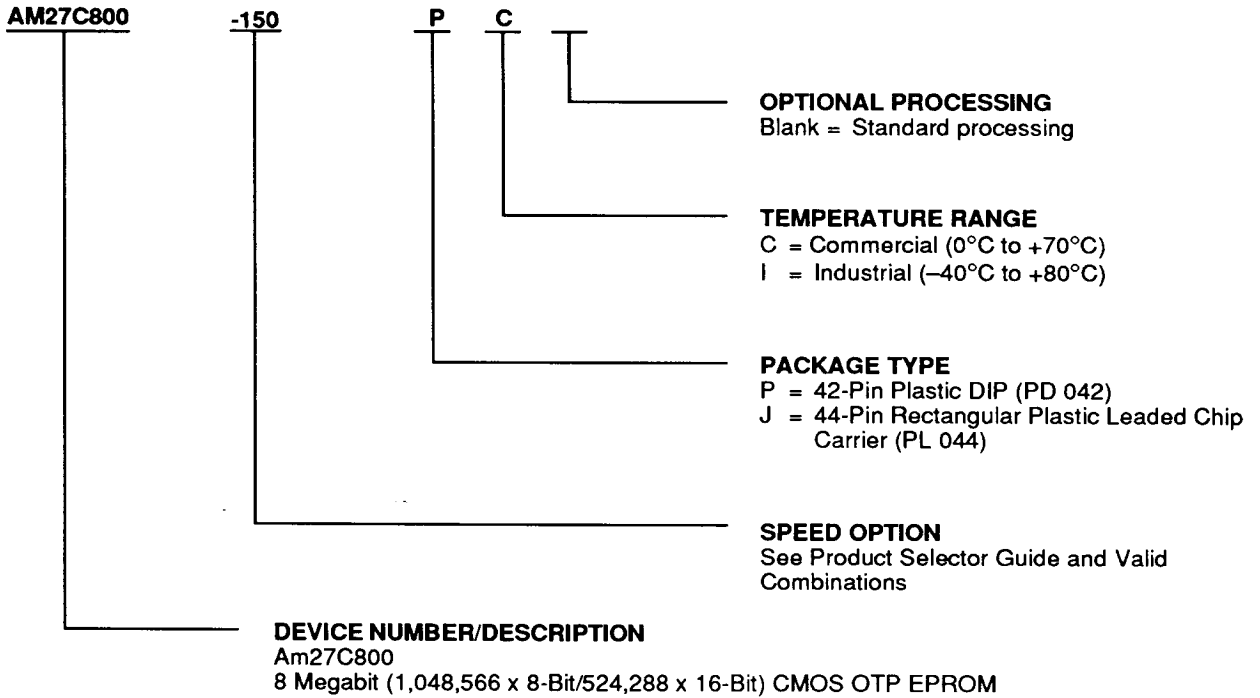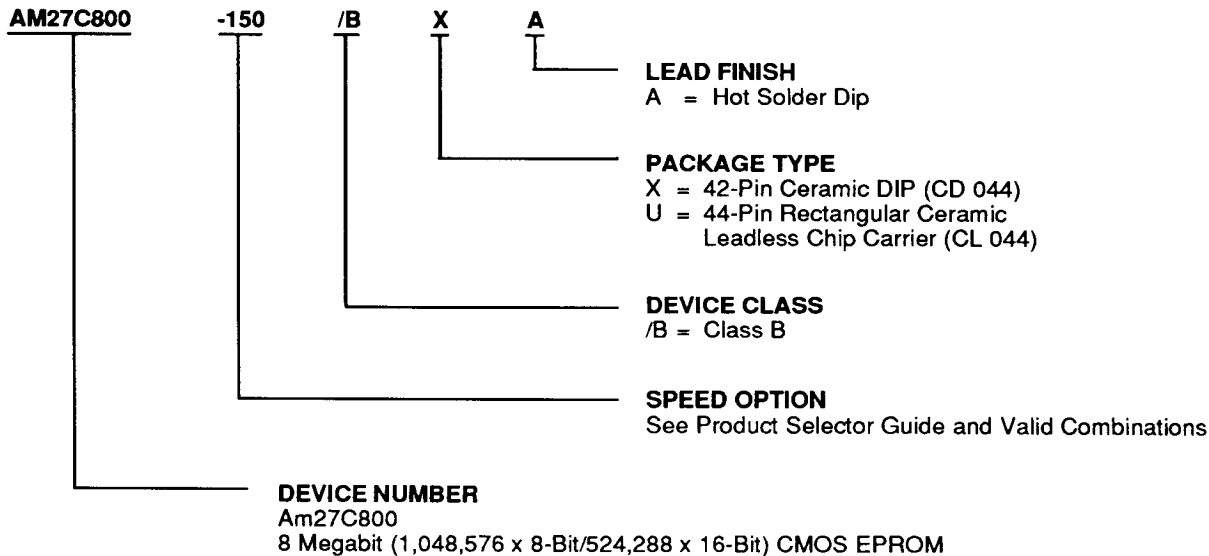| Valid Combinations	
AM27C800-120	
AM27C800-125	DC, DCB, DI, DIB,
AM27C800-150	DE, DEB, LC, LCB,
AM27C800-200	LI, LIB, LE, LEB
AM27C800-255	

Valid Combinations
Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

ORDERING INFORMATION

OTP Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:

AM27C800   -150   P   C

OPTIONAL PROCESSING
Blank = Standard processing

TEMPERATURE RANGE
C = Commercial (0°C to +70°C)
I = Industrial (−40°C to +80°C)

PACKAGE TYPE
P = 42-Pin Plastic DIP (PD 042)
J = 44-Pin Rectangular Plastic Leaded Chip
     Carrier (PL 044)

SPEED OPTION
See Product Selector Guide and Valid
Combinations

DEVICE NUMBER/DESCRIPTION
Am27C800
8 Megabit (1,048,566 x 8-Bit/524,288 x 16-Bit) CMOS OTP EPROM

Valid Combinations	
AM27C800-150	
AM27C800-155	PC, JC, PI, JI
AM27C800-200	
AM27C800-255	

Valid Combinations
Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

ORDERING INFORMATION

Military APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883 requirements. The order number (Valid Combination) is formed by a combination of:

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AM27C800    -150   /B   X    A
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LEAD FINISH
A = Hot Solder Dip

PACKAGE TYPE
X = 42-Pin Ceramic DIP (CD 044)
U = 44-Pin Rectangular Ceramic
    Leadless Chip Carrier (CL 044)

DEVICE CLASS
/B = Class B

SPEED OPTION
See Product Selector Guide and Valid Combinations

DEVICE NUMBER
Am27C800
8 Megabit (1,048,576 x 8-Bit/524,288 x 16-Bit) CMOS EPROM

Valid Combinations	
AM27C800-150	
AM27C800-200	/BUA, /BXA
AM27C800-250	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

Group A Tests

Group A tests consist of Subgroups
1, 2, 3, 7, 8, 9, 10, 11.

FUNCTIONAL DESCRIPTION

Erasing the Am27C800

In order to clear all locations of their programmed contents, it is necessary to expose the Am27C800 to an ultraviolet light source. A dosage of 15 W seconds/cm^2 is required to completely erase an Am27C800. This dosage can be obtained by exposure to an ultraviolet lamp — wavelength of 2,537 Å—with intensity of 12,000 μW/cm^2 for 15 to 20 minutes. The Am27C800 should be directly under and about one inch from the source and all filters should be removed from the UV light source prior to erasure.

It is important to note that the Am27C800 and similar devices will erase with light sources having wavelengths shorter than 4000 Å. Although erasure times will be much longer than with UV sources at 2,537Å, exposure to fluorescent light and sunlight will eventually erase the Am27C800 and exposure to them should be prevented to realize maximum system reliability. If used in such an environment, the package window should be covered by an opaque label or substance.

Programming the Am27C800

Upon delivery or after each erasure the Am27C800 has all 8,388,608 bits in the "ONE" or HIGH state. "ZEROs" are loaded into the Am27C800 through the procedure of programming.

The programming mode is entered when 12.75 V ± 0.25 V is applied to the V_{PP} pin, $\overline{CE/PGM}$ is at V_{IL}, and $\overline{OE}$ is at V_{IH}.

For programming, the data to be programmed is applied 16 bits in parallel to the data output pins.

The Flashrite algorithm reduces programming time by using 100 μs programming pulses and by giving each addresss only as many pulses as is necessary in order to reliably program the data. After each pulse is applied to a given address, the data in that address is verified. If the data does not verify, additional pulses are given until it verifies or the maximum is reached. This process is repeated while sequencing through each address of the Am27C800. This part of the algorithm is done at V_{CC} = 6.25 V to assure that each EPROM bit is programmed to a sufficiently high threshold voltage. After the final address is completed, the entire EPROM memory is verified at V_{CC} = V_{PP} = 5.25 V.

Please refer to Section 6.0 for programming flow chart and characteristics.

Program Inhibit

Programming of multiple Am27C800s in parallel with different data is also easily accomplished. Except for $\overline{CE/PGM}$, all like inputs of the parallel Am27C800 may be common. A TTL low-level program pulse applied to an Am27C800 $\overline{CE/PGM}$ input with V_{PP} = 12.75 V ± 0.25 V, and $\overline{OE}$ HIGH will program that Am27C800. A high-level $\overline{CE/PGM}$ input inhibits the other Am27C800 devices from being programmed.

Program Verify

A verify should be performed on the programmed bits to determine that they were correctly programmed. The verify should be performed with $\overline{OE}$ at V_{IL}, $\overline{CE/PGM}$ at V_{IH} and V_{PP} between 12.5 V and 13.0 V.

Auto Select Mode

The auto select mode allows the reading out of a binary code from an EPROM that will identify its manufacturer and type. This mode is intended for use by programming equipment for the purpose of automatically matching the device to be programmed with its corresponding programming algorithm. This mode is functional in the 25°C ± 5°C ambient temperature range that is required when programming the Am27C800.

To activate this mode, the programming equipment must force 12.0 V ± 0.5 V on address line A9 of the Am27C800. Two identifier bytes may then be sequenced from the device outputs by toggling address line A0 from V_{IL} to V_{IH}. All other address lines must be held at V_{IL} during auto select mode.

Byte 0 (A0 = V_{IL}) represents the manufacturer code, and Byte 1 (A0 = V_{IH}), the device identifier code. For the Am27C800, these two identifier bytes are given in the Mode Select table. All identifiers for manufacturer and device codes will possess odd parity, with the MSB (DQ7) defined as the parity bit.

Read Mode

The Am27C800 has two control functions, both of which must be logically satisfied in order to obtain data at the outputs. Chip Enable ($\overline{CE/PGM}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that addresses are stable, address access time (t_{ACC}) is equal to the delay from $\overline{CE/PGM}$ to output (t_{CE}). Data is available at the outputs t_{OE} after the falling edge of $\overline{OE}$, assuming that $\overline{CE/PGM}$ has been LOW and addresses have been stable for at least $t_{ACC} - t_{OE}$.

Byte Mode

The user has the option of reading data in either 16-bit words or 8-bit bytes under control of the $\overline{BYTE}$ input. With the $\overline{BYTE}$ input HIGH, inputs A18–A0 will address 512K words of 16-bit data. When the $\overline{BYTE}$ input is LOW, AB functions as the least significant address input and 1 Mbyte of data can be accessed. The 8 bits of data will appear on DQ7–DQ0.

Standby Mode

The Am27C800 has a CMOS standby mode which reduces the maximum V_{CC} current to 100 µA. It is placed in CMOS-standby when $\overline{CE/PGM}$ is at $V_{CC} \pm 0.3$ V. The Am27C800 also has a TTL-standby mode which reduces the maximum V_{CC} current to 1.0 mA. It is placed in TTL-standby when $\overline{CE/PGM}$ is at V_{IH}. When in standby mode, the outputs are in a high-impedance state, independent of the $\overline{OE}$ input.

Output OR-Tieing

To accommodate multiple memory connections, a two-line control function is provided to allow for:

■ Low memory power dissipation

■ Assurance that output bus contention will not occur

It is recommended that $\overline{CE/PGM}$ be decoded and used as the primary device-selecting function, while $\overline{OE}$ be made a common connection to all devices in the array and connected to the READ line from the system control

bus. This assures that all deselected memory devices are in their low-power standby mode and that the output pins are only active when data is desired from a particular memory device.

System Applications

During the switch between active and standby conditions, transient current peaks are produced on the rising and falling edges of Chip Enable. The magnitude of these transient current peaks is dependent on the output capacitance loading of the device. At a minimum, a 0.1 µF ceramic capacitor (high frequency, low inherent inductance) should be used on each device between V_{CC} and V_{SS} to minimize transient effects. In addition, to overcome the voltage drop caused by the inductive effects of the printed circuit board traces on EPROM arrays, a 4.7 µF bulk electrolytic capacitor should be used between V_{CC} and V_{SS} for each eight devices. The location of the capacitor should be close to where the power supply is connected to the array.

MODE SELECT TABLE

Mode	Pins	$\overline{CE/PGM}$	$\overline{OE}$	A0	A9	$\overline{BYTE}/V_{PP}$	Outputs
Read		V_{IL}	V_{IL}	X	X	X	D_{OUT}
Output Disable		V_{IL}	V_{IH}	X	X	X	Hi-Z
Standby (TTL)		V_{IH}	X	X	X	X	Hi-Z
Standby (CMOS)		$V_{CC} \pm 0.3$ V	X	X	X	X	Hi-Z
Program		V_{IL}	V_{IH}	X	X	V_{PP}	D_{IN}
Program Verify		V_{IH}	V_{IL}	X	X	V_{PP}	D_{OUT}
Program Inhibit		V_{IH}	V_{IH}	X	X	V_{PP}	Hi-Z
Auto Select (Note 3)	Manufacturer Code	V_{IL}	V_{IL}	V_{IL}	V_H	X	01H
	Device Code	V_{IL}	V_{IL}	V_{IH}	V_H	X	1AH

Notes:

1. $V_H = 12.0$ V $+ 0.5$ V

2. $X = $ Either V_{IH} or V_{IL}

3. A1–A8 = A10–A18 = V_{IL}, AB = X

4. See DC Programming Characteristics for V_{PP} voltage during programming.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature
  OTP Products .... –65°C to +125°C
  All Other Products .... –65°C to +150°C
Ambient Temperature
with Power Applied .... –55°C to +125°C
Voltage with Respect To V_{SS}
  All pins except A9, V_{PP}, V_{CC}
  (Note 1) .... –0.6 V to V_{CC} + 0.6 V

  A9 and V_{PP} (Note 2) .... –0.6 V to +13.5 V

  V_{CC} .... –0.6 V to +7.0 V

Notes:
1. During transitions, the inputs may overshoot V_{SS} to –2.0 V for periods of up to 20 ns. Maximum DC voltage on input may overshoot to V_{CC} + 2.0 V for periods of up to 20 ns.

2. During transitions, A9 and V_{PP} may overshoot V_{SS} to –2.0 V for periods of up to 20 ns. A9 and V_{PP} must not exceed 13.5 V for any period of time.

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure of the device to absolute maximum rating conditions for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
  Case Temperature (T_C) .... 0°C to +70°C
Industrial (I) Devices
  Case Temperature (T_C) .... –40°C to +85°C
Extended Commercial (E) Devices
  Case Temperature (T_C) .... –55°C to +125°C
Military (M) Devices
  Case Temperature (T_C) .... –55°C to +125°C
Supply Read Voltages
  V_{CC} for Am27C800-XX5 ..... +4.75 V to +5.25 V

  V_{CC} for Am27C800-XX0 ..... +4.50 V to +5.50 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range unless otherwise specified. (Notes 1, 2 and 4) (for APL Products, Group A, Subgroups 1, 2, 3, 6 and 7 are tested unless otherwise noted)

Parameter Symbol	Parameter Description	Test Conditions		Min	Max	Unit
V_{OH}	Output HIGH Voltage	$I_{OH} = -400\ \mu A$		2.4		V
V_{OL}	Output LOW Voltage	$I_{OL} = 2.1$ mA			0.45	V
V_{IH}	Input HIGH Voltage			2.0	$V_{CC} + 0.5$	V
V_{IL}	Input LOW Voltage			−0.5	+0.8	V
I_{LI}	Input Load Current	$V_{IN} = 0$ V to $+V_{CC}$			1.0	μA
I_{LO}	Output Leakage Current	$V_{OUT} = 0$ V to $+V_{CC}$			5.0	μA
I_{CC1}	Vcc Active Current (Note 3)	$\overline{CE} = V_{IL}$, f = 5 MHz, $I_{OUT} = 0$ mA	C/I Devices		50	mA
			E/M Devices		60	
I_{CC2}	Vcc TTL Standby Current	$\overline{CE} = V_{IH}$			1.0	mA
I_{CC3}	Vcc CMOS Standby Current	$\overline{CE} = V_{CC} \pm 0.3$ V			100	μA
I_{PP1}	VPP Current During Read	$\overline{CE} = \overline{OE} = V_{IL}$, $V_{PP} = V_{CC}$			100	μA

Notes:

1. V_{CC} must be applied simultaneously or before V_{PP}, and removed simultaneously or after V_{PP}.

2. **Caution:** The Am27C800 must not be removed from (or inserted into) a socket when V_{CC} or V_{PP} is applied.

3. I_{CC1} is tested with $\overline{OE}/V_{PP} = V_{IH}$ to simulate open outputs.

4. Minimum DC Input Voltage is −0.5 V. During transitions, the inputs may overshoot to −2.0 V for periods less than 20 ns. Maximum DC Voltage on output pins is $V_{CC} + 0.5$ V, which may overshoot to $V_{CC} + 2.0$ V for periods less than 20 ns.
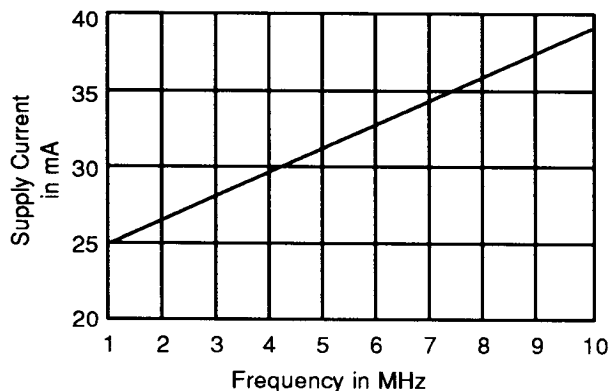

Figure 1. Typical Supply Current
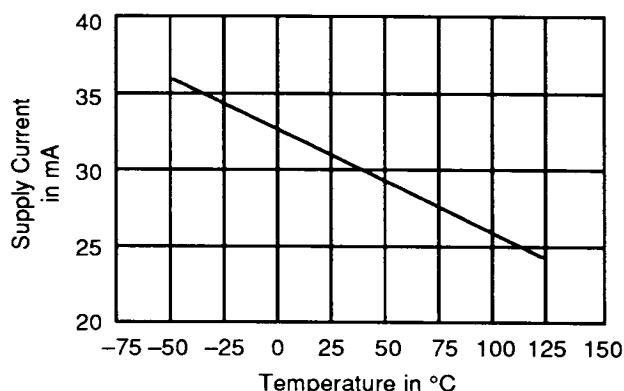vs. Frequency
Vcc = 5.5 V, T = 25°C

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Figure 2. Typical Supply Current
vs. Temperature
Vcc = 5.5 V, f = 5 MHz

15452B-6

CAPACITANCE

Parameter Symbol	Parameter Description	Test Conditions	CDV042 Typ	CDV042 Max	CLV044 Typ	CLV044 Max	PD 042 Typ	PD 042 Max	PL 044 Typ	PL 044 Max	Unit
C_{IN}	Input Capacitance	$V_{IN} = 0$	10	18	10	18	10	18	10	18	pF
C_{OUT}	Output Capacitance	$V_{OUT} = 0$	10	18	10	18	10	18	10	18	pF

Notes:

1. This parameter is only sampled and not 100% tested.

2. $T_A = +25°C$, $f = 1$ MHz

SWITCHING CHARACTERISTICS over operating ranges unless otherwise specified (Notes 1, 3 and 4) (for APL Products, Group A, Subgroups 9, 10 and 11 are tested unless otherwise noted)

| JEDEC	Standard	Parameter Description	Test Conditions		Am27C800 -125 -120	-150	-200	-255 -250	Unit
tAVQV	tACC	Address to Output Delay	$\overline{CE} = \overline{OE} = V_{IL}$	Min	–	–	–	–	ns
				Max	120	150	200	250	
tELQV	tCE	Chip Enable to Output Delay	$\overline{OE} = V_{IL}$	Min	–	–	–	–	ns
				Max	120	150	200	250	
tGLQV	tOE	Output Enable to Output Delay	$\overline{CE} = V_{IL}$	Min	–	–	–	–	ns
				Max	50	55	60	60	
tEHQZ, tGHQZ	tDF (Note 2)	Chip Enable HIGH or Output Enable HIGH, whichever comes first, to Output Float		Min	0	0	0	0	ns
				Max	40	40	40	60	
tAXQX	tOH	Output Hold from Addresses, $\overline{CE}$, or $\overline{OE}$, whichever occurred first		Min	0	0	0	0	ns
				Max	–	–	–	–	

Notes:

1. V_{CC} must be applied simultaneously or before V_{PP}, and removed simultaneously or after V_{PP}.

2. This parameter is only sampled and not 100% tested.

3. Caution: The Am27C800 must not be removed from (or inserted into) a socket or board when V_{PP} or V_{CC} is applied.

4. Output Load: 1 TTL gate and $C_L = 100$ pF
   Input Rise and Fall Times: 20 ns
   Input Pulse Levels: 0.45 V to 2.4 V
   Timing Measurement Reference Level: Inputs: 0.8 V and 2.0 V
   Outputs: 0.8 V and 2.0 V

SWITCHING TEST CIRCUIT
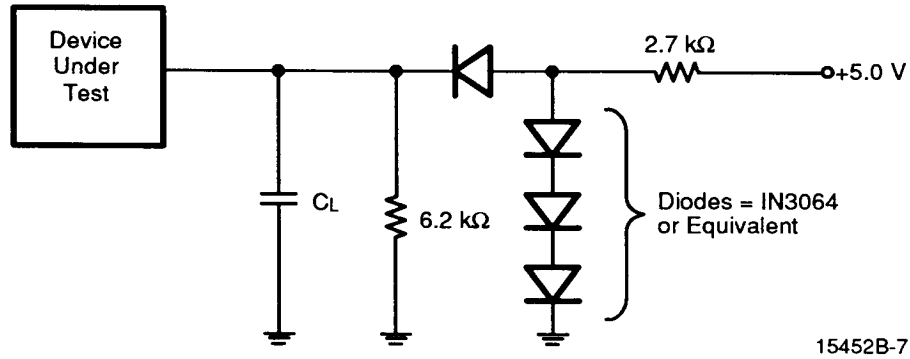
C_L = 100 pF including jig capacitance

SWITCHING TEST WAVEFORM
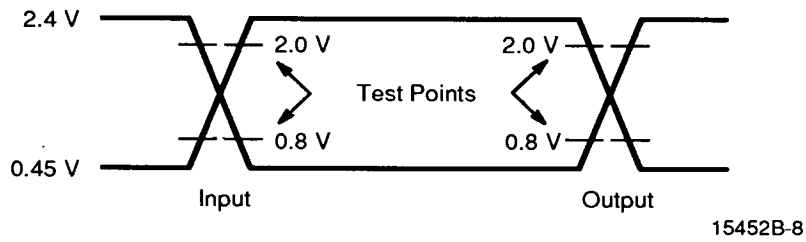
AC Testing: Inputs are driven at 2.4 V for a logic "1" and 0.45 for a logic "0". Input pulse rise and fall times are ≤ 20 ns.

KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	Must Be Steady	Will Be Steady
	May Change from H to L	Will Be Changing from H to L
	May Change from L to H	Will Be Changing from L to H
	Don't Care, Any Change Permitted	Changing, State Unknown
	Does Not Apply	Center Line is High Impedance "Off" State

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SWITCHING WAVEFORMS
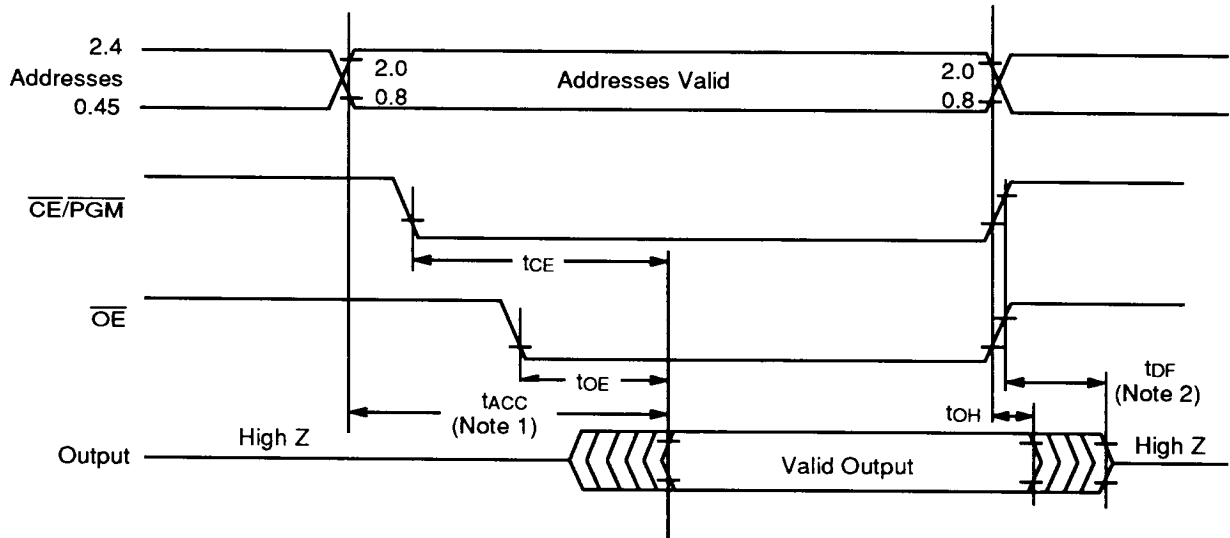
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Notes:

1. $\overline{OE}/V_{PP}$ may be delayed up to $t_{ACC} - t_{OE}$ after the falling edge of the addresses without impact on t_{ACC}.

2. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$, whichever occurs first.