

# Wireless Components

ASK/FSK Single Conversion Receiver

TDA 5211 Version 2.0

Specification May 2001

<b>Revision History</b>		
Current Version: 2.0 as of 18.05.01		
Previous Version: 1.1, Dec. 2000		
Page (in previous Version)	Page (in current Version)	Subjects (major changes since last revision)
3-12	3-12	Sec. 3.4.8: max. datarate changed, Sec. 3.4.9: max. output current changed
4-4	4-4	value of a changed to 1.414
4-13	4-13	value for C2 changed to 22nF according to bill of materials, $\tau_2$ and $T_2$ changed
5-3	5-3	min. supply current limits added, max. limits changed
5-4	5-4	supply current max. limit changed, min. limit added
5-5	5-5	3VOUT min. & max. limits changed, TAGC typ. & max. values changed
5-6	5-6	Section "SLICER" reworked, max. datarate at given load capacitance quoted, high output voltage limits changed, precharge current: min., max. limits changed
5-7	5-7	PDO load and leakage currents limits and typ. values changed, FSK demodulation gain min. limit changed
5-9	5-9	PDWN-current max. limit changed, supply currents min. limits added, max. limits changed, 3VOUT min. & max. limits changed, $I_{TAGC\_out}$ limits changed
5-10	5-10	Section "SLICER" reworked, max. datarate at given load capacitance quoted, high output voltage limits changed, precharge current: min., max. limits changed, PDO output voltage removed
5-15	5-15	C18 value changed

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**Published by Infineon Technologies AG,  
Balanstraße 73,  
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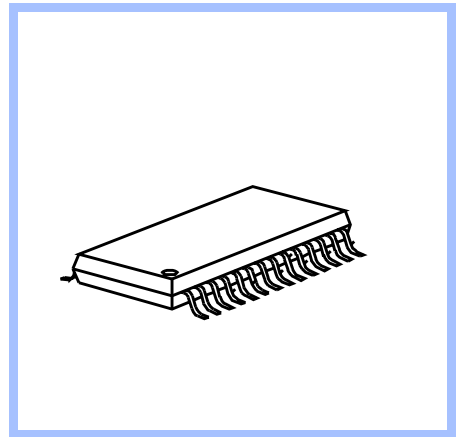
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## Product Info

### General Description

The IC is a very low power consumption single chip FSK/ASK Superheterodyne Receiver (SHR) for the frequency band 310 to 350 MHz that is pin compatible with the ASK Receiver TDA5201. The IC offers a high level of integration and needs only a few external components. The device contains a low noise amplifier (LNA), a double balanced mixer, a fully integrated VCO, a PLL synthesiser, a crystal oscillator, a limiter with RSSI generator, a PLL FSK demodulator, a data filter, a data comparator (slicer) and a peak detector. Additionally there is a power down feature to save battery life.

### Package



### Features

- Low supply current ( $I_s = 5.7 \text{ mA}$  typ. in FSK mode,  $I_s = 5 \text{ mA}$  typ. in ASK mode)
- Supply voltage range  $5V \pm 10\%$
- Power down mode with very low supply current ( $50\text{nA}$  typ.)
- FSK and ASK demodulation capability
- Fully integrated VCO and PLL Synthesiser
- ASK sensitivity better than  $-110 \text{ dBm}$  over specified temperature range ( $-40$  to  $+105^\circ\text{C}$ )
- Selectable frequency ranges 310-330 MHz and 330-350 MHz
- Limiter with RSSI generation, operating at 10.7MHz
- Selectable reference frequency
- 2nd order low pass data filter with external capacitors
- Data slicer with self-adjusting threshold
- FSK sensitivity better than  $-102 \text{ dBm}$  over specified temperature range ( $-40$  to  $+105^\circ\text{C}$ )

### Applications

- Keyless Entry Systems
- Remote Control Systems
- Alarm Systems
- Low Bitrate Communication Systems

### Ordering Information

Type	Ordering Code	Package
TDA 5211	Q67037-A1147	P-TSSOP-28-1
samples available		

# 1

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# 2 Product Description

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## 2.1 Overview

The IC is a very low power consumption single chip FSK/ASK Superheterodyne Receiver (SHR) for receive frequencies between 310 and 350 MHz that is pin compatible to the ASK Receiver TDA5201. The IC offers a high level of integration and needs only a few external components. The device contains a low noise amplifier (LNA), a double balanced mixer, a fully integrated VCO, a PLL synthesiser, a crystal oscillator, a limiter with RSSI generator, a PLL FSK demodulator, a data filter, a data comparator (slicer) and a peak detector. Additionally there is a power down feature to save battery life.

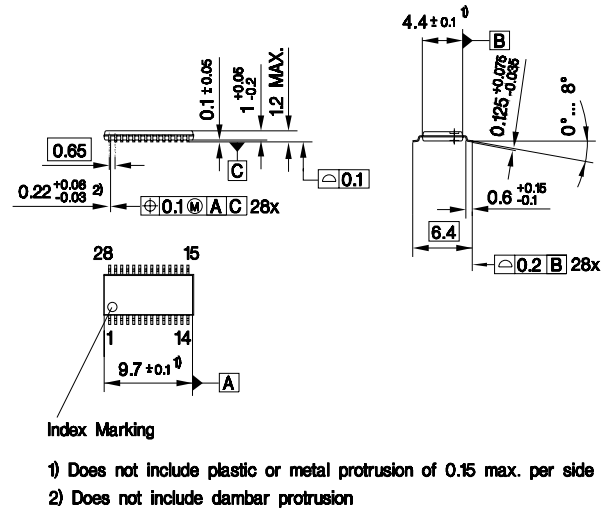
## 2.2 Application

- Keyless Entry Systems
- Remote Control Systems
- Alarm Systems
- Low Bitrate Communication Systems

## 2.3 Features

- Low supply current ( $I_s = 5.7$  mA typ. FSK mode, 5mA typ. ASK mode)
- Supply voltage range 5V  $\pm$ 10%
- Power down mode with very low supply current (50nA typ.)
- FSK and ASK demodulation capability
- Fully integrated VCO and PLL Synthesiser
- RF input sensitivity ASK -113dBm typ. at 25°C, better than -110dBm over complete specified operating temperature range (-40 to +105°C)
- RF input sensitivity FSK -105dBm typ. at 25°C, better than -102dBm over complete specified operating temperature range (-40 to +105°C)
- Receive frequency range between 310 and 350 MHz
- Selectable reference frequency
- Limiter with RSSI generation, operating at 10.7MHz
- 2nd order low pass data filter with external capacitors
- Data slicer with self-adjusting threshold

## 2.4 Package Outlines



P\_TSSOP\_28.EPS

Figure 2-1 P-TSSOP-28-1 package outlines

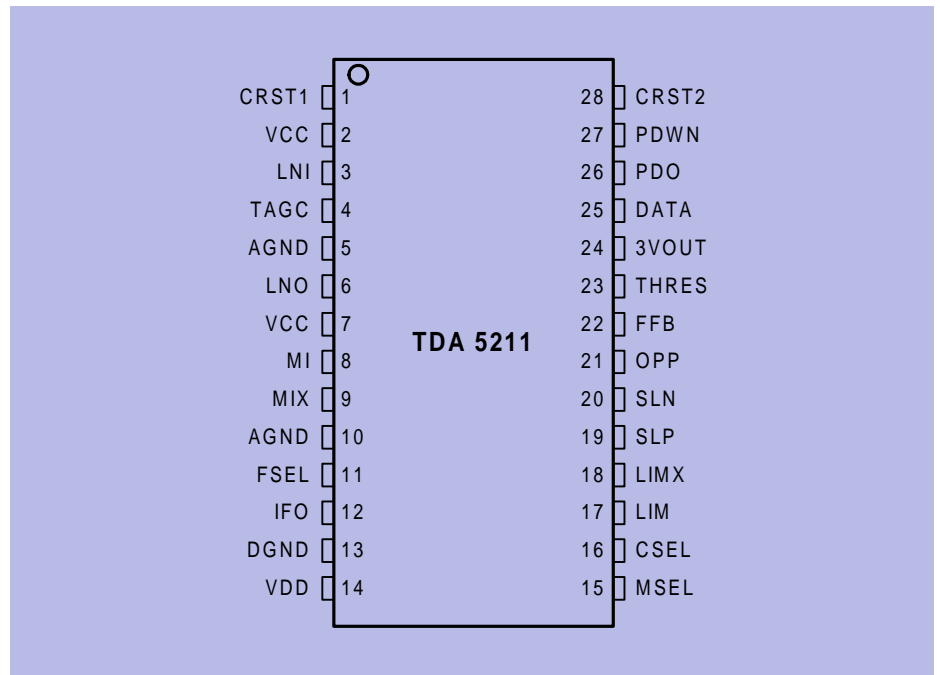


# 3 Functional Description

## Contents of this Chapter

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### 3.1 Pin Configuration

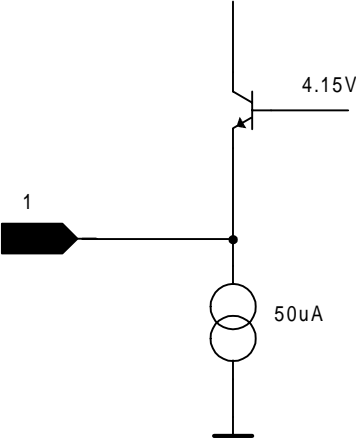
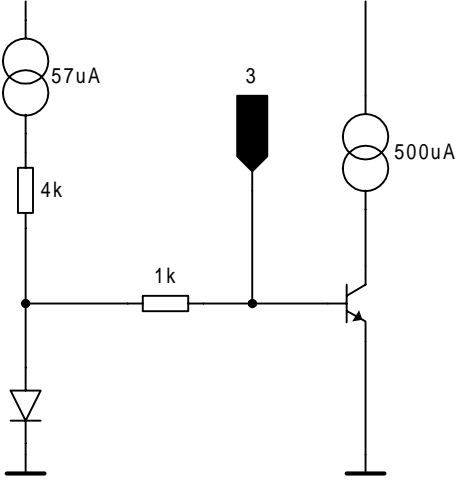


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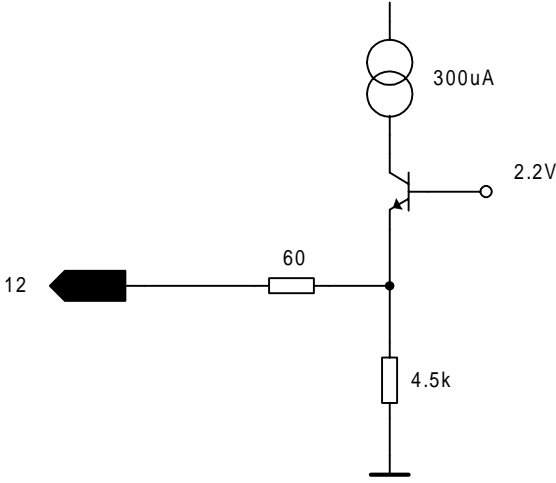
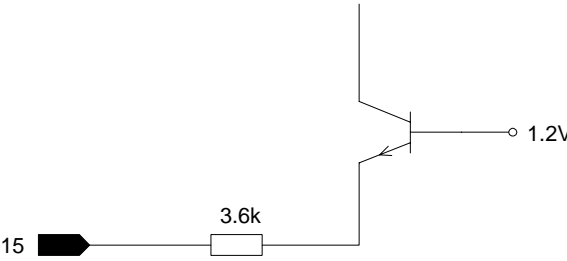
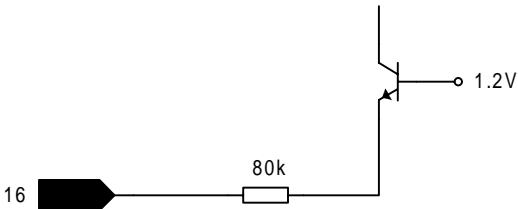
Figure 3-1 IC Pin Configuration

### 3.2 Pin Definition and Function

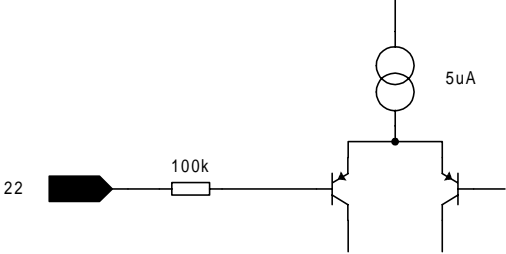
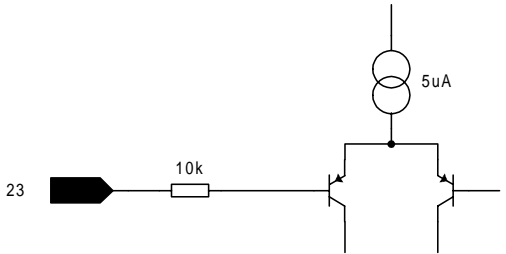
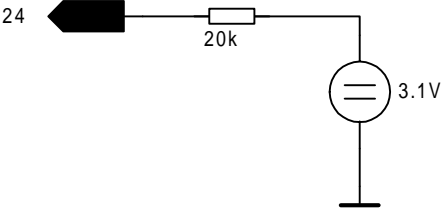
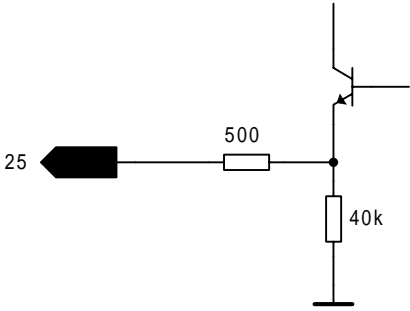
In the subsequent table the internal circuits connected to the pins of the device are shown. ESD-protection circuits are omitted to ease reading.

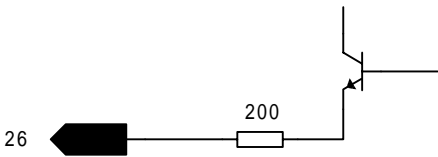
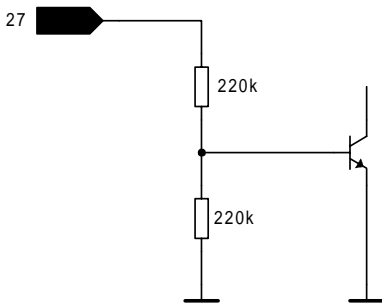
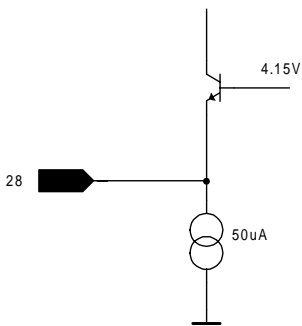
Table 3-1 Pin Definition and Function			
Pin No.	Symbol	Equivalent I/O-Schematic	Function
1	CRST1		External Crystal Connector 1
2	VCC		5V Supply
3	LNI		LNA Input

4	TAGC		AGC Time Constant Control
5	AGND		Analogue Ground Return
6	LNO		LNA Output
7	VCC		5V Supply
8	MI		Mixer Input
9	MIX		Complementary Mixer Input
10	AGND		Analogue Ground Return
11	FSEL		not applicable - has to be left open

12	IFO		10.7 MHz IF Mixer Output
13	DGND		Digital Ground Return
14	VDD		5V Supply (PLL Counter Circuitry)
15	MSEL		ASK/FSK Modulation Format Selector
16	CSEL		6.xx or 13.xx MHz Quartz Selector

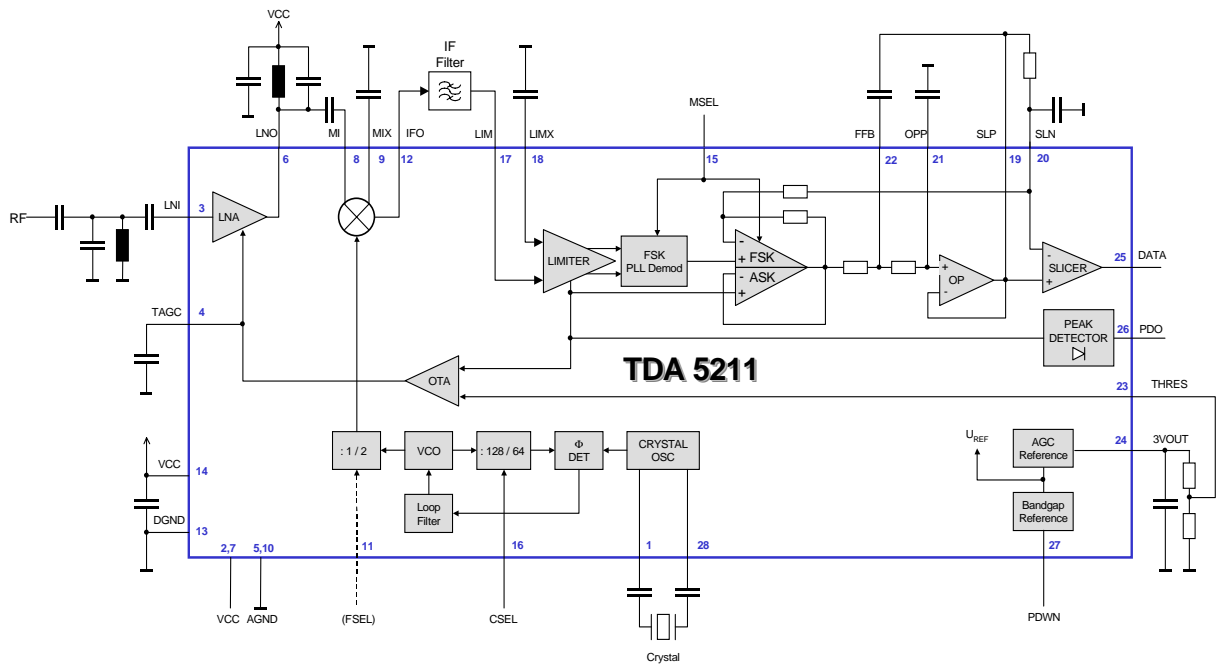
<p>17 18</p>	<p>LIM LIMX</p>		<p>Limiter Input Complementary Limiter Input</p>
<p>19</p>	<p>SLP</p>		<p>Data Slicer Positive Input</p>
<p>20</p>	<p>SLN</p>		<p>Data Slicer Negative Input</p>
<p>21</p>	<p>OPP</p>		<p>OpAmp Noninverting Input</p>

22	FFB		Data Filter Feedback Pin
23	THRES		AGC Threshold Input
24	3VOUT		3V Reference Output
25	DATA		Data Output

26	PDO		Peak Detector Output
27	PDWN		Power Down Input
28	CRST2		External Crystal Connector 2



### 3.3 Functional Block Diagram



Functional\_diagram\_5211.wmf

Figure 3-2 Main Block Diagram

### 3.4 Functional Blocks

#### 3.4.1 Low Noise Amplifier (LNA)

The LNA is an on-chip cascode amplifier with a voltage gain of 15 to 20dB. The gain figure is determined by the external matching networks situated ahead of LNA and between the LNA output **LNO** (Pin 6) and the Mixer Inputs **MI** and **MIX** (Pins 8 and 9). The noise figure of the LNA is approximately 3dB, the current consumption is 500µA. The gain can be reduced by approximately 18dB. The switching point of this AGC action can be determined externally by applying a threshold voltage at the **THRES** pin (Pin 23). This voltage is compared internally with the received signal (RSSI) level generated by the limiter circuitry. In case that the RSSI level is higher than the threshold voltage the LNA gain is reduced and vice versa. The threshold voltage can be generated by attaching a voltage divider between the **3VOUT** pin (Pin 24) which provides a temperature stable 3V output generated from the internal bandgap voltage and the **THRES** pin as described in Section 4.1. The time constant of the AGC action can be deter-

mined by connecting a capacitor to the **TAGC** pin (Pin 4) and should be chosen along with the appropriate threshold voltage according to the intended operating case and interference scenario to be expected during operation. The optimum choice of AGC time constant and the threshold voltage is described in Section 4.1.

### 3.4.2 Mixer

The Double Balanced Mixer downconverts the input frequency (RF) in the range of 310-350MHz to the intermediate frequency (IF) at 10.7MHz with a voltage gain of approximately 21dB by utilising either high- or low-side injection of the local oscillator signal. In case the mixer is interfaced only single-ended, the unused mixer input has to be tied to ground via a capacitor. The mixer is followed by a low pass filter with a corner frequency of 20MHz in order to suppress RF signals to appear at the IF output (**IFO** pin). The IF output is internally consisting of an emitter follower that has a source impedance of approximately 330Ω to facilitate interfacing the pin directly to a standard 10.7MHz ceramic filter without additional matching circuitry.

### 3.4.3 PLL Synthesizer

The Phase Locked Loop synthesizer consists of a VCO, an asynchronous divider chain, a phase detector with charge pump and a loop filter and is fully implemented on-chip. The VCO is including spiral inductors and varactor diodes. The **FSEL** pin (Pin11) has to be left open. The tuning range of the VCO was designed to guarantee over production spread and the specified temperature range a receive frequency range between 310 and 350MHz depending on whether high- or low-side injection of the local oscillator is used. The oscillator signal is fed both to the synthesiser divider chain and to a divider that is dividing the signal by 2 before it is applied to the downconverting mixer. Local oscillator high side injection has to be used for receive frequencies between approximately 310 and 330 MHz, low side injection for receive frequencies between 330 and 350MHz - see also Section 4.4..

### 3.4.4 Crystal Oscillator

The on-chip crystal oscillator circuitry allows for utilisation of quartzes both in the 5 and 10MHz range as the overall division ratio of the PLL can be switched between 32 and 64 via the **CSEL** (Pin 16 ) pin according to the following table.

Table 3-2 CSEL Pin Operating States	
CSEL	Crystal Frequency
Open	5.xx MHz
Shorted to ground	10.xx MHz

The calculation of the value of the necessary quartz load capacitance is shown in Section 4.3, the quartz frequency calculation is explained in Section 4.4.

### 3.4.5 Limiter

The Limiter is an AC coupled multistage amplifier with a cumulative gain of approximately 80 dB that has a bandpass-characteristic centred around 10.7 MHz. It has a typical input impedance of 330 Ω to allow for easy interfacing to a 10.7 MHz ceramic IF filter. The limiter circuit also acts as a Receive Signal Strength Indicator (RSSI) generator which produces a DC voltage that is directly proportional to the input signal level as can be seen in Figure 4-2. This signal is used to demodulate ASK-modulated receive signals in the subsequent baseband circuitry. The RSSI output is applied to the modulation format switch, to the Peak Detector input and to the AGC circuitry.

In order to demodulate ASK signals the MSEL pin has to be left open as described in the next chapter.

### 3.4.6 FSK Demodulator

To demodulate frequency shift keyed (FSK) signals a PLL circuit is used that is contained fully on chip. The Limiter output differential signal is fed to the linear phase detector as is the output of the 10.7 MHz center frequency VCO. The demodulator gain is typically 140µV/kHz. The passive loop filter output that is comprised fully on chip is fed to both the VCO and the modulation format switch described in more detail below. This signal is representing the demodulated signal with low frequencies applied to the demodulator demodulated to logic ones and high frequencies demodulated to logic zeroes. However this is only valid in case the local oscillator is low-side injected to the mixer which is applicable to receive frequencies above 330MHz (e.g. 345MHz). In case of receive frequencies below 330MHz (e.g.315MHz) high frequencies are demodulated as logical ones due to a sign inversion in the downconversion mixing process. See also Section 4.4.

The modulation format switch is actually a switchable amplifier with an AC gain of 11 that is controlled by the **MSEL** pin (Pin 15) as shown in the following table. This gain was chosen to facilitate detection in the subsequent circuits. The DC gain is 1 in order not to saturate the subsequent Data Filter with the DC offset produced by the demodulator in case of large frequency offsets of the IF signal. The resulting frequency characteristic and details on the principle of operation of the switch are described in Section 4.6.

Table 3-3 MSEL Pin Operating States	
MSEL	Modulation Format
Open	ASK
Shorted to ground	FSK

The demodulator circuit is switched off in case of reception of ASK signals.

### 3.4.7 Data Filter

The data filter comprises an OP-Amp with a bandwidth of 100kHz used as a voltage follower and two 100kΩ on-chip resistors. Along with two external capacitors a 2nd order Sallen-Key low pass filter is formed. The selection of the capacitor values is described in Section 4.2.

### 3.4.8 Data Slicer

The data slicer is a fast comparator with a bandwidth of 100 kHz. This allows for a maximum receive data rate of up to 100kbaud. The maximum achievable data rate also depends on the IF Filter bandwidth and the local oscillator tolerance values. Both inputs are accessible. The output delivers a digital data signal (CMOS-like levels) for subsequent circuits. The self-adjusting threshold on pin 20 is generated by RC-term or peak detector depending on the baseband coding scheme. The data slicer threshold generation alternatives are described in more detail in Section 4.5.

### 3.4.9 Peak Detector

The peak detector generates a DC voltage which is proportional to the peak value of the receive data signal. An external RC network is necessary. The input is connected to the output of the RSSI-output of the Limiter, the output is connected to the **PDO** pin (Pin 26). This output can be used as an indicator for the received signal strength to use in wake-up circuits and as a reference for the data slicer in ASK mode. The output current is typically 950µA, the discharge current is lower than 2µA. Note that the RSSI level is also output in case of FSK mode.

### 3.4.10 Bandgap Reference Circuitry

A Bandgap Reference Circuit provides a temperature stable reference voltage for the device. A power down mode is available to switch off all subcircuits which is controlled by the PWDN pin (Pin 27) as shown in the following table. The supply current drawn in this case is typically 50nA.

PWDN	Operating State
Open or tied to ground	Powerdown Mode
Tied to Vs	Receiver On

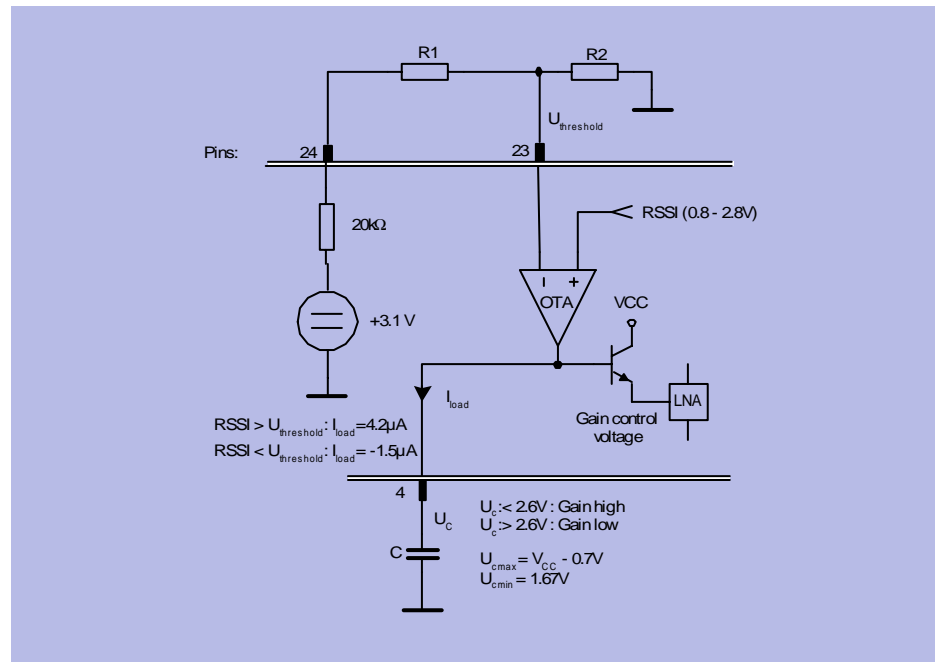
# 4 Applications

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## 4.1 Choice of LNA Threshold Voltage and Time Constant

In the following figure the internal circuitry of the LNA automatic gain control is shown.



LNA\_autom.wmf

Figure 4-1 LNA Automatic Gain Control Circuitry

The LNA automatic gain control circuitry consists of an operational transimpedance amplifier that is used to compare the received signal strength signal (RSSI) generated by the Limiter with an externally provided threshold voltage  $U_{thres}$ . As shown in the following figure the threshold voltage can have any value between approximately 0.8 and 2.8V to provide a switching point within the receive signal dynamic range.

This voltage  $U_{thres}$  is applied to the **THRES** pin (Pin 23). The threshold voltage can be generated by attaching a voltage divider between the **3VOUT** pin (Pin 24) which provides a temperature stable 3V output generated from the internal bandgap voltage and the **THRES** pin. If the RSSI level generated by the Limiter is higher than  $U_{thres}$ , the OTA generates a positive current  $I_{load}$ . This yields a voltage rise on the **TAGC** pin (Pin 4). Otherwise, the OTA generates a negative current. These currents do not have the same values in order to achieve a fast-attack and slow-release action of the AGC and are used to charge an external capacitor which finally generates the LNA gain control voltage.

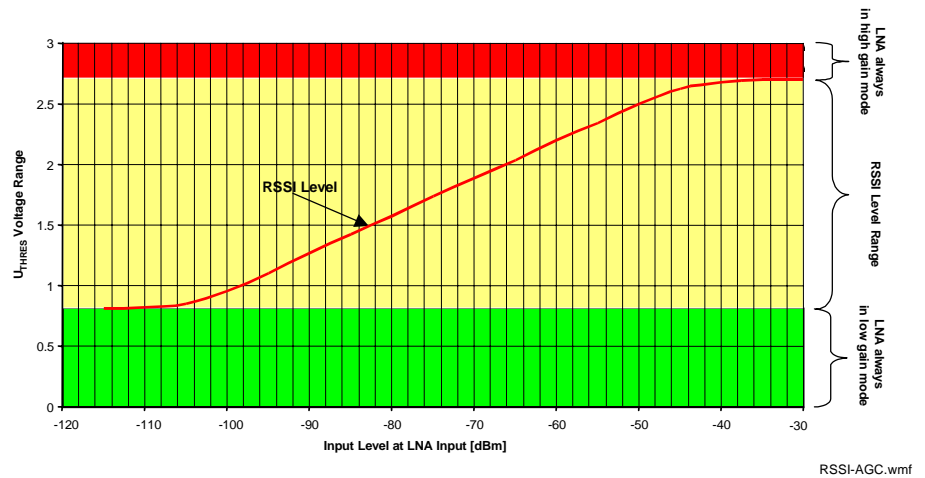


Figure 4-2 RSSI Level and Permissive AGC Threshold Levels

The switching point should be chosen according to the intended operating scenario. The determination of the optimum point is described in the accompanying Application Note, a threshold voltage level of 1.8V is apparently a viable choice. It should be noted that the output of the **3VOUT** pin is capable of driving up to 50µA, but that the **THRES** pin input current is only in the region of 40nA. As the current drawn out of the **3VOUT** pin is directly related to the receiver power consumption, the power divider resistors should have high impedance values. The sum of R1 and R2 has to be 600kΩ in order to yield 3V at the **3VOUT** pin. R1 can thus be chosen as 240kΩ, R2 as 360kΩ to yield an overall **3VOUT** output current of 5µA<sup>1</sup> and a threshold voltage of 1.8V

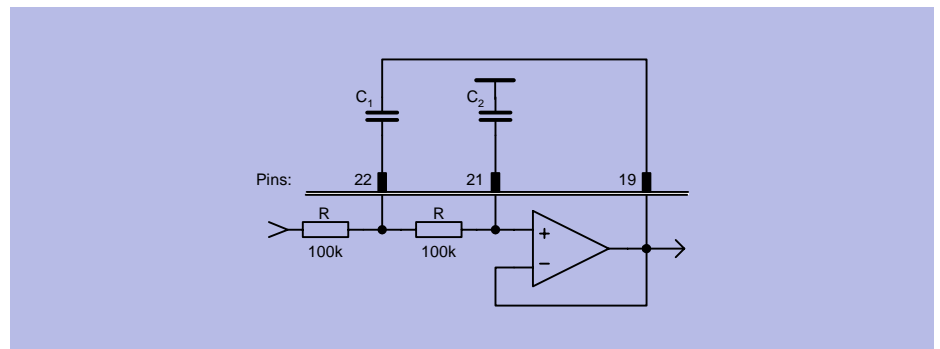
**Note:** If the LNA gain shall be kept in either high or low gain mode this has to be accomplished by tying the **THRES** pin to a fixed voltage. In order to achieve high gain mode operation, a voltage higher than 2.8V shall be applied to the **THRES** pin, such as a short to the **3VOLT** pin. In order to achieve low gain mode operation a voltage lower than 0.7V shall be applied to the **THRES**, such as a short to ground.

As stated above the capacitor connected to the **TAGC** pin is generating the gain control voltage of the LNA due to the charging and discharging currents of the OTA and thus is also responsible for the AGC time constant. As the charging and discharging currents are not equal two different time constants will result. The time constant corresponding to the charging process of the capacitor shall be chosen according to the data rate. According to measurements performed at Infineon the capacitor value should be greater than 47nF.

1. note the 20kΩ resistor in series with the 3.1V internal voltage source

## 4.2 Data Filter Design

Utilising the on-board voltage follower and the two 100kΩ on-chip resistors a 2nd order Sallen-Key low pass data filter can be constructed by adding 2 external capacitors between pins 19 (SLP) and 22 (FFB) and to pin 21 (OPP) as depicted in the following figure and described in the following formulas<sup>1</sup>.



Filter\_Design.wmf

Figure 4-3 Data Filter Design

(1)(2)

$$C_1 = \frac{2Q\sqrt{b}}{R^2\Pi f_{3dB}} \quad C_2 = \frac{\sqrt{b}}{4QR\Pi f_{3dB}}$$

with

$$Q = \frac{\sqrt{b}}{a} \quad (3) \text{the quality factor of the poles}$$

where

in case of a Bessel filter  $a = 1.3617$ ,  $b = 0.618$

and thus  $Q = 0.577$

and in case of a Butterworth filter  $a = 1.414$ ,  $b = 1$

and thus  $Q = 0.71$

Example: Butterworth filter with  $f_{3dB} = 5\text{kHz}$  and  $R = 100\text{k}\Omega$ :

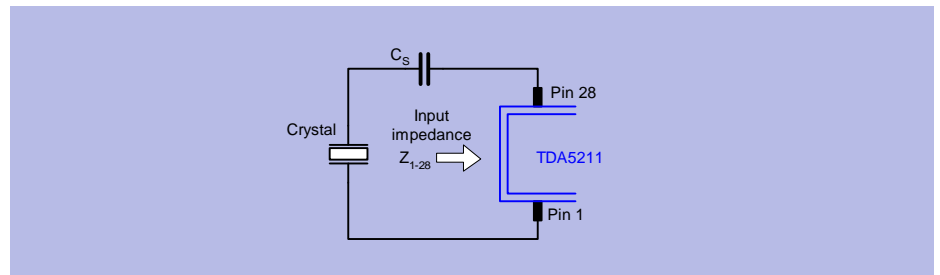
$$C_1 = 450\text{pF}, C_2 = 225\text{pF}$$

1. taken from Tietze/Schenk: Halbleiterschaltungstechnik, Springer Berlin, 1999



### 4.3 Quartz Load Capacitance Calculation

The value of the capacitor necessary to achieve that the quartz oscillator is operating at the intended frequency is determined by the reactive part of the negative resistance of the oscillator circuit as shown in Section 5.1.3 and by the quartz specifications given by the quartz manufacturer.



Quartz\_load\_5211.wmf

Figure 4-4 Determination of Series Capacitance Value for the Quartz Oscillator

Crystal specified with load capacitance

$$C_s = \frac{1}{\frac{1}{C_l} + 2\pi f X_L}$$

with  $C_l$  the load capacitance (refer to the quartz crystal specification).

Example:

$$10.18 \text{ MHz: } C_L = 12 \text{ pF} \quad X_L = 870 \text{ } \Omega \quad C_S = 7.2 \text{ pF}$$

This value may be obtained by putting two capacitors in series to the quartz, such as 18pF and 22pF in the 5.1MHz case and 18pF and 12pF in the 10.2MHz case.

## 4.4 Quartz Frequency Calculation

As described in Section 3.4.3 the operating range of the on-chip VCO is wide enough to guarantee a receive frequency range between 310 and 350MHz. The VCO signal is divided by 2 before applied to the mixer . This local oscillator signal can be used to downconvert the RF signals both with high- or low-side injection at the mixer. High-side injection of the local oscillator has to be used for receive frequencies between 310 and 330 MHz. In this case the local oscillator frequency is calculated by adding the IF frequency (10.7 MHz) to the RF frequency. In this case the higher frequency of a FSK-modulated signal is demodulated as a logical one (high).

Low-side injection has to be used for receive frequencies between 330 and 350 MHz. The local oscillator frequency is calculated by subtracting the IF frequency (10.7 MHz) from the RF frequency then. Please note that in this case sign-inversion occurs and the higher frequency of a FSK-modulated signal is demodulated as a logical zero (low). The overall division ratios in the PLL are 64 or 32 depending on whether the CSEL-pin is left open or tied to ground.

Therefore the quartz frequency may be calculated by using the following formula:

$$f_{QU} = (f_{RF} \pm 10.7) / r$$

with  $f_{RF}$  receive frequency

$f_{LO}$  local oscillator (PLL) frequency ( $f_{RF} \pm 10.7$ )

$f_{QU}$  quartz oscillator frequency

r ratio of local oscillator (PLL) frequency and quartz frequency as shown in the subsequent table

**Table 4-1 PLL Division Ratio Dependence on States of CSEL**

CSEL	Ratio r = ( $f_{LO}/f_{QU}$ )
open	64
GND	32

This yields the following examples:

CSEL tied to GND:

$$f_{QU} = (315\text{ MHz} + 10.7\text{ MHz}) / 32 = 10.1781\text{ MHz}$$

$$f_{QU} = (345\text{ MHz} - 10.7\text{ MHz}) / 32 = 10.4469\text{ MHz}$$

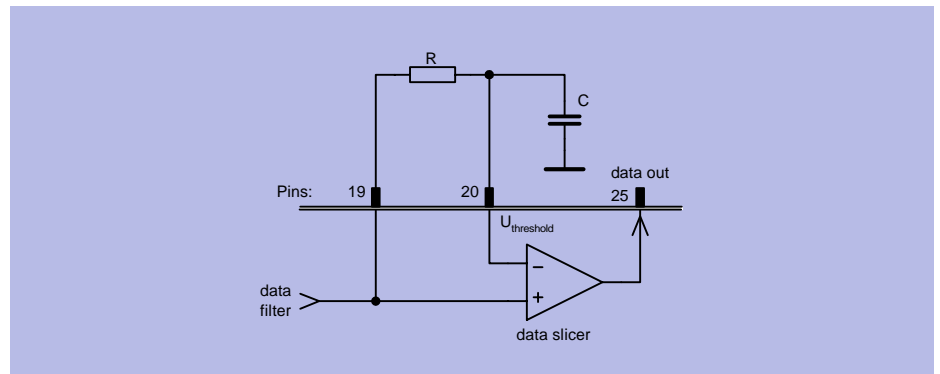
CSEL open:

$$f_{QU} = (315\text{ MHz} + 10.7\text{ MHz}) / 64 = 5.0891\text{ MHz}$$

$$f_{QU} = (345\text{ MHz} - 10.7\text{ MHz}) / 64 = 5.2234\text{ MHz}$$

## 4.5 Data Slicer Threshold Generation

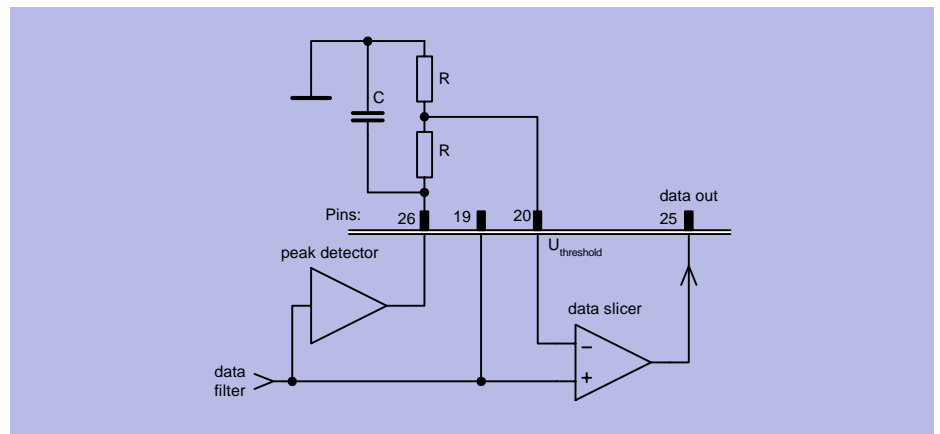
The threshold of the data slicer can be generated using an external R-C integrator as shown in Figure 4-5. The cut-off frequency of the R-C integrator has to be lower than the lowest frequency appearing in the data signal. In order to keep distortion low, the minimum value for R is 20kΩ.



Data\_slice1.wmf

Figure 4-5 Data Slicer Threshold Generation with External R-C Integrator

In case of ASK operation another possibility for threshold generation is to use the peak detector in connection with two resistors and one capacitor as shown in the following figure. The component values are depending on the coding scheme and the protocol used.



Data\_slice2.wmf

Figure 4-6 Data Slicer Threshold Generation Utilising the Peak Detector

## 4.6 ASK/FSK Switch Functional Description

The TDA5211 is containing an ASK/FSK switch which can be controlled via Pin 15 (MSEL). This switch is actually consisting of 2 operational amplifiers that are having a gain of 1 in case of the ASK amplifier and a gain of 11 in case of the FSK amplifier in order to achieve an appropriate demodulation gain characteristic. In order to compensate for the DC-offset generated especially in case of the FSK PLL demodulator there is a feedback connection between the threshold voltage of the bit slicer comparator (Pin 20) to the negative input of the FSK switch amplifier. This is shown in the following figure.

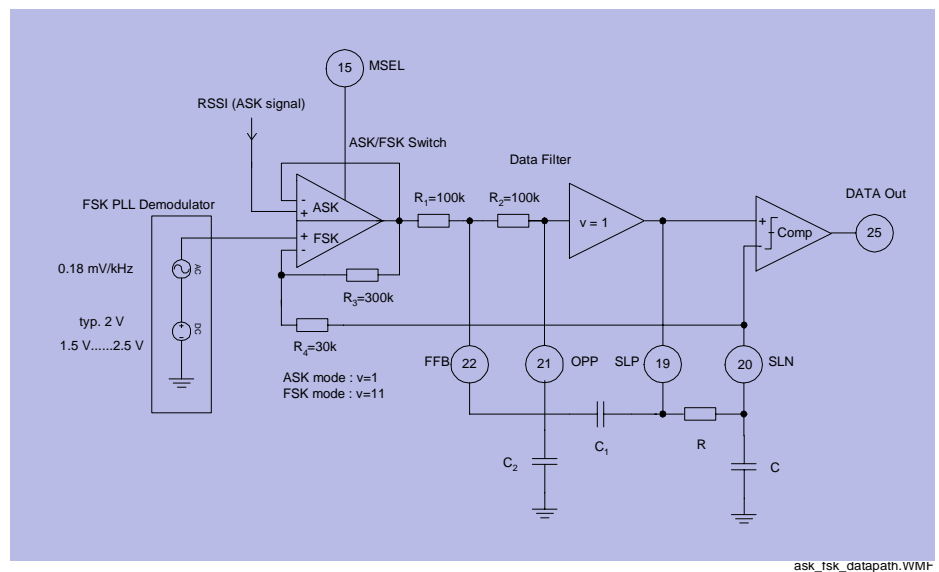


Figure 4-7 ASK/FSK mode datapath

### 4.6.1 FSK Mode

The FSK datapath has a bandpass characteristic due to the feedback shown above (highpass) and the data filter (lowpass). The lower cutoff frequency  $f_2$  is determined by the external RC-combination. The upper cutoff frequency  $f_3$  is determined by the data filter bandwidth.

The demodulation gain of the FSK PLL demodulator is  $140\mu\text{V}/\text{kHz}$ . This gain is increased by the gain  $v$  of the FSK switch, which is 11. Therefore the resulting dynamic gain of this circuit is  $1.5\text{mV}/\text{kHz}$  within the bandpass. The gain for the DC content of FSK signal remains at  $140\mu\text{V}/\text{kHz}$ . The cutoff frequencies of the bandpass have to be chosen such that the spectrum of the data signal is influenced in an acceptable amount.

In case that the user data is containing long sequences of logical zeroes the effect of the drift-off of the bit slicer threshold voltage can be lowered if the offset voltage inherent at the negative input of the slicer comparator (Pin 20) is used. The comparator has no hysteresis built in.

This offset voltage is generated by the bias current of the negative input of the comparator (i.e. 20nA) running over the external resistor R. This voltage raises the voltage appearing at pin 20 (e.g. 1mV with R = 100kΩ). In order to obtain benefit of this asymmetrical offset for the demodulation of long zeros the lower of the two FSK frequencies should be chosen in the transmitter as the zero-symbol frequency.

In the following figure the shape of the above mentioned bandpass is shown.

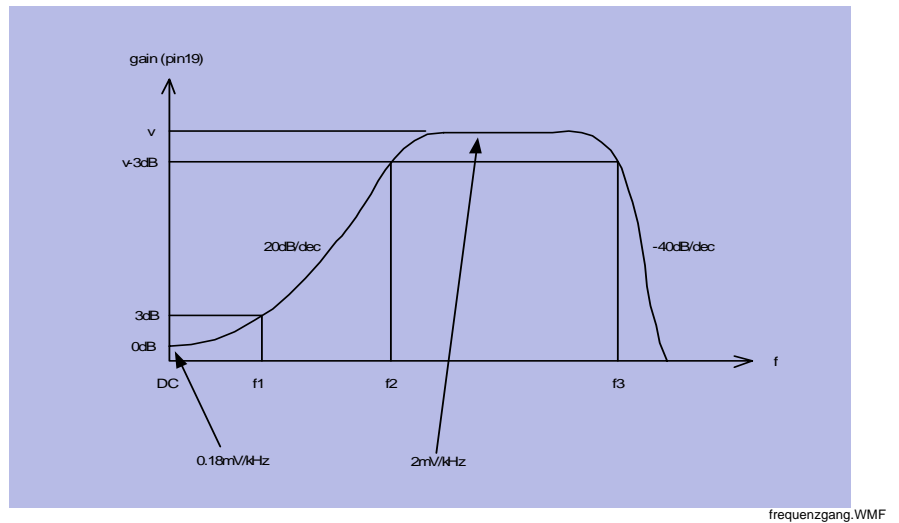


Figure 4-8 Frequency characteristic in case of FSK mode

The cutoff frequencies are calculated with the following formulas:

$$f_1 = \frac{1}{2\pi \frac{R \cdot 330k\Omega}{R + 330k\Omega} \cdot C}$$

$$f_2 = v \cdot f_1 = 11 \cdot f_1$$

$$f_3 = f_{3dB}$$

$f_3$  is the 3dB cutoff frequency of the data filter - see Section 4.2.

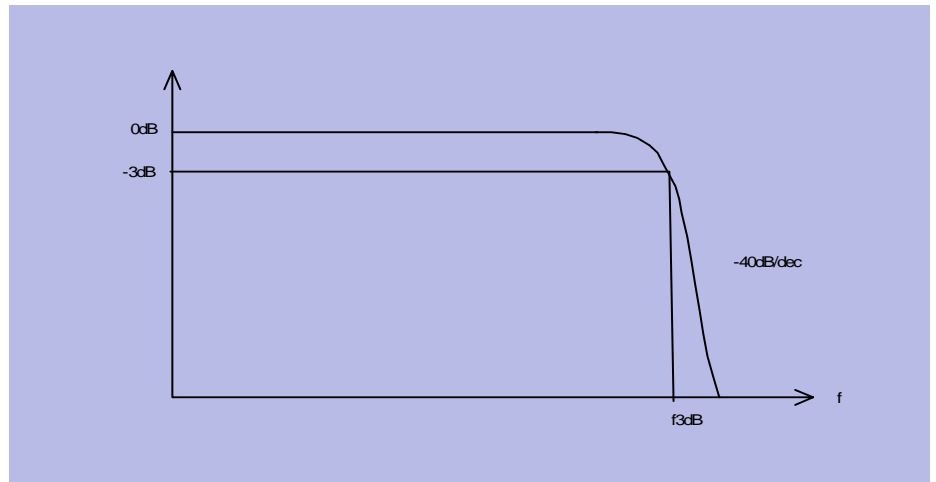
Example:

$R = 100k\Omega$ ,  $C = 47nF$

This leads to  $f_1 = 44Hz$  and  $f_2 = 485Hz$

### 4.6.2 ASK Mode

In case the receiver is operated in ASK mode the datapath frequency characteristic is dominated by the data filter alone, thus it is lowpass shaped. The cutoff frequency is determined by the external capacitors C12 and C14 and the internal 100k resistors as described in Section 4.2



freq\_ask.WMF

Figure 4-9 Frequency characteristic in case of ASK mode



This circuit charges the capacitor C with an inrush current  $I_{load}$  of typically  $220\mu A$  for a duration of  $T_2$  until the voltage  $U_c$  appearing on the capacitor is equal to the voltage  $U_s$  at the input of the data filter. This voltage is limited to 2.5V. As soon as these voltages are equal or the duration  $T_2$  is exceeded the precharge circuit is disabled.

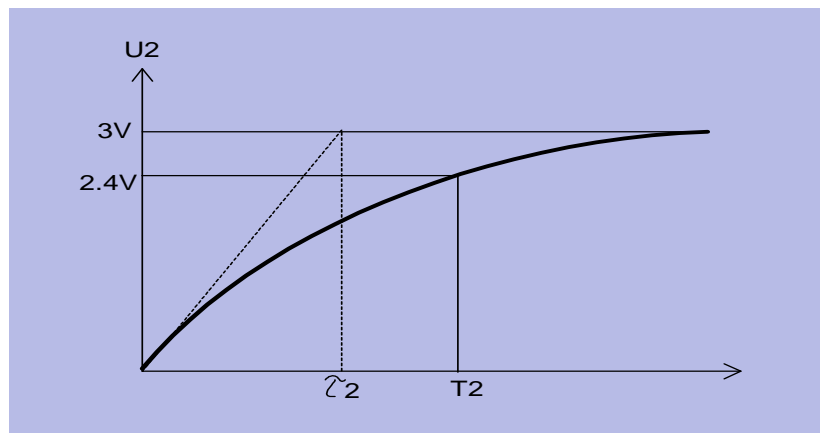
$\tau_2$  is the time constant of the charging process of C which can be calculated as

$$\tau_2 \approx 20k\Omega \cdot C2$$

as the sum of R1 and R2 is sufficiently large and thus can be neglected.  $T_2$  can then be calculated according to the following formula:

$$T_2 = \tau_2 \ln \left( \frac{1}{1 - \frac{2.4V}{3V}} \right) \approx \tau_2 \cdot 1.6$$

The voltage transient during the charging of C2 is shown in the following figure:



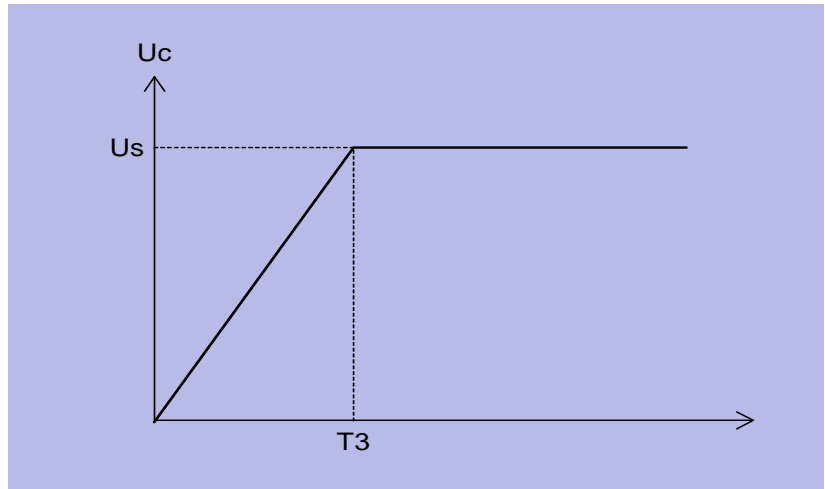
e-fkt1.WMF

Figure 4-11 Voltage appearing on C2 during precharging process

The voltage appearing on the capacitor C connected to pin 20 is shown in the following figure. It can be seen that due to the fact that it is charged by a constant current source it exhibits a linear increase in voltage which is limited to  $U_{Smax} = 2.5V$  which is also the approximate operating point of the data filter input. The time constant appearing in this case can be denoted as  $T_3$ , which can be calculated with

$$T_3 = \frac{U_{Smax} \cdot C}{220\mu A} = \frac{2.5V}{220\mu A} \cdot C$$





e-Fkt2.WMF

Figure 4-12 Voltage transient on capacitor C attached to pin 20

As an example the choice of  $C_2 = 22\text{nF}$  and  $C = 47\text{nF}$  yields

$$\tau_2 = 0.44\text{ms}$$

$$T_2 = 0.71\text{ms}$$

$$T_3 = 0.53\text{ms}$$

This means that in this case the inrush current could flow for a duration of  $0.64\text{ms}$  but stops already after  $0.49\text{ms}$  when the  $U_{S\text{max}}$  limit has been reached.  $T_3$  should always be chosen to be shorter than  $T_2$ .

It has to be noted finally that during the turn-on duration  $T_2$  the overall device power consumption is increased by the  $220\mu\text{A}$  needed to charge C.

The precharge circuit may be disabled if  $C_2$  is not equipped. This yields a  $T_2$  close to zero. Note that the sum of  $R_4$  and  $R_5$  has to be  $600\text{k}\Omega$  in order to produce  $3\text{V}$  at the THRES pin as this voltage is internally used also as the reference for the FSK demodulator.

# 5 Reference

## Contents of this Chapter

5.1	Electrical Data . . . . .	5-2
5.2	Test Circuit . . . . .	5-11
5.3	Test Board Layouts . . . . .	5-12
5.4	Bill of Materials . . . . .	5-14

## 5.1 Electrical Data

### 5.1.1 Absolute Maximum Ratings



#### WARNING

The maximum ratings may not be exceeded under any circumstances, not even momentarily and individually, as permanent damage to the IC will result.

Table 5-1 Absolute Maximum Ratings, Ambient temperature  $T_{AMB} = -40^{\circ}\text{C} \dots +105^{\circ}\text{C}$

#	Parameter	Symbol	Limit Values		Unit	Remarks
			min	max		
1	Supply Voltage	$V_s$	-0.3	5.5	V	
2	Junction Temperature	$T_j$	-40	+150	$^{\circ}\text{C}$	
3	Storage Temperature	$T_s$	-40	+125	$^{\circ}\text{C}$	
4	Thermal Resistance	$R_{thJA}$		114	K/W	
5	ESD integrity, all pins excl. Pins 1,3, 6, 28 ESD integrity Pins 1,3,6,28	$V_{ESD}$		+2 +1.5	kV kV	HBM according to MIL STD 883D, method 3015.7

## 5.1.2 Operating Range

Within the operational range the IC operates as explained in the circuit description. The AC/DC characteristic limits are not guaranteed. Currents flowing into the device are denoted as positive currents and v.v.

Supply voltage:  $V_{CC} = 4.5V \dots 5.5V$

**Table 5-2 Operating Range, Ambient temperature  $T_{AMB} = -40^{\circ}C \dots +105^{\circ}C$**

#	Parameter	Symbol	Limit Values		Unit	Test Conditions	L	Item
			min	max				
1	Supply Current	$I_{SF}$	3.9	7.5	mA	$f_{RF} = 315MHz$ , FSK Mode		
		$I_{SA}$	3.2	6.8	mA	$f_{RF} = 315MHz$ , ASK Mode		
2	Receiver Input Level ASK FSK, frequ. dev. $\pm 50kHz$	$RF_{in}$	-110 -102	-13 -13	dBm dBm	@ source impedance $50\Omega$ , BER 2E-3, average power level, Manchester encoded datarate 4kBit, 280kHz IF Bandwidth	■	
3	LNI Input Frequency	$f_{RF}$	310	350	MHz			
4	MI/X Input Frequency	$f_{MI}$	310	350	MHz			
5	3dB IF Frequency Range ASK FSK	$f_{IF -3dB}$	5 10.4	23 11	MHz		■	
6	Powerdown Mode On	$PWDN_{ON}$	0	0.8	V			
7	Powerdown Mode Off	$PWDN_{OFF}$	2	$V_S$	V			
8	Gain Control Voltage, LNA high gain state	$V_{THRES}$	2.8	$V_S$	V			
9	Gain Control Voltage, LNA low gain state	$V_{THRES}$	0	0.7	V			

■ This value is guaranteed by design.

### 5.1.3 AC/DC Characteristics at $T_{AMB} = 25^{\circ}\text{C}$

AC/DC characteristics involve the spread of values guaranteed within the specified voltage and ambient temperature range. Typical characteristics are the median of the production. Currents flowing into the device are denoted as positive currents and vice versa.

The device performance parameters marked with ■ were measured on an Infineon evaluation board as described in Section 5.2.

**Table 5-3 AC/DC Characteristics with  $T_A = 25^{\circ}\text{C}$ ,  $V_{VCC} = 4.5 \dots 5.5 \text{ V}$** 

	Parameter	Symbol	Limit Values			Unit	Test Conditions	L	Item
			min	typ	max				
<b>Supply</b>									
<b>Supply Current</b>									
1	Supply current, standby mode	$I_{S\text{ PDWN}}$		50	100	nA	Pin 27 (PDWN) open or tied to 0 V		
2	Supply current, device operating in FSK mode	$I_{SF}$	4.9	5.7	6.5	mA	Pin 11 (FSEL) open, Pin 15 (MSEL) tied to GND		
3	Supply current, device operating in ASK mode	$I_{SA}$	4.2	5	5.8	mA	Pin 11 (FSEL) open, Pin 15 (MSEL) open		
<b>LNA</b>									
<b>Signal Input LNI (PIN 3), <math>V_{THRES} &gt; 2.8\text{V}</math>, high gain mode</b>									
1	Average Power Level at BER = 2E-3 (Sensitivity)	$RF_{in}$		-113		dBm	Manchester encoded datarate 4kBit, 280kHz IF Bandwidth	■	
2	Average Power Level at BER = 2E-3 (Sensitivity) FSK	$RF_{in}$		-105		dBm	Manchester enc. datarate 4kBit, 280kHz IF Bandw., $\pm 50\text{kHz}$ pk. dev.	■	
3	Input impedance, $f_{RF} = 315 \text{ MHz}$	$S_{11\text{ LNA}}$	0.895 / -25.5 deg					■	
4	Input level @ 1dB C.P. $f_{RF}=315 \text{ MHz}$	$P_{1dB\text{ LNA}}$		-14		dBm		■	
5	Input 3 <sup>rd</sup> order intercept point $f_{RF} = 315 \text{ MHz}$	$IIP3\text{ LNA}$		-10		dBm	$f_{in} = 315 \text{ \& } 317\text{MHz}$	■	
6	LO signal feedthrough at antenna port	$LO_{LNI}$		-119		dBm		■	
<b>Signal Output LNO (PIN 6), <math>V_{THRES} &gt; 2.8\text{V}</math>, high gain mode</b>									
1	Gain $f_{RF} = 315 \text{ MHz}$	$S_{21\text{ LNA}}$	1.577 / 150.3 deg					■	
2	Output impedance, $f_{RF} = 315 \text{ MHz}$	$S_{22\text{ LNA}}$	0.897 / -10.3 deg					■	

**Table 5-3 AC/DC Characteristics with  $T_A = 25\text{ }^\circ\text{C}$ ,  $V_{CC} = 4.5 \dots 5.5\text{ V}$  (continued)**

	Parameter	Symbol	Limit Values			Unit	Test Conditions	L	Item
			min	typ	max				
3	Voltage Gain Antenna to MI $f_{RF} = 315\text{ MHz}$	$G_{AntMI}$		21		dB		■	
4	Noise Figure	$NF_{LNA}$		2		dB	excluding matching network loss - see Appendix	■	

**Signal Input LNI,  $V_{THRES} = GND$ , low gain mode**

1	Input impedance, $f_{RF} = 315\text{ MHz}$	$S_{11\text{ LNA}}$	0.918 / -25.2 deg					■	
2	Input level @ 1dB C. P. $f_{RF} = 315\text{ MHz}$	$P1dB_{LNA}$		-7		dBm	matched input	■	
3	Input 3 <sup>rd</sup> order intercept point $f_{RF} = 315\text{ MHz}$	$IIP3_{LNA}$		-13		dBm	$f_{in} = 315 \text{ \& } 317\text{ MHz}$	■	

**Signal Output LNO,  $V_{THRES} = GND$ , low gain mode**

1	Gain $f_{RF} = 315\text{ MHz}$	$S_{21\text{ LNA}}$	0.193 / 153.7 deg					■	
2	Output impedance, $f_{RF} = 315\text{ MHz}$	$S_{22\text{ LNA}}$	0.907 / -10.5 deg					■	
3	Voltage Gain Antenna to MI $f_{RF} = 315\text{ MHz}$	$G_{AntMI}$		2		dB		■	

**Signal 3VOUT (PIN 24)**

1	Output voltage	$V_{3VOUT}$	2.9	3.1	3.3	V	3VOUT Pin open		
2	Current out	$I_{3VOUT}$	-3	-5	-10	$\mu\text{A}$	see Section 4.1		

**Signal THRES (PIN 23)**

1	Input Voltage range	$V_{THRES}$	0		$V_S$	V	see Section 4.1		
2	LNA low gain mode	$V_{THRES}$	0		0.3	V			
3	LNA high gain mode	$V_{THRES}$	3.3		$V_S$	V	or shorted to VCC		
4	Current in	$I_{THRES\_in}$		5		nA			

**Signal TAGC (PIN 4)**

1	Current out, LNA low gain state	$I_{TAGC\_out}$	-3.6	-4.2	-5	$\mu\text{A}$	$RSSI > V_{THRES}$		
2	Current in, LNA high gain state	$I_{TAGC\_in}$	1	1.6	2.2	$\mu\text{A}$	$RSSI < V_{THRES}$		

**MIXER**
**Signal Input MI/MIX (PINS 8/9)**

1	Input impedance, $f_{RF} = 315\text{ MHz}$	$S_{11\text{ MIX}}$	0.954 / -10.9 deg					■	
2	Input 3 <sup>rd</sup> order intercept point	$IIP3_{MIX}$		-25		dBm		■	

**Table 5-3 AC/DC Characteristics with  $T_A$  25 °C,  $V_{CC} = 4.5 \dots 5.5$  V (continued)**

	Parameter	Symbol	Limit Values			Unit	Test Conditions	L	Item
			min	typ	max				
<b>Signal Output IFO (PIN 12)</b>									
1	Output impedance	$Z_{IFO}$		330		$\Omega$		■	
2	Conversion Voltage Gain $f_{RF} = 315$ MHz	$G_{MIX}$		21		dB		■	
3	Noise Figure, SSB (~DSB NF+3dB)	$NF_{MIX}$		13		dB		■	
4	RF to IF isolation	$A_{RF-IF}$		46		dB		■	

**LIMITER**
**Signal Input LIM/X (PINS 17/18)**

1	Input Impedance	$Z_{LIM}$	264	330	396	$\Omega$		■	
2	RSSI dynamic range	$DR_{RSSI}$	60		80	dB			
3	RSSI linearity	$LIN_{RSSI}$		$\pm 1$		dB		■	
4	Operating frequency (3dB points)	$f_{LIM}$	5	10.7	23	MHz		■	

**DATA FILTER**

1	Useable bandwidth	$BW_{BB\ FILT}$			100	kHz		■	
2	RSSI Level at Data Filter Output SLP, $RF_{IN} = -103$ dBm	$RSSI_{low}$	0.3		1	V	LNA in high gain mode		
3	RSSI Level at Data Filter Output SLP, $RF_{IN} = -30$ dBm	$RSSI_{high}$	1.8		3	V	LNA in high gain mode		

**SLICER**
**Signal Output DATA (PIN 25)**

1	Maximum Datarate	$DR_{max}$			100	kBps	NRZ, 20pF capacitive loading	■	
2	LOW output voltage	$V_{SLIC\_L}$	0		0.1	V			
3	HIGH output voltage	$V_{SLIC\_H}$	$V_S - 1.3V$	$V_S - 1V$	$V_S - 0.7V$	V			

**Slicer, Signal Output DATA (PIN 20)**

1	Precharge Current Out	$I_{PCH\_SLN}$	-100	-220	-300	$\mu A$	see Section 4.7		
---	-----------------------	----------------	------	------	------	---------	-----------------	--	--

**Table 5-3 AC/DC Characteristics with  $T_A = 25\text{ }^\circ\text{C}$ ,  $V_{CC} = 4.5 \dots 5.5\text{ V}$  (continued)**

	Parameter	Symbol	Limit Values			Unit	Test Conditions	L	Item
			min	typ	max				
<b>PEAK DETECTOR</b>									
<b>Signal Output PDO (PIN 26)</b>									
1	Load current	$I_{load}$	-600	-950	-1300	$\mu\text{A}$			
2	Leakage current	$I_{leakage}$	0	200	1000	nA			
<b>CRYSTAL OSCILLATOR</b>									
<b>Signals CRSTL1, CRISTL 2, (PINS 1/28)</b>									
1	Operating frequency	$f_{CRSTL}$	5		11	MHz	fundamental mode, series resonance		
2	Input Impedance @ ~5MHz	$Z_{1-28}$		-850 + j 625		$\Omega$		■	
3	Input Impedance @ ~10MHz	$Z_{1-28}$		-700 + j 865		$\Omega$		■	
4	Serial Capacity @ ~5MHz	$C_{S5=C1}$		9.7		pF			
5	Serial Capacity @ ~10MHz	$C_{S10=C1}$		7.2		pF			
<b>ASK/FSK Signal Switch</b>									
<b>Signal MSEL (PIN 15)</b>									
1	ASK Mode	$V_{MSEL}$	1.4		4	V	or open		
2	FSK Mode	$V_{MSEL}$	0		0.2	V	or tied to ground		
<b>FSK DEMODULATOR</b>									
1	Demodulation Gain	$G_{FMDEM}$	85	140	225	$\mu\text{V}/\text{kHz}$			
2	Useable IF Bandwidth	$BW_{IFPLL}$	10.2	10.7	11.2	MHz			
<b>POWER DOWN MODE</b>									
<b>Signal PDWN (PIN 27)</b>									
1	Powerdown Mode On	$PWDN_{ON}$	0		0.8	V			
2	Powerdown Mode Off	$PWDN_{Off}$	2.8		$V_S$	V			
3	Input bias current PDWN	$I_{PDWN}$		19		$\mu\text{A}$	Power On Mode		
4	Start-up Time until valid IF signal is detected	$T_{SU}$			1	ms			



**Table 5-3 AC/DC Characteristics with  $T_A$  25 °C,  $V_{CC} = 4.5 \dots 5.5$  V (continued)**

	Parameter	Symbol	Limit Values			Unit	Test Conditions	L	Item
			min	typ	max				
<b>PLL DIVIDER</b>									
<b>Signal CSEL (PIN 16)</b>									
1	$f_{CRSTL}$ range 5.xxMHz	$V_{CSEL}$	1.4		4	V	or open		
2	$f_{CRSTL}$ range 10.xxMHz	$V_{CSEL}$	0		0.2	V			
3	Input bias current CSEL	$I_{CSEL}$	-3	-5	-7	$\mu$ A	CSEL tied to GND		

■ Measured only in lab.

### 5.1.4 AC/DC Characteristics at $T_{AMB} = -40$ to $105^{\circ}\text{C}$

Currents flowing into the device are denoted as positive currents and vice versa.

**Table 5-4 AC/DC Characteristics with  $T_{AMB} = -40^{\circ}\text{C} \dots +105^{\circ}\text{C}$ ,  $V_{VCC} = 4.5 \dots 5.5 \text{ V}$** 

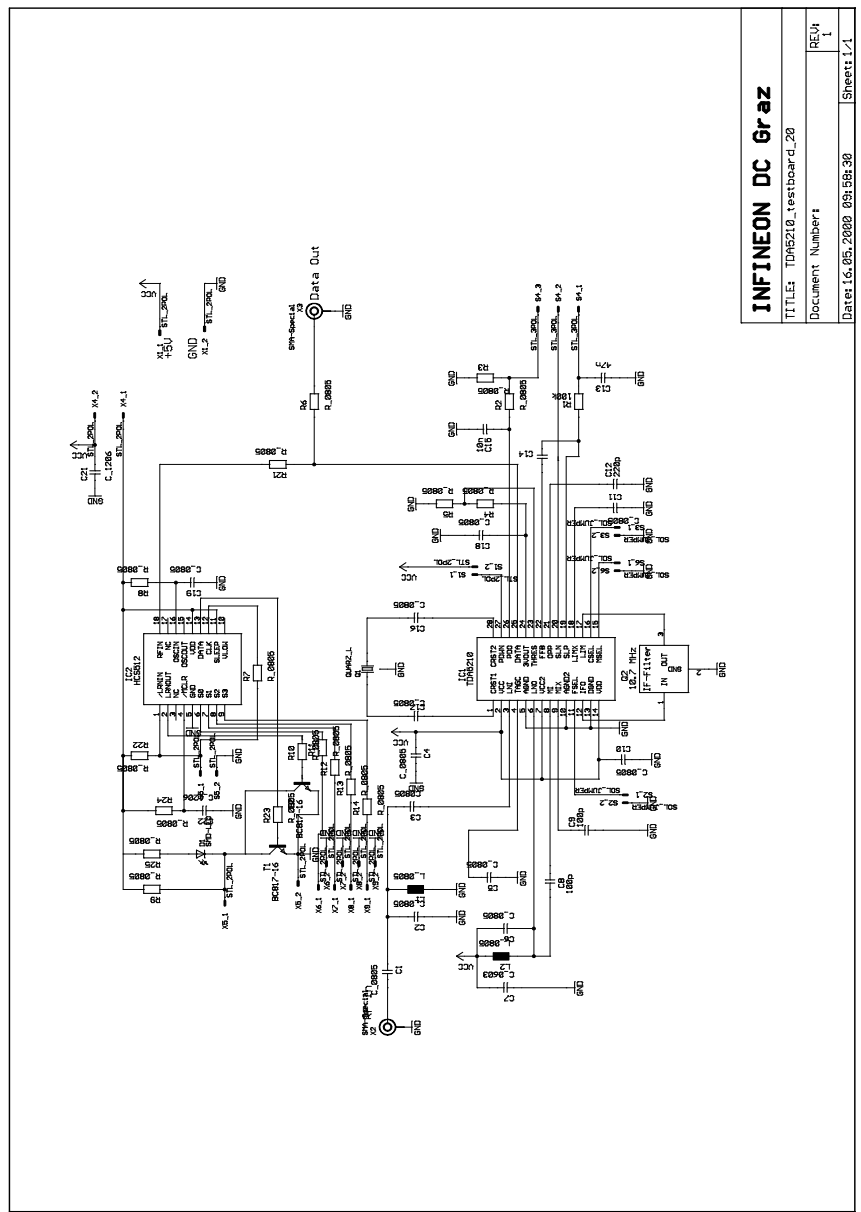
	Parameter	Symbol	Limit Values			Unit	Test Conditions	L	Item
			min	typ	max				
<b>Supply</b>									
<b>Supply Current</b>									
1	Supply current, standby mode	$I_{S\text{PDWN}}$		50	400	nA	Pin 27 (PDWN) open or tied to 0 V		
2	Supply current, device operating in FSK mode	$I_{SF}$	3.9	5.7	7.5	mA	Pin 11 (FSEL) tied to GND, Pin 15 (MSEL) tied to GND		
3	Supply current, device operating in ASK mode	$I_{SA}$	3.2	5	6.8	mA	Pin 11 (FSEL) open, Pin 15 (MSEL) open		
<b>Signal 3VOUT (PIN 24)</b>									
1	Output voltage	$V_{3\text{VOUT}}$	2.9	3.1	3.3	V	3VOUT Pin open		
2	Current out	$I_{3\text{VOUT}}$	-3	-5	-10	$\mu\text{A}$	see Section 4.1		
<b>Signal THRES (PIN 23)</b>									
1	Input Voltage range	$V_{\text{THRES}}$	0		$V_S - 1\text{V}$	V	see Section 4.1		
2	LNA low gain mode	$V_{\text{THRES}}$	0		0.3	V			
3	LNA high gain mode	$V_{\text{THRES}}$	3		$V_S$	V	or shorted to Pin 24		
4	Current in	$I_{\text{THRES\_in}}$		5		nA			
<b>Signal TAGC (PIN 4)</b>									
1	Current out, LNA low gain state	$I_{\text{TAGC\_out}}$	-1	-4.2	-8	$\mu\text{A}$	$\text{RSSI} > V_{\text{THRES}}$		
2	Current in, LNA high gain state	$V_{\text{TAGC\_in}}$	0.5	1.5	5	$\mu\text{A}$	$\text{RSSI} < V_{\text{THRES}}$		
<b>MIXER</b>									
1	Conversion Voltage Gain $f_{RF} = 315 \text{ MHz}$	$G_{\text{MIX}}$		+19		dB			
<b>LIMITER</b>									
<b>Signal Input LIM/X (PINS 17/18)</b>									
1	RSSI dynamic range	$\text{DR}_{\text{RSSI}}$	60		80	dB			
2	RSSI Level at Data Filter Output SLP, $\text{RF}_{\text{IN}} = -103\text{dBm}$	$\text{RSSI}_{\text{low}}$	0.3		1	V	LNA in high gain mode		
3	RSSI Level at Data Filter Output SLP, $\text{RF}_{\text{IN}} = -30\text{dBm}$	$\text{RSSI}_{\text{high}}$	1.8		3	V	LNA in high gain mode		

**Table 5-4 AC/DC Characteristics with  $T_{AMB} = -40^{\circ}\text{C} \dots +105^{\circ}\text{C}$ ,  $V_{VCC} = 4.5 \dots 5.5 \text{ V}$** 

	Parameter	Symbol	Limit Values			Unit	Test Conditions	L	Item
			min	typ	max				
<b>DATA FILTER</b>									
<b>Slicer, Signal Output DATA (PIN 25)</b>									
1	Maximum Datarate	$DR_{max}$			100	kBps	NRZ, 20pF capacitive loading	■	
2	LOW output voltage	$V_{SLIC\_L}$	0		0.1	V			
3	HIGH output voltage	$V_{SLIC\_H}$	$V_S - 1.5\text{V}$	$V_S - 1\text{V}$	$V_S - 0.5\text{V}$	V			
<b>Slicer, Signal Output DATA (PIN 20)</b>									
1	Precharge Current Out	$I_{PCH\_SLN}$	-100	-220	-300	$\mu\text{A}$	see Section 4.7		
<b>PEAK DETECTOR</b>									
<b>Signal Output PDO (PIN 26)</b>									
1	Load current	$I_{load}$	-400	-850	-1400	$\mu\text{A}$			
2	Leakage current	$I_{leakage}$	0	700	2000	nA			
<b>CRYSTAL OSCILLATOR</b>									
<b>Signals CRSTL1, CRSTL 2, (PINS 1/28)</b>									
1	Operating frequency	$f_{CRSTL}$	5		11	MHz	fundamental mode, series resonance		
<b>ASK/FSK Signal Switch</b>									
<b>Signal MSEL (PIN 15)</b>									
1	ASK Mode	$V_{MSEL}$	1.4		4	V	or open		
2	FSK Mode	$V_{MSEL}$	0		0.2	V			
<b>FSK DEMODULATOR</b>									
1	Demodulation Gain	$G_{FMDEM}$	105	140	245	$\mu\text{V}/\text{kHz}$			
2	Useable IF Bandwidth	$BW_{IFPLL}$	10.4	10.7	11	MHz			
<b>POWER DOWN MODE</b>									
<b>Signal PDWN (PIN 27)</b>									
1	Powerdown Mode On	$PWDN_{ON}$	0		0.8	V			
2	Powerdown Mode Off	$PWDN_{Off}$	2.8		$V_S$	V			
3	Start-up Time until valid signal is detected at IF	$T_{SU}$			1	ms			
<b>PLL DIVIDER</b>									
<b>Signal CSEL (PIN 16)</b>									
1	$f_{CRSTL}$ range 5.xxMHz	$V_{CSEL}$	1.4		4	V	or open		
2	$f_{CRSTL}$ range 10.xxMHz	$V_{CSEL}$	0		0.2	V			
3	Input bias current CSEL	$I_{CSEL}$	-3	-5	-7	$\mu\text{A}$	CSEL tied to GND		

## 5.2 Test Circuit

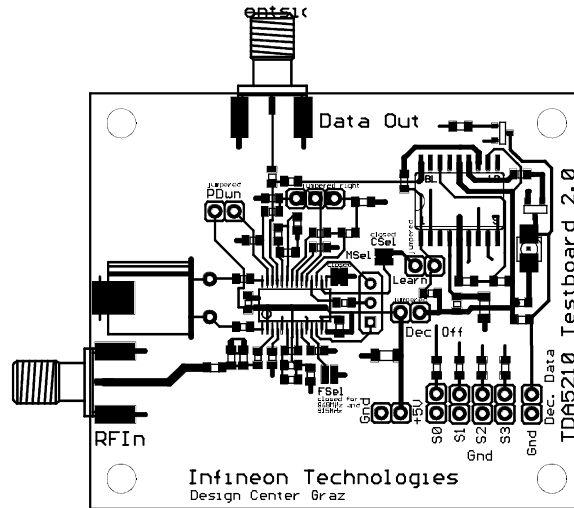
The device performance parameters marked with ■ in Section 5.1.3 were measured on an Infineon evaluation board. This evaluation board can be obtained together with evaluation boards of the accompanying transmitter device TDA5101 in an evaluation kit that may be ordered on the INFINEON RKE Webpage [www.infineon.com/rke](http://www.infineon.com/rke). In case a matching codeword is received, decoded and accepted by the decoder the on-board LED will turn on. This signal is also accessible on a 2-pole pin connector and can be used for simple remote-control applications. More information on the kit is available on request.



TDA521x\_testboard\_20\_schematic.WMF

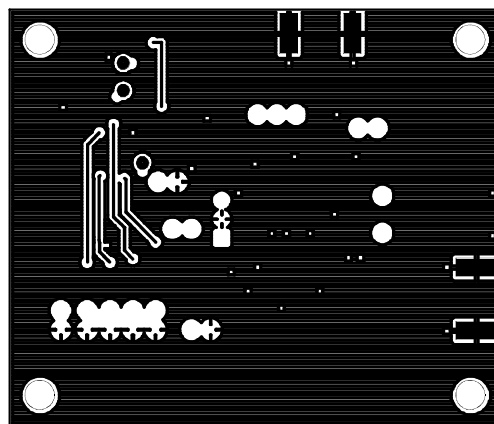
Figure 5-1 Schematic of the Evaluation Board

### 5.3 Test Board Layouts



tda521x\_testboard\_20\_top.WMF

Figure 5-2 Top Side of the Evaluation Board



tda521x\_testboard\_20\_bot.WMF

Figure 5-3 Bottom Side of the Evaluation Board



## 5.4 Bill of Materials

The following components are necessary for evaluation of the TDA5211 at 315 MHz without use of a Microchip HCS512 decoder.

**Table 5-5 Bill of Materials**

Ref	Value	Specification
R1	100kΩ	0805, ± 5%
R2	100kΩ	0805, ± 5%
R3	820kΩ	0805, ± 5%
R4	240kΩ	0805, ± 5%
R5	360kΩ	0805, ± 5%
R6	10kΩ	0805, ± 5%
L1	15nH	Toko, PTL2012-F15N0G
L2	12pF	0805, COG, ± 2%
C1	3.3 pF	0805, COG, ± 0.1pF
C2	10pF	0805, COG, ± 0.1pF
C3	6.8pF	0805, COG, ± 0.1pF
C4	100pF	0805, COG, ± 5%
C5	47nF	1206, X7R, ± 10%
C6	15nH	Toko, PTL2012-F15N0G
C7	100pF	0805, COG, ± 5%
C8	33pF	0805, COG, ± 5%
C9	100pF	0805, COG, ± 5%
C10	10nF	0805, X7R, ± 10%
C11	10nF	0805, X7R, ± 10%
C12	220pF	0805, COG, ± 5%
C13	47nF	0805, X7R, ± 10%
C14	470pF	0805, COG, ± 5%
C15	47nF	0805, COG, ± 5%
C16	12pF	0805, COG, ± 1%
C17	18pF	0805, COG, ± 1%
C18	22nF	0805, X7R, ± 5%
Q1	$(315 + 10.7\text{MHz})/32$	HC49/U, fundamental mode, $C_L = 12\text{pF}$ , e.g. 315 MHz: Jauch Q 10,178130-S11-1017-12-10/20
Q2	SFE10.7MA5-A	Murata
X2, X3	142-0701-801	Johnson

S1-S3, S6 X1		2-pole pin connector
S4		3-pole pin connector, or not equipped
IC1	TDA 5211	Infineon

Please note that a capacitor has to be soldered in place L2 and an inductor in place C6.

The following components are necessary in addition to the above mentioned ones for evaluation of the TDA5211 in conjunction with a Microchip HCS512 decoder.

**Table 5-6 Bill of Materials Addendum**

Ref	Value	Specification
R7	100k $\Omega$	0805, $\pm$ 5%
R8	10k $\Omega$	0805, $\pm$ 5%
R9	100k $\Omega$	0805, $\pm$ 5%
R10	22k $\Omega$	0805, $\pm$ 5%
R11	100 $\Omega$	0805, $\pm$ 5%
R12	100 $\Omega$	0805, $\pm$ 5%
R13	100 $\Omega$	0805, $\pm$ 5%
R14	100 $\Omega$	0805, $\pm$ 5%
R21	22k $\Omega$	0805, $\pm$ 5%
R22	10k $\Omega$	0805, $\pm$ 5%
R23	22k $\Omega$	0805, $\pm$ 5%
R24	820k $\Omega$	0805, $\pm$ 5%
R25	560 $\Omega$	0805, $\pm$ 5%
C19	10pF	0805, COG, $\pm$ 5%
C21	100nF	1206, X7R, $\pm$ 10%
C22	100nF	1206, X7R, $\pm$ 10%
IC2	HCS512	Microchip
S5, X4-X9		2-pole pin connector
T1, T2	BC 847B	Infineon
D1	LS T670-JL	Infineon



## 5.5 Appendix - Noise Figure and Gain Circles

The following gain and noise figure circles were measured utilizing Microlab Stub Stretchers and a HP8514 network analyser. Maximum gain is shown at point 1 at 18.5 dB, minimum noise figure is 1.9dB at point 2, step size of circles is 0.5dB.

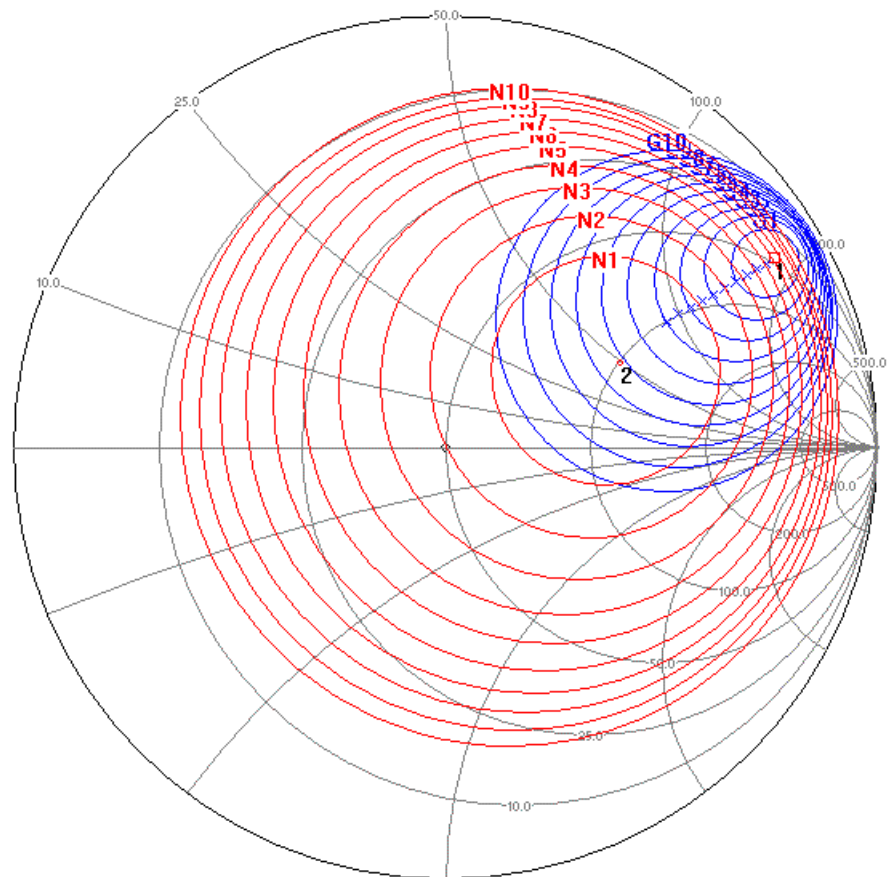


Figure 5-5 Gain and Noise Circles of the TDA5211 at 315 MHz.



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