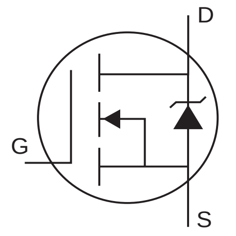
International
IOR Rectifier

PRELIMINARY

IRL3102S

HEXFET® Power MOSFET

- Advanced Process Technology
- Surface Mount
- Optimized for 4.5V-7.0V Gate Drive
- Ideal for CPU Core DC-DC Converters
- Fast Switching



V_{DSS} = 20V

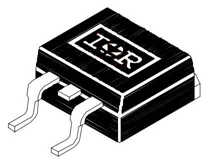
$R_{DS(on)}$ = 0.013Ω

I_D = 61A

Description

These HEXFET Power MOSFETs were designed specifically to meet the demands of CPU core DC-DC converters. Advanced processing techniques combined with an optimized gate oxide design results in a die sized specifically to offer maximum efficiency at minimum cost.

The D²Pak is a surface mount power package capable of accommodating die sizes up to HEX-4. It provides the highest power capability and the lowest possible on-resistance in any existing surface mount package. The D²Pak is suitable for high current applications because of its low internal connection resistance and can dissipate up to 2.0W in a typical surface mount application.



D²Pak

Absolute Maximum Ratings

	Parameter	Max.	Units
I_D @ T_C = 25°C	Continuous Drain Current, V_{GS} @ 4.5V⑤	61	A
I_D @ T_C = 100°C	Continuous Drain Current, V_{GS} @ 4.5V⑤	39	
I_{DM}	Pulsed Drain Current ①⑤	240	
P_D @T_C = 25°C	Power Dissipation	89	W
	Linear Derating Factor	0.71	W/°C
V_{GS}	Gate-to-Source Voltage	± 10	V
E_{AS}	Single Pulse Avalanche Energy②⑤	220	mJ
I_{AR}	Avalanche Current①	35	A
E_{AR}	Repetitive Avalanche Energy①	8.9	mJ
dv/dt	Peak Diode Recovery dv/dt ③⑤	5.0	V/ns
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to + 150	°C
	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	

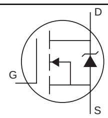
Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	——	1.4	°C/W
$R_{\theta JA}$	Junction-to-Ambient (PCB Mounted,steady-state)**	——	40	

Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	20	——	——	V	V_{GS} = 0V, I_D = 250µA
$DV_{(BR)DSS}/DT_J$	Breakdown Voltage Temp. Coefficient	——	0.016	——	V/°C	Reference to 25°C, I_D = 1mA⑤
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	——	——	0.015	W	V_{GS} = 4.5V, I_D = 37A ④
		——	——	0.013		V_{GS} = 7.0V, I_D = 37A ④
$V_{GS(th)}$	Gate Threshold Voltage	0.70	——	——	V	V_{DS} = V_{GS}, I_D = 250µA
g_{fs}	Forward Transconductance	36	——	——	S	V_{DS} = 16V, I_D = 35A⑤
I_{DSS}	Drain-to-Source Leakage Current	——	——	25	µA	V_{DS} = 20V, V_{GS} = 0V
		——	——	250		V_{DS} = 10V, V_{GS} = 0V, T_J = 150°C
I_{GSS}	Gate-to-Source Forward Leakage	——	——	100	nA	V_{GS} = 10V
	Gate-to-Source Reverse Leakage	——	——	-100		V_{GS} = -10V
Q_g	Total Gate Charge	——	——	58	nC	I_D = 35A
Q_{gs}	Gate-to-Source Charge	——	——	14		V_{DS} = 16V
Q_{gd}	Gate-to-Drain ("Miller") Charge	——	——	21		V_{GS} = 4.5V, See Fig. 6 ④⑤
$t_{d(on)}$	Turn-On Delay Time	——	10	——	ns	V_{DD} = 10V
t_r	Rise Time	——	130	——		I_D = 35A
$t_{d(off)}$	Turn-Off Delay Time	——	80	——		R_G = 9.0W, V_{GS} = 4.5V
t_f	Fall Time	——	110	——		R_D = 0.28W, ④⑤
L_S	Internal Source Inductance	——	7.5	——	nH	Between lead, and center of die contact
C_{iss}	Input Capacitance	——	2500	——	pF	V_{GS} = 0V
C_{oss}	Output Capacitance	——	1000	——		V_{DS} = 15V
C_{rss}	Reverse Transfer Capacitance	——	360	——		ƒ = 1.0MHz, See Fig. 5

Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	——	——	61	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I_{SM}	Pulsed Source Current (Body Diode) ①⑤	——	——	240		
V_{SD}	Diode Forward Voltage	——	——	1.3	V	T_J = 25°C, I_S = 37A, V_{GS} = 0V ④
t_{rr}	Reverse Recovery Time	——	59	88	ns	T_J = 25°C, I_F = 35A
Q_{rr}	Reverse Recovery Charge	——	110	160	nC	di/dt = 100A/µs ④⑤
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L_S+L_D)				

Notes:

① Repetitive rating; pulse width limited by max. junction temperature.

② Starting T_J = 25°C, L = 0.36mH R_G = 25W, I_{AS} = 35A.

③ I_{SD} £ 35A, di/dt £ 100A/µs, V_{DD} £ $V_{(BR)DSS}$, T_J £ 150°C

④ Pulse width £ 300µs; duty cycle £ 2%.

⑤ Uses IRL3102 data and test conditions

** When mounted on FR-4 board using minimum recommended footprint.
For recommended footprint and soldering techniques refer to application note #AN-994.

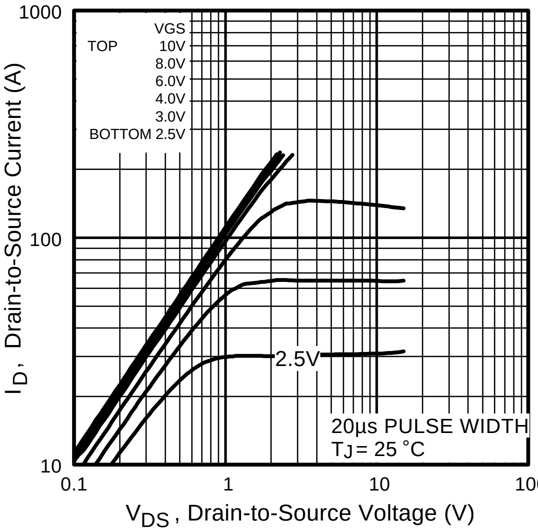


Fig 1. Typical Output Characteristics

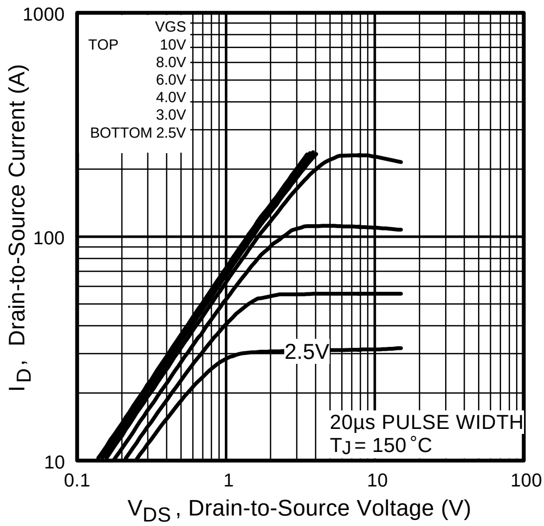


Fig 2. Typical Output Characteristics

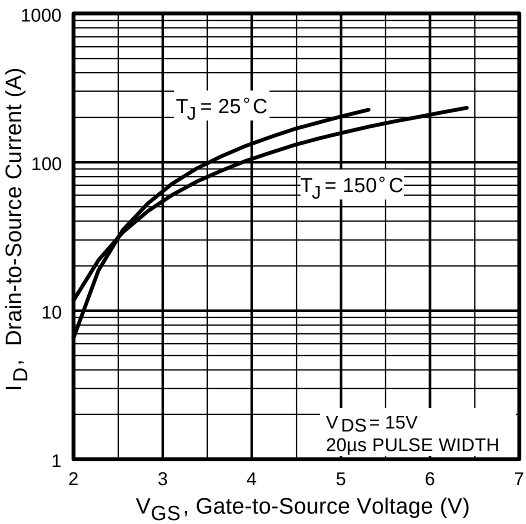


Fig 3. Typical Transfer Characteristics

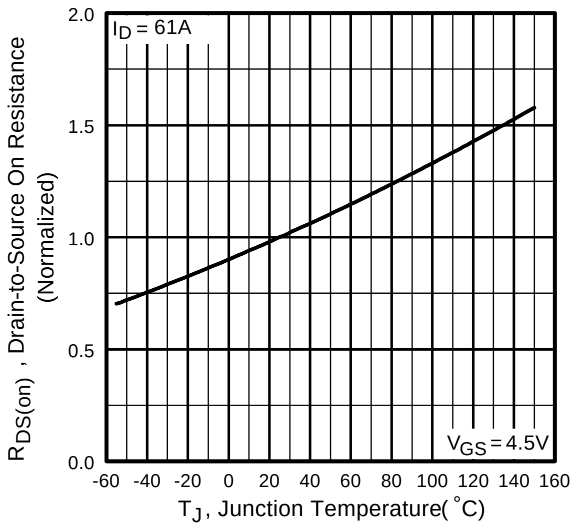


Fig 4. Normalized On-Resistance Vs. Temperature

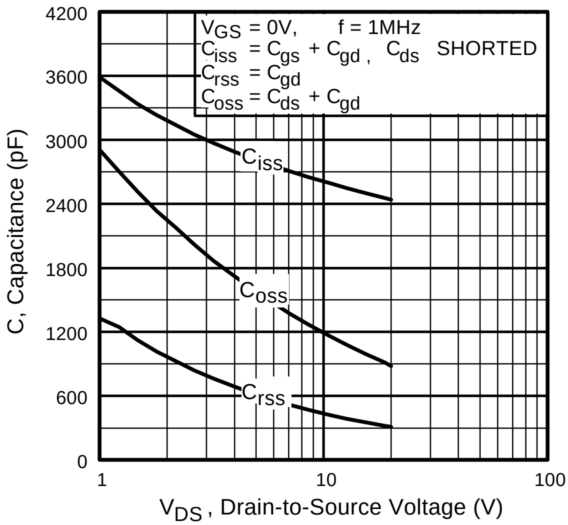


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

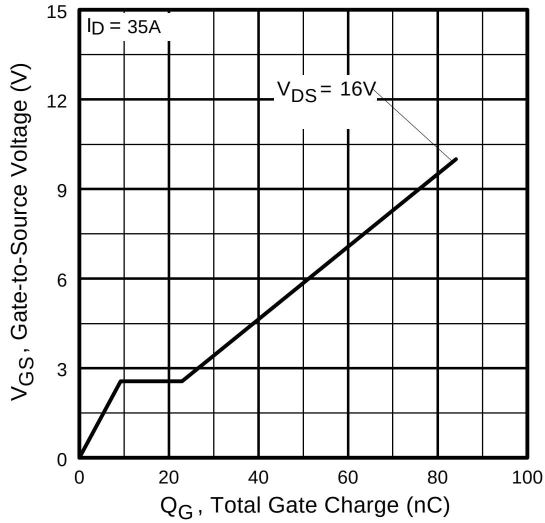


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

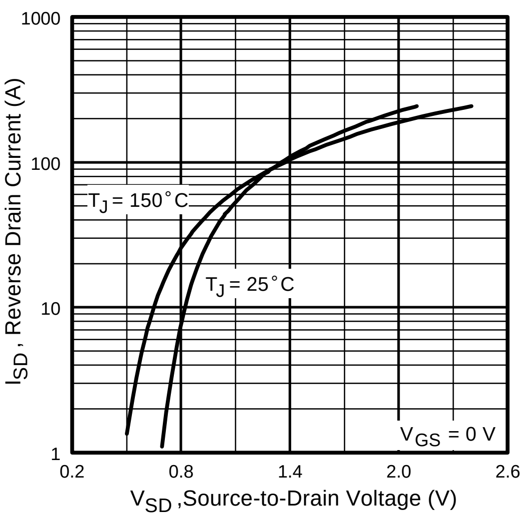


Fig 7. Typical Source-Drain Diode Forward Voltage

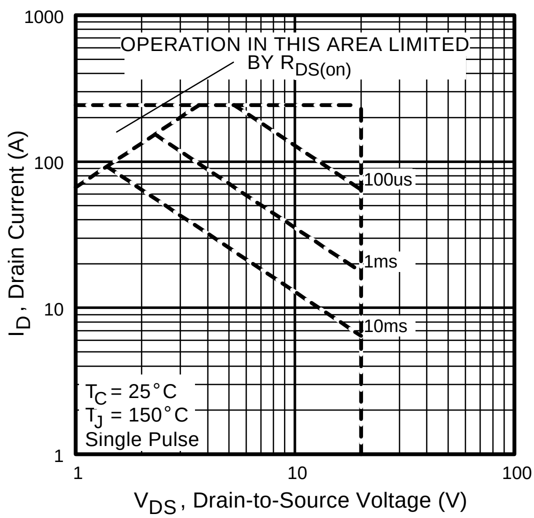


Fig 8. Maximum Safe Operating Area

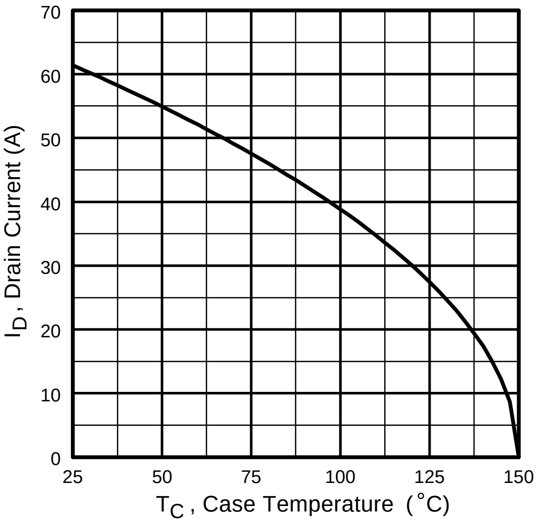


Fig 9. Maximum Drain Current Vs. Case Temperature

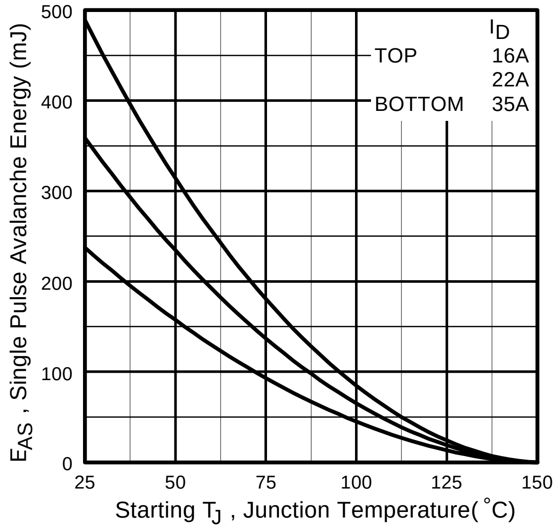


Fig 10. Maximum Avalanche Energy Vs. Drain Current

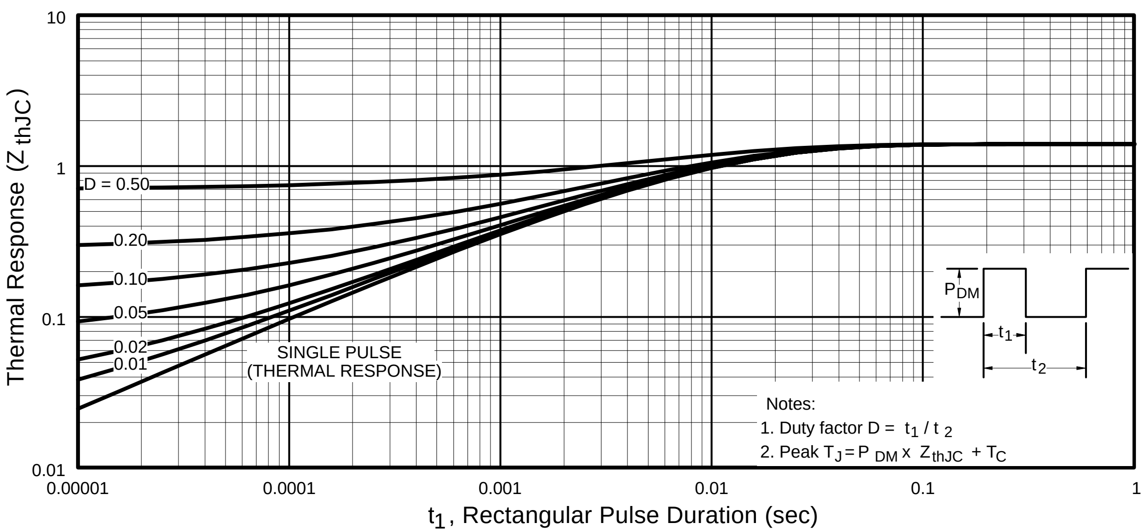


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

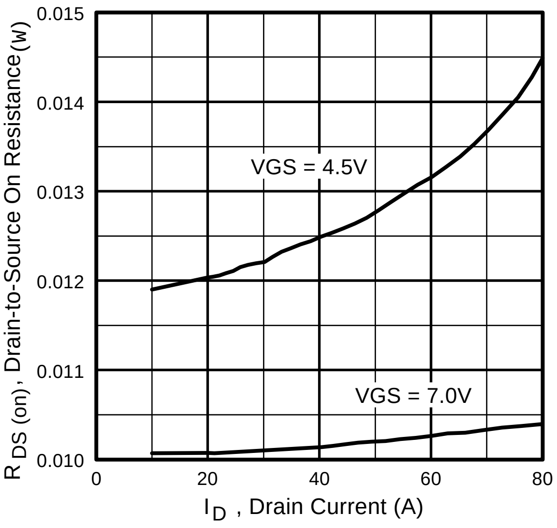


Fig 12. On-Resistance Vs. Drain Current

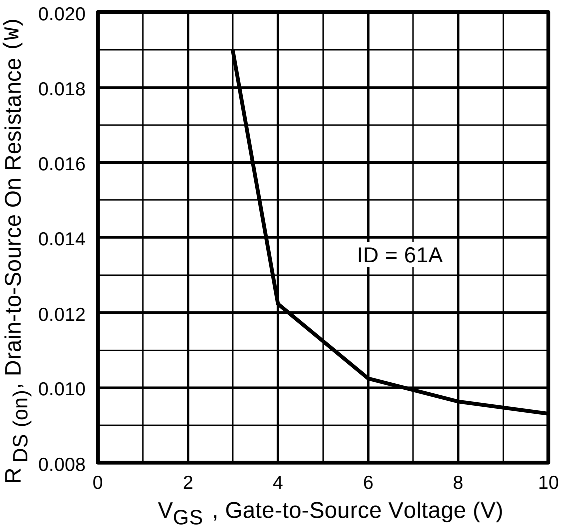
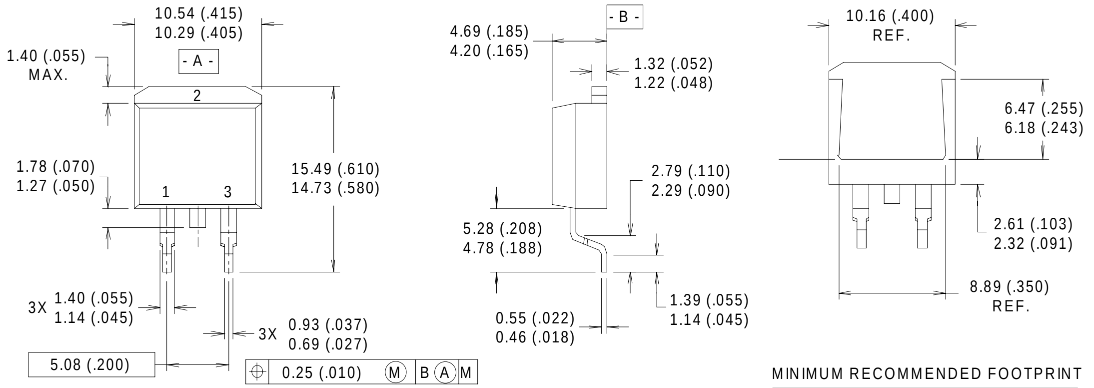
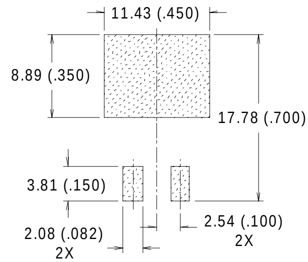


Fig 13. On-Resistance Vs. Gate Voltage

D²Pak Package Outline



MINIMUM RECOMMENDED FOOTPRINT



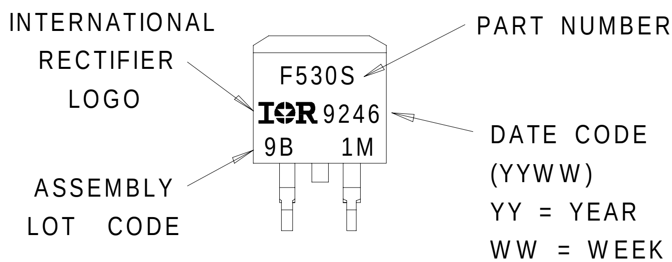
NOTES:

1 DIMENSIONS AFTER SOLDER DIP.
2 DIMENSIONING & TOLERANCING PER ANSI Y14.5M, 1982.
3 CONTROLLING DIMENSION : INCH.
4 HEATSINK & LEAD DIMENSIONS DO NOT INCLUDE BURRS.

LEAD ASSIGNMENTS
1 - GATE
2 - DRAIN
3 - SOURCE

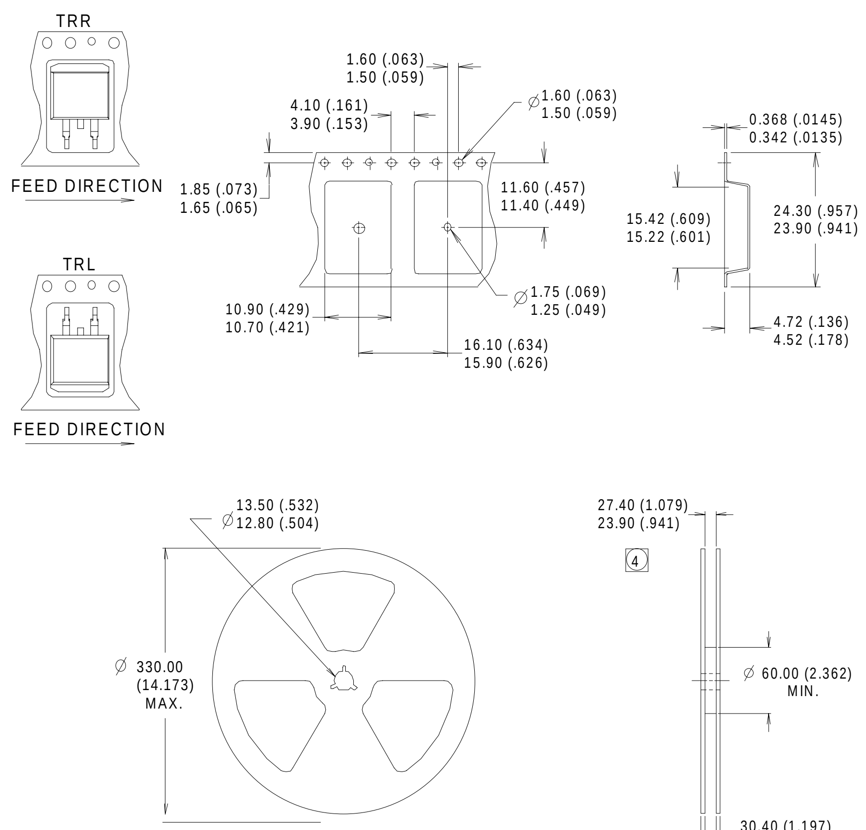
Part Marking Information

D²Pak



Tape & Reel Information

D²Pak



NOTES :
1. COMFORMS TO EIA-418.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION MEASURED @ HUB.
4. INCLUDES FLANGE DISTORTION @ OUTER EDGE.

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