

MECHANICAL DATA

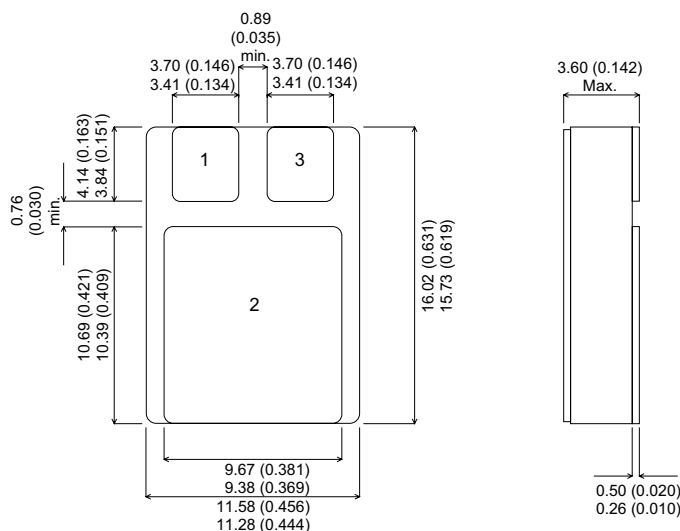
Dimensions in mm (inches)

N-CHANNEL POWER MOSFET

V_{DSS}	60V
$I_{D(cont)}$	34A
$R_{DS(on)}$	0.040 Ω

FEATURES

- **HERMETICALLY SEALED SURFACE MOUNT PACKAGE**
- **SMALL FOOTPRINT – EFFICIENT USE OF PCB SPACE.**
- **SIMPLE DRIVE REQUIREMENTS**
- **LIGHTWEIGHT**
- **HIGH PACKING DENSITIES**



SMD1 – Surface Mount Package

Pad 1 – Gate

Pad 2 – Drain

Pad 3 – Source

Note: IRFNxxx also available with pins 1 and 3 reversed.

ABSOLUTE MAXIMUM RATINGS ($T_{case} = 25^{\circ}C$ unless otherwise stated)

V_{GS}	Gate – Source Voltage	$\pm 20V$
I_D	Continuous Drain Current ($V_{GS} = 0$, $T_{case} = 25^{\circ}C$)	34A
I_D	Continuous Drain Current ($V_{GS} = 0$, $T_{case} = 100^{\circ}C$)	21A
I_{DM}	Pulsed Drain Current ¹	136A
P_D	Power Dissipation @ $T_{case} = 25^{\circ}C$	75W
	Linear Derating Factor	0.6W/ $^{\circ}C$
E_{AS}	Single Pulse Avalanche Energy ²	340mJ
dv/dt	Peak Diode Recovery ³	4.5V/ns
T_J , T_{stg}	Operating and Storage Temperature Range	-55 to $150^{\circ}C$
T_L	Package Mounting Surface Temperature (for 5 sec)	$300^{\circ}C$
$R_{\theta JC}$	Thermal Resistance Junction to Case	$1.67^{\circ}C/W$
$R_{\theta J-PCB}$	Thermal Resistance Junction to PCB (Typical)	$4^{\circ}C/W$

Notes

- 1) Pulse Test: Pulse Width $\leq 300\text{ms}$, $\delta \leq 2\%$
- 2) @ $V_{DD} = 25\text{V}$, $L \geq 0.3\text{mH}$, $R_G = 25\Omega$, Peak $I_L = 34\text{A}$, Starting $T_J = 25^\circ\text{C}$
- 3) @ $I_{SD} \leq 34\text{A}$, $di/dt \leq 100\text{A}/\mu\text{s}$, $V_{DD} \leq BV_{DSS}$, $T_J \leq 150^\circ\text{C}$, SUGGESTED $R_G = 9.1\Omega$

ELECTRICAL CHARACTERISTICS ($T_{amb} = 25^{\circ}\text{C}$ unless otherwise stated)

Parameter		Test Conditions		Min.	Typ.	Max.	Unit
STATIC ELECTRICAL RATINGS							
BV _{DSS}	Drain – Source Breakdown Voltage	V _{GS} = 0	I _D = 1mA	60			V
ΔBV _{DSS} ΔT _J	Temperature Coefficient of Breakdown Voltage	Reference to 25°C I _D = 1mA			0.68		V/°C
R _{DS(on)}	Static Drain – Source On–State Resistance ¹	V _{GS} = 10V	I _D = 21A			0.040	Ω
		V _{GS} = 10V	I _D = 34A			0.050	
V _{GS(th)}	Gate Threshold Voltage	V _{DS} = V _{GS}	I _D = 250μA	2		4	V
g _{fs}	Forward Transconductance ¹	V _{DS} ≥ 15V	I _{DS} = 21A	17			S(Ω)
I _{DSS}	Zero Gate Voltage Drain Current	V _{GS} = 0	V _{DS} = 0.8BV _{DSS}			25	μA
			T _J = 125°C			250	
I _{GSS}	Forward Gate – Source Leakage	V _{GS} = 20V				100	nA
I _{GSS}	Reverse Gate – Source Leakage	V _{GS} = –20V				–100	
DYNAMIC CHARACTERISTICS							
C _{iss}	Input Capacitance	V _{GS} = 0 V _{DS} = 25V f = 1MHz			2400		pF
C _{oss}	Output Capacitance				1100		
C _{rss}	Reverse Transfer Capacitance				230		
Q _g	Total Gate Charge ¹	V _{GS} = 10V I _D = 34A V _{DS} = 0.5BV _{DSS}		39		88	nC
Q _{gs}	Gate – Source Charge ¹	I _D = 34A V _{DS} = 0.5BV _{DSS}		6.7		15	nC
Q _{gd}	Gate – Drain (“Miller”) Charge ¹			18		52	
t _{d(on)}	Turn–On Delay Time	V _{DD} = 30V I _D = 34A R _G = 9.1Ω				23	ns
t _r	Rise Time					130	
t _{d(off)}	Turn–Off Delay Time					81	
t _f	Fall Time					79	
SOURCE – DRAIN DIODE CHARACTERISTICS							
I _S	Continuous Source Current					34	A
I _{SM}	Pulse Source Current ²					136	
V _{SD}	Diode Forward Voltage	I _S = 34A T _J = 25°C V _{GS} = 0				2.5	V
t _{rr}	Reverse Recovery Time	I _F = 34A T _J = 25°C				220	ns
Q _{rr}	Reverse Recovery Charge	d _i / d _t ≤ 100A/μs V _{DD} ≤ 50V				1.6	μC
t _{on}	Forward Turn–On Time			Negligible			
PACKAGE CHARACTERISTICS							
L _D	Internal Drain Inductance (from centre of drain pad to die)				0.8		nH
L _S	Internal Source Inductance (from centre of source pad to end of source bond wire)				2.8		

Notes

- 1) Pulse Test: Pulse Width $\leq 300\text{ms}$, $\delta \leq 2\%$
- 2) Repetitive Rating – Pulse width limited by maximum junction temperature.