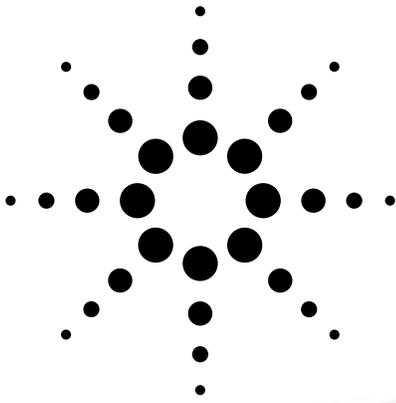


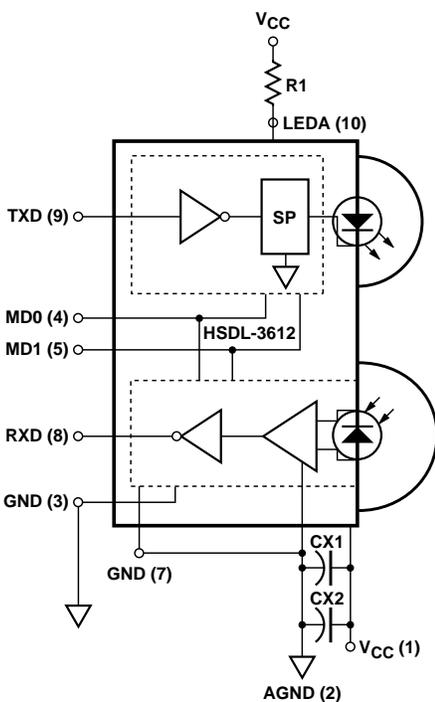
Agilent HSDL-3612 IrDA® Data 1.4 Compliant 115.2 kb/s 3 V to 5 V Infrared Transceiver Data Sheet



Description

The HSDL-3612 is a low-profile infrared transceiver module that provides interface between logic and IR signals for through-air, serial, half-duplex IR data link. The module is compliant to IrDA Data Physical Layer Specifications 1.0 and IEC825-Class 1 Eye Safe.

Functional Block Diagram



Applications

- **Digital imaging**
 - Digital still cameras
 - Photo-imaging printers
- **Data communication**
 - Notebook computers
 - Desktop PCs
 - Win CE handheld products
 - Personal Digital Assistants (PDAs)
 - Printers
 - Fax machines, photocopiers
 - Screen projectors
 - Auto PCs
 - Dongles
 - Set-Top box
- **Telecommunication products**
 - Cellular phones
 - Pagers
- **Small industrial & medical instrumentation**
 - General data collection devices
 - Patient & pharmaceutical data collection devices

Features

- **Fully compliant to IrDA 1.0 physical layer specifications**
 - 9.6 kb/s to 115.2 kb/s operation
- **Typical link distance > 1.5 m**
- **IEC825-Class 1 eye safe**
- **Low power operation range**
 - 2.7 V to 5.25 V
- **Small module size**
 - 4.0 x 12.2 x 4.9 mm (HxWxD)
- **Complete shutdown**
 - TXD, RXD, PIN diode
- **Low shutdown current**
 - 10 nA typical
- **Adjustable optical power management**
 - Adjustable LED drive-current to maintain link integrity
- **Integrated EMI shield**
 - Excellent noise immunity
- **Edge detection input**
 - Prevents the LED from long turn-on time
- **Interface to various super I/O and controller devices**
- **Designed to accommodate light loss with cosmetic window**
- **Only 2 external components are required**

The HSDL-3612 contains a high-speed and high-efficiency 870 nm LED, a silicon PIN diode, and an integrated circuit. The IC contains an LED driver and a receiver providing a single output (RXD) for all data rates supported.

The HSDL-3612 can be completely shut down to achieve very low power consumption. In the shut down mode, the PIN diode will be inactive and thus producing very little photo-current even under very bright ambient light. The HSDL-3612

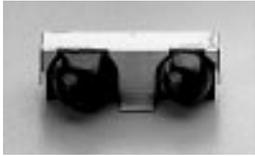
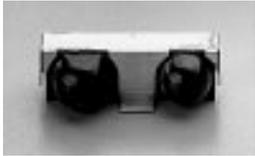
also incorporated the capability for adjustable optical power. With two programming pins; MODE 0 and MODE 1, the optical power output can be adjusted lower when the nominal desired link distance is one-third or two-third of the full IrDA link.

The HSDL-3612 front view options (HSDL-3612-007/-037) come with integrated shield that helps to ensure low EMI emission and high immunity to EMI field, thus enhancing reliable performance.

Application Support Information

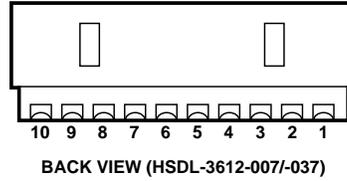
The Application Engineering group is available to assist you with the technical understanding associated with HSDL-3612 infrared transceiver module. You can contact them through your local sales representatives for additional details.

Ordering Information

Package Option	Package	Part Number	Standard Package Increment
	Front View	HSDL-3612-007	400
	Front View	HSDL-3612-037	1800

I/O Pins Configuration Table

Pin	Description	Symbol
1	Supply Voltage	V _{CC}
2	Analog Ground	AGND
3	Ground	GND
4	Mode 0	MD0
5	Mode 1	MD1
6	No Connection	NC
7	Ground	GND
8	Receiver Data Output	RXD
9	Transmitter Data Input	TXD
10	LED Anode	LEDA



Transceiver Control Truth Table

Mode 0	Mode 1	RX Function	TX Function
1	0	Shutdown	Shutdown
0	0	SIR	Full Distance Power
0	1	SIR	2/3 Distance Power
1	1	SIR	1/3 Distance Power

Transceiver I/O Truth Table

Transceiver Mode	Inputs		Outputs	
	TXD	EI	LED	RXD
Active	1	X	On	Not Valid
Active	0	High ^[1]	Off	Low ^[2]
Active	0	Low	Off	High
Shutdown	X ^[3]	Low	Not Valid	Not Valid

X = Don't Care EI = In-Band Infrared Intensity at detector

Notes:

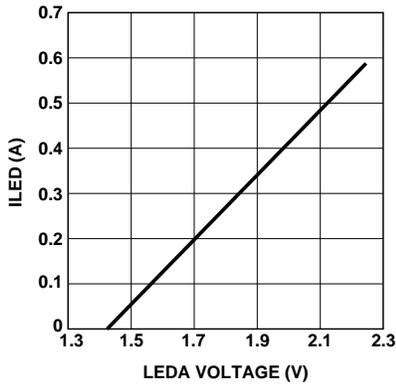
1. In-Band EI ≤ 115.2 kb/s.
2. Logic Low is a pulsed response. The condition is maintained for duration dependent on the pattern and strength of the incident intensity.
3. To maintain low shutdown current, TXD needs to be driven high or low and not left floating.

Recommended Application Circuit Components

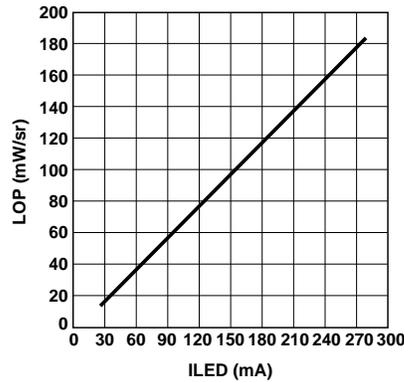
Component	Recommended Value
R1	6.2 Ω \pm 5%, 0.5 Watt, for 2.7 \leq V _{CC} \leq 3.6 V operation 15.0 Ω \pm 5%, 0.5 Watt, for 4.75 \leq V _{CC} \leq 5.25 V operation
CX1 ^[4]	0.47 μ F \pm 20%, X7R Ceramic
CX2 ^[5]	6.8 μ F \pm 20%, Tantalum

Notes:

- CX1 must be placed within 0.7 cm of the HSDL-3612 to obtain optimum noise immunity.
- In environments with noisy power supplies, supply rejection performance can be enhanced by including CX2, as shown in "HSDL-3612 Functional Block Diagram" in page 3.



I_{LED} vs. LEDA.



Light Output Power (LOP) vs. I_{LED}.

Marking Information

The HSDL-3612-007/-037 is marked "3612YYWW" on the shield where "YY" indicates the unit's manufacturing year, and "WW" refers to the work week in which the unit is tested.

CAUTIONS: The BiCMOS inherent to the design of this component increases the component's susceptibility to damage from electrostatic discharge (ESD). It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation which may be induced by ESD.

Absolute Maximum Ratings^[6]

Parameter	Symbol	Minimum	Maximum	Unit	Conditions
Storage Temperature	T _S	-40	+100	°C	
Operating Temperature	T _A	-20	+70	°C	
DC LED Current	I _{LED(DC)}		165	mA	
Peak LED Current	I _{LED(PK)}		750	mA	≤ 2 μs pulse width, ≤ 10% duty cycle
LED Anode Voltage	V _{LEDA}	-0.5	7	V	
Supply Voltage	V _{CC}	0	7	V	
Transmitter Data Input Current	I _{TXD(DC)}	-12	12	mA	
Receiver Data Output Voltage	V _O	-0.5	V _{CC} +0.5	V	I _{O(RXD)} = 20 μA

Note:

6. For implementations where case to ambient thermal resistance ≤ 50°C/W.

Recommended Operating Conditions

Parameter	Symbol	Minimum	Maximum	Unit
Operating Temperature	T _A	-20	+70	°C
Supply Voltage	V _{CC}	2.7	5.25	V
Logic High Input Voltage for TXD, MD0, MD1, and FIR_SEL	V _{IH}	2 V _{CC} /3	V _{CC}	V
Logic Low Transmitter Input Voltage	V _{IL}	0	V _{CC} /3	V
LED (Logic High) Current Pulse Amplitude	I _{LEDA}	180	300	mA
Receiver Signal Rate		2.4	115.2	kb/s

Electrical & Optical Specifications

Specifications hold over the Recommended Operating Conditions unless otherwise noted. Unspecified test conditions can be anywhere in their operating range. All typical values are at 25 °C and 3.3 V unless otherwise noted.

Parameter		Symbol	Min.	Typ.	Max.	Unit	Conditions
Transceiver							
Supply Current	Shutdown	I_{CC1}		10	200	nA	$V_I(\text{TXD}) \leq V_{IL}$ or $V_I(\text{TXD}) \geq V_{IH}$
	Idle	I_{CC2}		2.5	5	mA	$V_I(\text{TXD}) \leq V_{IL}$, $EI = 0$
Digital Input Current	Logic Low/High	$I_{L/H}$	-1		1	μA	$0 \leq V_I \leq V_{CC}$
Transmitter							
Transmitter Radiant Intensity	Logic High Intensity	E_{IH}	50	120	400	mW/sr	$V_{IH} = 3.0 \text{ V}$ $I_{LEDA} = 200 \text{ mA}$ $\theta_{1/2} \leq 15^\circ$
	Peak Wavelength	λ_P		875		nm	
	Spectral Line Half Width	$\Delta\lambda_{1/2}$		35		nm	
	Viewing Angle	$2\theta_{1/2}$	30		60	°	
	Optical Pulse Width	$tpw(EI)$	1.5	1.6	1.8	μs	$tpw(\text{TXD}) = 1.6 \mu\text{s}$ at 115.2 kb/s
	Rise and Fall Times	$t_r(EI)$, $t_f(EI)$			40	ns	$tpw(\text{TXD}) = 1.6 \mu\text{s}$ at 115.2 kb/s $t_{r/f}(\text{TXD}) = 10 \text{ ns}$
	Maximum Optical Pulse Width	$tpw(\text{max})$		20	50	μs	TXD pin stuck high
LED Anode On State Voltage		$V_{ON}(\text{LEDA})$			2.4	V	$I_{LEDA} = 200 \text{ mA}$, $V_I(\text{TXD}) \geq V_{IH}$
LED Anode Off State Leakage Current		$I_{LK}(\text{LEDA})$		1	100	nA	$V_{LEDA} = V_{CC} = 5.25 \text{ V}$, $V_I(\text{TXD}) \leq V_{IL}$

Electrical & Optical Specifications

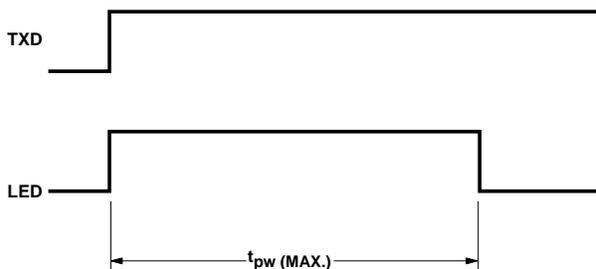
Specifications hold over the Recommended Operating Conditions unless otherwise noted. Unspecified test conditions can be anywhere in their operating range. All typical values are at 25 °C and 3.3 V unless otherwise noted.

	Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Receiver							
Receiver Data Output Voltage	Logic Low ^[7]	V_{OL}	0	-	0.4	V	$I_{OL} = 1.0 \text{ mA}$, $EI \geq 3.6 \mu\text{W}/\text{cm}^2$, $\theta_{1/2} \leq 15^\circ$
	Logic High	V_{OH}	$V_{CC} - 0.2$	-	V_{CC}	V	$I_{OH} = -20 \mu\text{A}$, $EI \leq 0.3 \mu\text{W}/\text{cm}^2$, $\theta_{1/2} \leq 15^\circ$
	Viewing Angle	$2\theta_{1/2}$	30			°	
Logic High Receiver Input Irradiance		EI_H	0.0036		500	mW/cm^2	For in-band signals $\leq 115.2 \text{ kb/s}$ ^[8]
Logic Low Receiver Input Irradiance		EI_L			0.3	$\mu\text{W}/\text{cm}^2$	For in-band signals ^[8]
Receiver Peak Sensitivity Wavelength		λ_P		880		nm	
Receiver SIR Pulse Width		$t_{pw} \text{ (SIR)}$	1		4.0	μs	$\theta_{1/2} \leq 15^\circ$ ^[9] , $C_L = 10 \text{ pF}$
Receiver Latency Time		t_L		20	50	μs	
Receiver Rise/Fall Times		$t_{r/f} \text{ (RXD)}$		25		ns	
Receiver Wake Up Time		t_W			100	μs	[10]

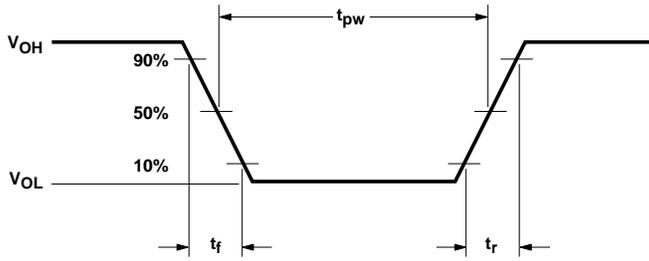
Notes:

7. Logic Low is a pulsed response. The condition is maintained for duration dependent on pattern and strength of the incident intensity.
8. An in-band optical signal is a pulse/sequence where the peak wavelength, λ_P , is defined as $850 \leq \lambda_P \leq 900 \text{ nm}$, and the pulse characteristics are compliant with the IrDA Serial Infrared Physical Layer Link Specification.
9. For in-band signals $\leq 115.2 \text{ kb/s}$ where $3.6 \mu\text{W}/\text{cm}^2 \leq EI \leq 500 \text{ mW}/\text{cm}^2$.
10. Wake Up Time is the time between the transition from a shutdown state to an active state and the time when the receiver is active and ready to receive infrared signals.

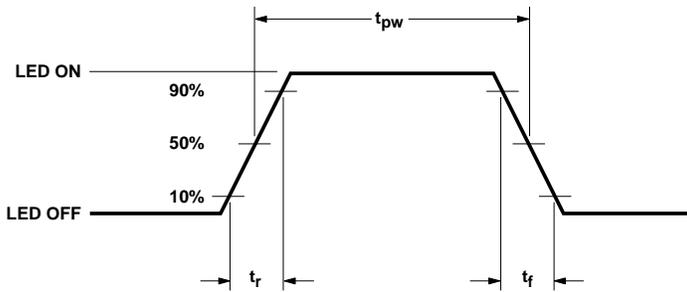
TXD “Stuck ON” Protection



RXD Output Waveform

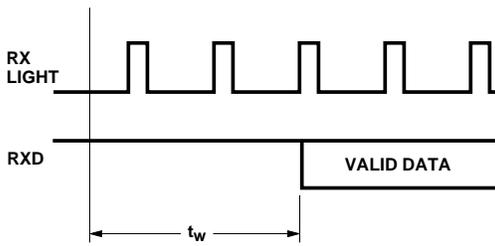


LED Optical Waveform



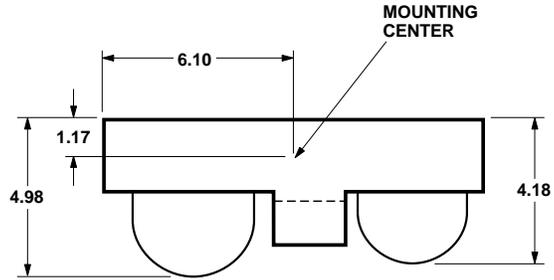
Receiver Wake Up Time Definition

(when MD0 π 1 and MD1 π 0)

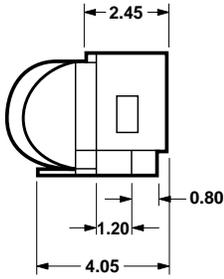


HSDL-3612-007 and HSDL3612-037 Package Outline with Dimension and Recommended PC Board Pad Layout

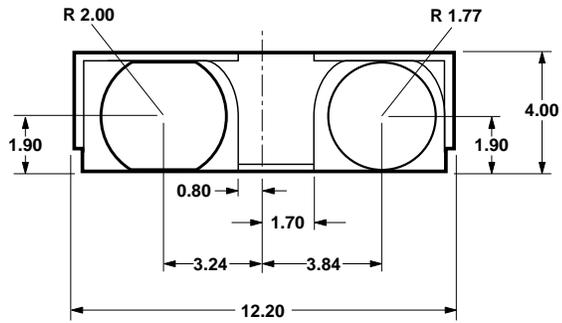
PIN	FUNCTION	PIN	FUNCTION
1	V _{CC}	6	NC
2	AGND	7	GND
3	GND	8	RXD
4	MD0	9	TXD
5	MD1	10	LEDA



TOP VIEW

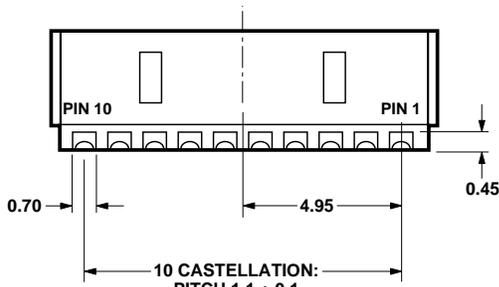


SIDE VIEW

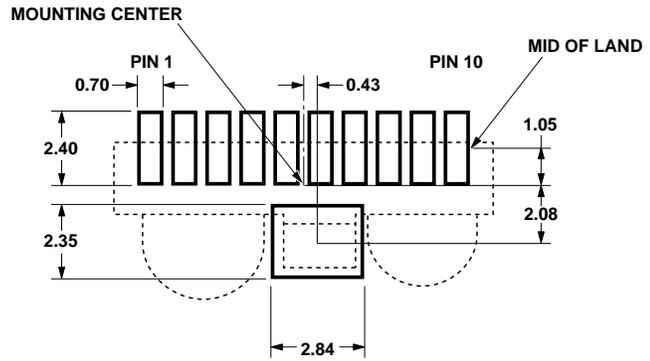


FRONT VIEW

ALL DIMENSIONS IN MILLIMETERS (mm).
DIMENSION TOLERANCE IS 0.20 mm
UNLESS OTHERWISE SPECIFIED.



BACK VIEW

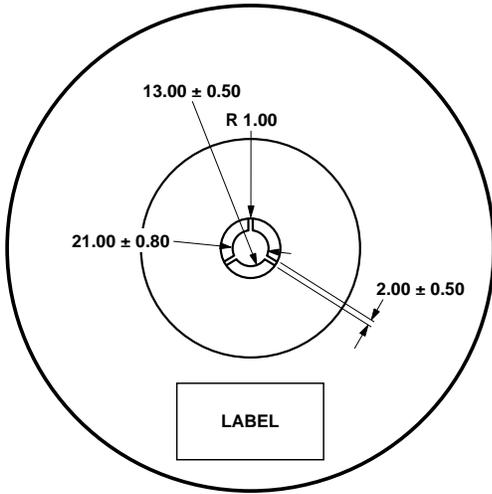


LAND PATTERN

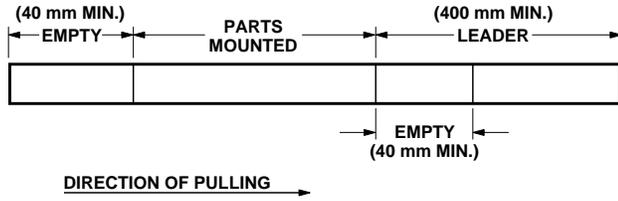
Tape and Reel Dimensions (HSDL-3612-007, -037)

ALL DIMENSIONS IN MILLIMETERS (mm)

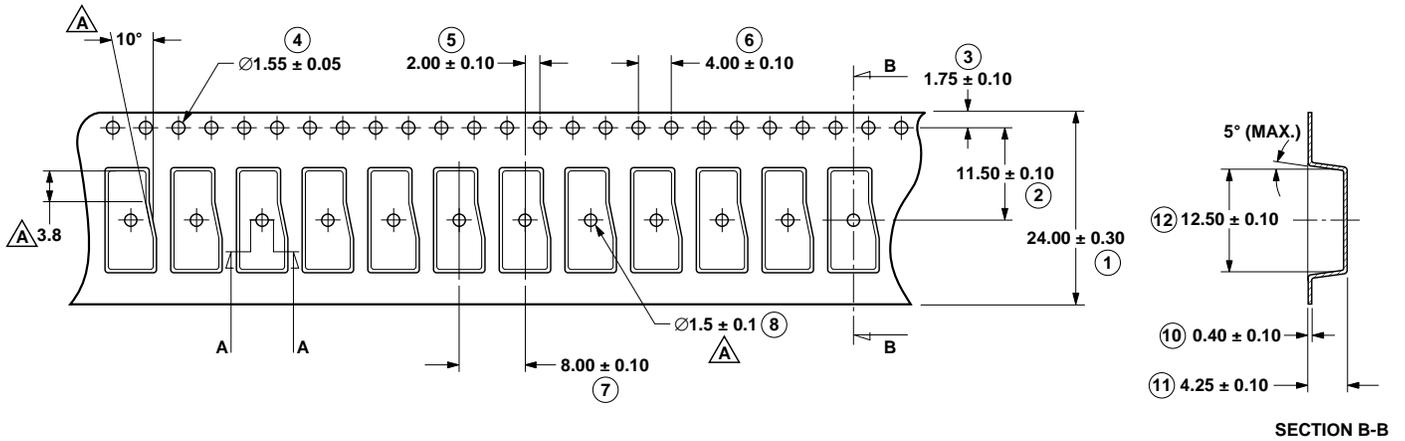
QUANTITY = 400 PIECES PER REEL (HSDL-3612-007)
1800 PIECES PER TAPE (HSDL-3612-037)



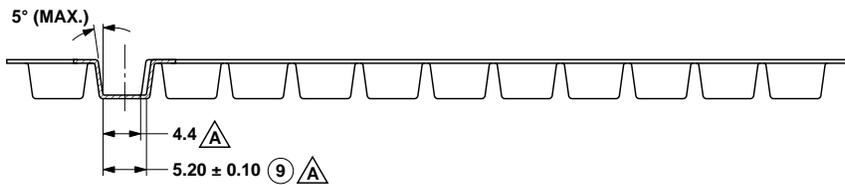
SHAPE AND DIMENSIONS OF REELS



CONFIGURATION OF TAPE



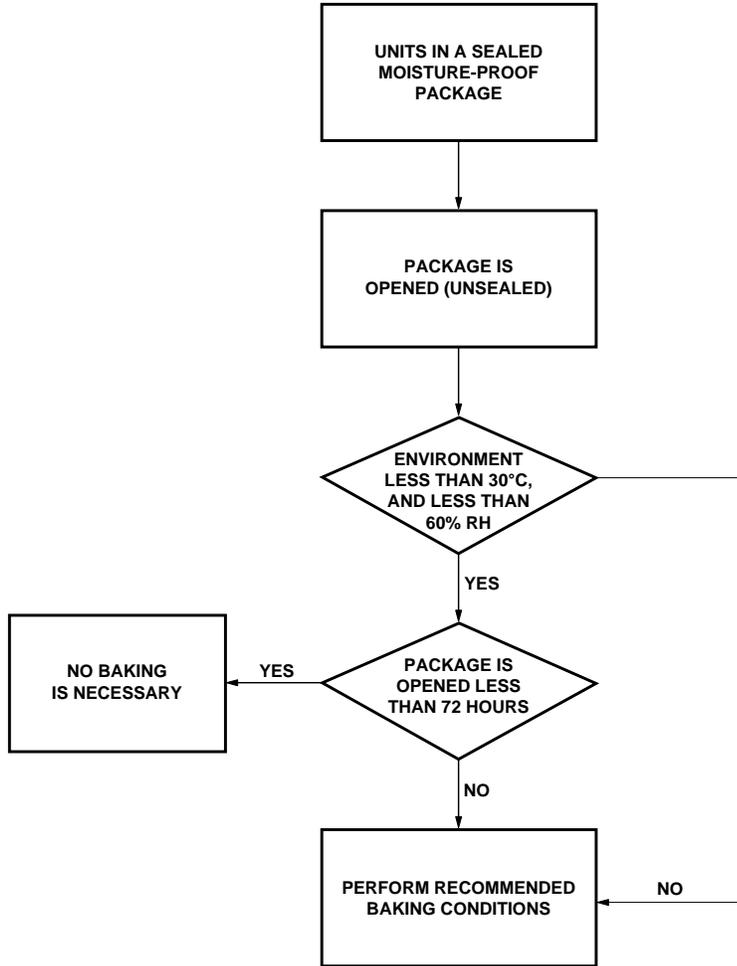
SECTION B-B



SECTION A-A

Moisture Proof Packaging

All HSDL-3612 options are shipped in moisture proof package. Once opened, moisture absorption begins.



Baking Conditions

If the parts are not stored in dry conditions, they must be baked before reflow to prevent damage to the parts.

Package	Temp.	Time
In reels	60°C	≥ 48 hours
In bulk	100°C	≥ 4 hours
	125°C	≥ 2 hours
	150°C	≥ 1 hour

Baking should be done only once.

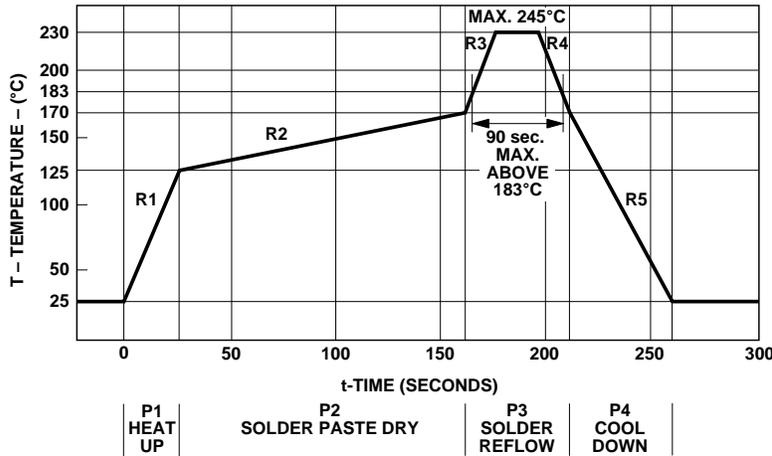
Recommended Storage Conditions

Storage Temperature	10°C to 30°C
Relative Humidity	below 60% RH

Time from Unsealing to Soldering

After removal from the bag, the parts should be soldered within three days if stored at the recommended storage conditions. If times longer than 72 hours are needed, the parts must be stored in a dry box.

Reflow Profile



Process Zone	Symbol	DT	Maximum DT/Dtime
Heat Up	P1, R1	25°C to 125°C	4°C/s
Solder Paste Dry	P2, R2	125°C to 170°C	0.5°C/s
Solder Reflow	P3, R3	170°C to 230°C (245°C at 10 seconds max.)	4°C/s
	P3, R4	230°C to 170°C	-4°C/s
Cool Down	P4, R5	170°C to 25°C	-3°C/s

The reflow profile is a straight-line representation of a nominal temperature profile for a convective reflow solder process. The temperature profile is divided into four process zones, each with different $\Delta T/\Delta \text{time}$ temperature change rates. The $\Delta T/\Delta \text{time}$ rates are detailed in the above table. The temperatures are measured at the component to printed circuit board connections.

In **process zone P1**, the PC board and HSDL-3612 castellation I/O pins are heated to a temperature of 125°C to activate the flux in the solder paste. The temperature ramp up rate, R1, is limited to 4°C per second to allow for even heating of both the PC board and HSDL-3612 castellation I/O pins.

Process zone P2 should be of sufficient time duration (> 60 seconds) to dry the solder paste. The temperature is raised to a level just below the liquidus point of the solder, usually 170°C (338°F).

Process zone P3 is the solder reflow zone. In zone P3, the temperature is quickly raised above the liquidus point of solder to 230°C (446°F) for optimum results. The dwell time above the liquidus point of solder should be between 15 and 90 seconds. It usually takes about 15 seconds to assure proper coalescing of the solder balls into liquid solder and the formation of good solder connections. Beyond a dwell time of 90 seconds, the intermetallic growth within the solder connections becomes excessive,

resulting in the formation of weak and unreliable connections. The temperature is then rapidly reduced to a point below the solidus temperature of the solder, usually 170°C (338°F), to allow the solder within the connections to freeze solid.

Process zone P4 is the cool down after solder freeze. The cool down rate, R5, from the liquidus point of the solder to 25°C (77°F) should not exceed -3°C per second maximum. This limitation is necessary to allow the PC board and HSDL-3612 castellation I/O pins to change dimensions evenly, putting minimal stresses on the HSDL-3612 transceiver.

Appendix A: HSDL-3612-007/-037 SMT Assembly Application Note

1.0 Solder Pad, Mask and Metal Solder Stencil Aperture

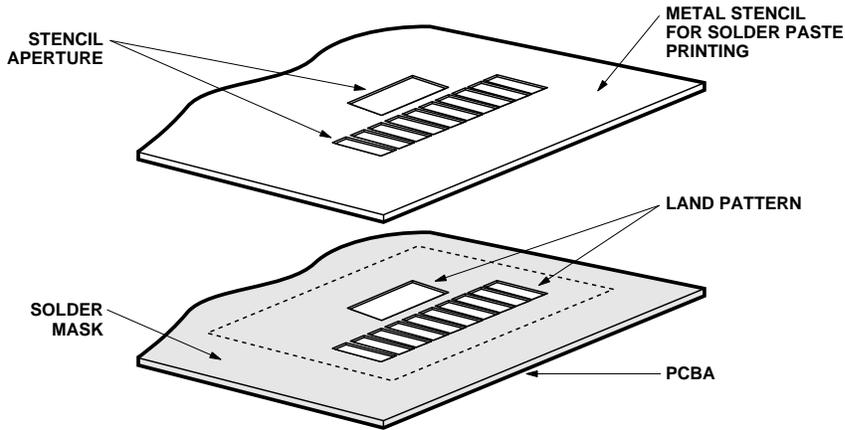


Figure 1.0. Stencil and PCBA.

1.1 Recommended Land Pattern for HSDL-3612-007/-037

Dim.	mm	Inches
a	2.40	0.095
b	0.70	0.028
c (pitch)	1.10	0.043
d	2.35	0.093
e	2.80	0.110
f	3.13	0.123
g	4.31	0.170

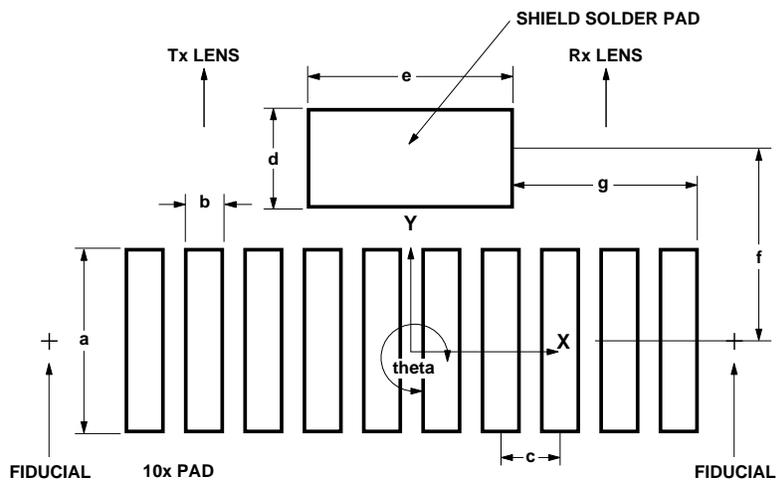


Figure 2.0. Top view of land pattern.

1.2 Adjacent Land Keep-out and Solder Mask Areas

Dim.	mm	Inches
h	min. 0.2	min. 0.008
j	13.4	0.528
k	4.7	0.185
l	3.2	0.126

- Adjacent land keep-out is the **maximum space** occupied by the unit relative to the land pattern. There should be no other SMD components within this area.
- “h” is the minimum solder resist strip width required to avoid solder bridging adjacent pads.
- It is recommended that 2 fiducial cross be placed at mid-length of the pads for unit alignment.

Note: Wet/Liquid Photo-Imaginable solder resist/mask is recommended.

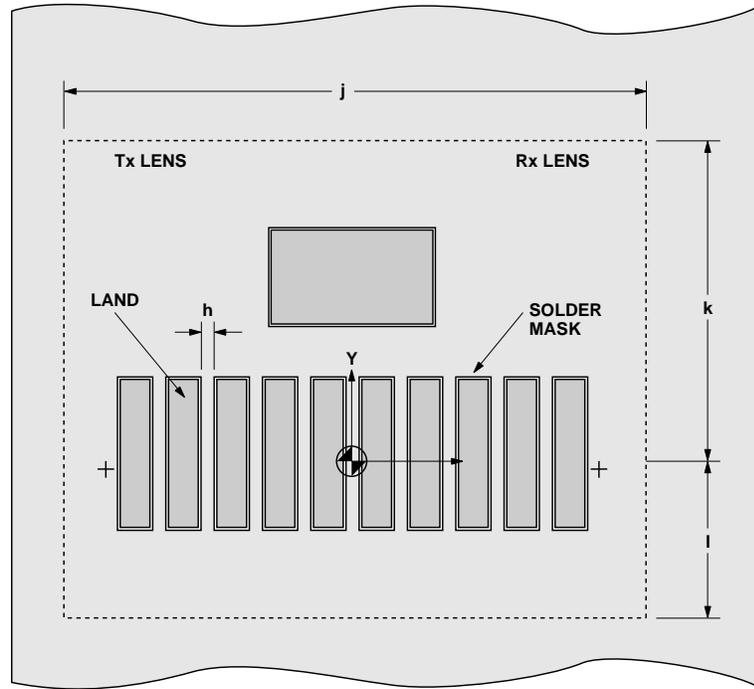


Figure 3.0. HSDL-3612-007/-037 PCBA – Adjacent land keep-out and solder mask.

2.0 Recommended Solder Paste/ Cream Volume for Castellated Joints

Based on calculation and experiment, the printed solder paste volume required per castellated pad is **0.30 cubic mm** (based on either no-clean or aqueous solder cream types with typically 60 to 65% solid content by volume).

2.1 Recommended Metal Solder Stencil Aperture

It is recommended that only 0.152 mm (0.006 inches) or 0.127 mm (0.005 inches) thick stencil be used for solder paste

printing. This is to ensure adequate printed solder paste volume and no shorting. The following combination of metal stencil aperture and metal stencil thickness should be used:

See Fig 4.0			
t, nominal stencil thickness		l, length of aperture	
mm	inches	mm	inches
0.152	0.006	2.8 ± 0.05	0.110 ± 0.002
0.127	0.005	3.4 ± 0.05	0.134 ± 0.002

w, the width of aperture is fixed at 0.70 mm (0.028 inches)

Aperture opening for shield pad is 2.8 mm x 2.35 mm as per land dimensions

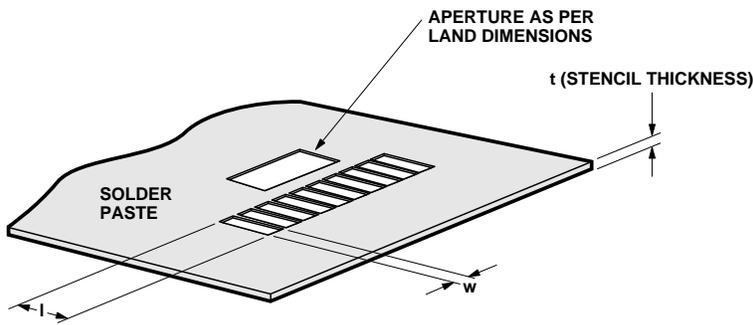


Figure 4.0. Solder paste stencil aperture.

3.0 Pick and Place Misalignment Tolerance and Product Self-Alignment after Solder Reflow

If the printed solder paste volume is adequate, **the unit will self-align** in the X-direction after solder reflow. Units should be properly reflowed in IR Hot Air convection oven using the recommended reflow profile. The direction of board travel does not matter.

Allowable Misalignment Tolerance

X – direction	≤ 0.2 mm (0.008 inches)
Theta – direction	± 2 degrees

3.1 Tolerance for X-axis Alignment of Castellations

Misalignment of castellation to the land pad should not exceed 0.2 mm or approximately half the width of the castellation during

placement of the unit. The castellations will completely self-align to the pads during solder reflow as seen in the pictures below.



Photo 1.0. Castellation misaligned to land pads in x-axis before reflow.

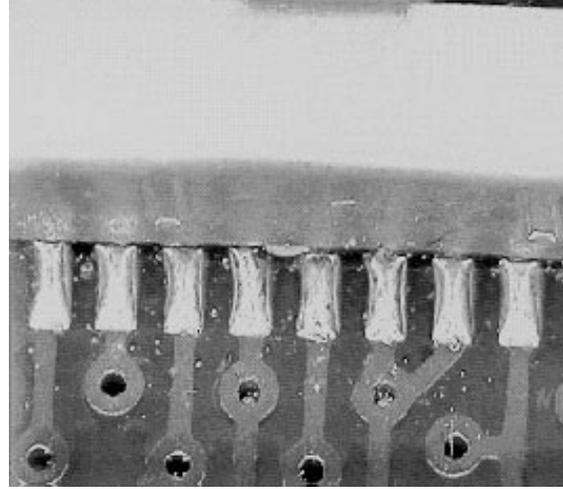


Photo 2.0. Castellation self-align to land pads after reflow.

3.2 Tolerance for Rotational (Theta) Misalignment

Units when mounted should not be rotated more than ± 2 degrees with reference to center X-Y as specified in Fig 2.0. Pictures 3.0 and 4.0 show units before and

after reflow. Units with a Theta misalignment of more than 2 degrees do not completely self-align after reflow. Units with ± 2 degree rotational or Theta misalignment self-aligned completely after solder reflow.

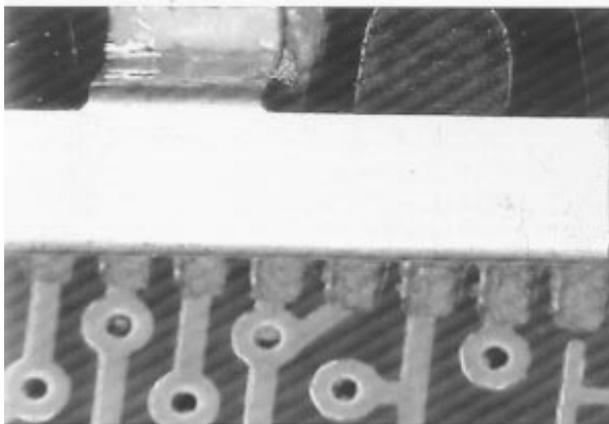


Photo 3.0. Unit is rotated before reflow.



Photo 4.0. Unit self-aligns after reflow.

3.3 Y-axis Misalignment of Castellation

In the Y-direction, the unit does not self-align after solder reflow. It is recommended that the unit be placed in line with the fiducial mark (mid-length of land pad.) This will enable sufficient land length (minimum of 1/2 land length.) to form a good joint. See Fig 5.0.

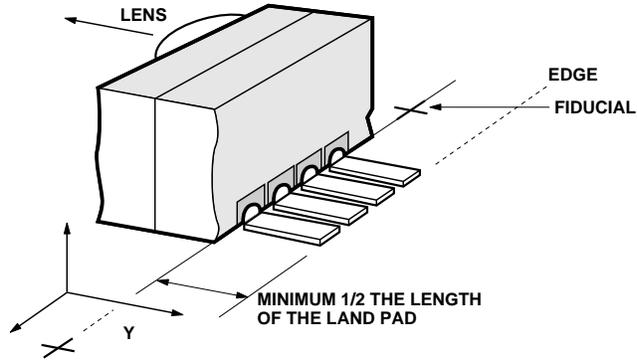


Figure 5.0. Section of a castellation in Y-axis.

3.4 Example of Good HSDL-3612-007/-037 Castellation Solder Joints

This joint is formed when the printed solder paste volume is adequate, i.e. 0.30 cubic mm and reflowed properly. It should be reflowed in IR Hot-air convection reflow oven. Direction of board travel does not matter.

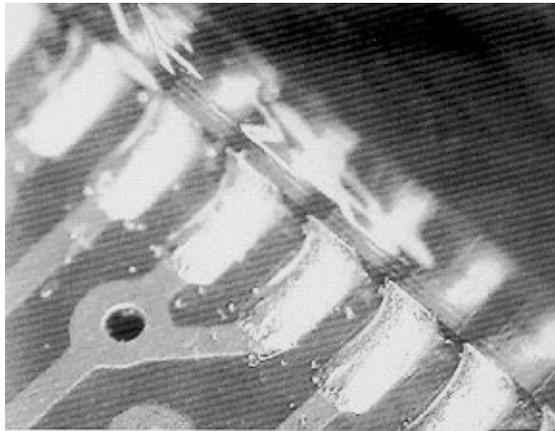
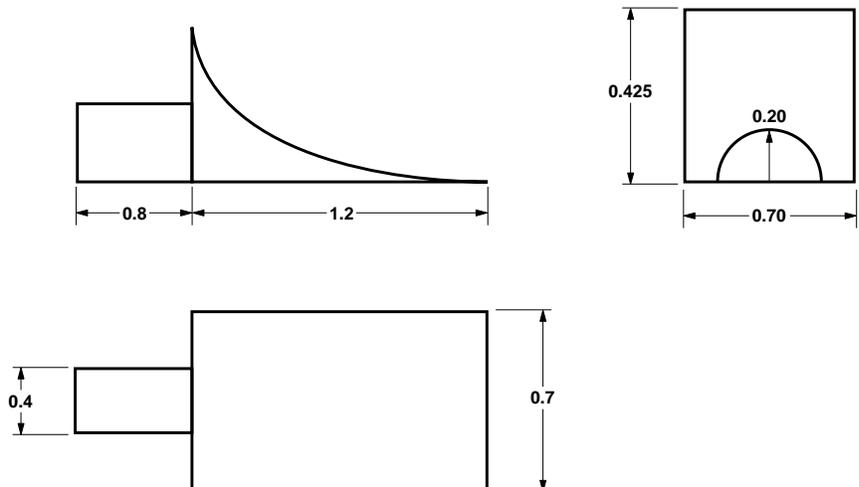


Photo 5.0. Good solder joint.

4.0 Solder Volume Evaluation and Calculation

Geometry of an HSDL-3612-007/-037 solder fillet.



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