

T-39-15

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

Designer's Data Sheet
Power Field Effect Transistor
N-Channel Enhancement-Mode
Silicon Gate TMOS

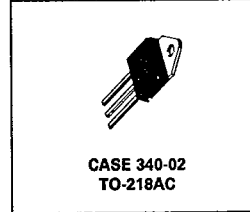
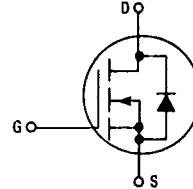
These TMOS Power FETs are designed for high voltage, high speed power switching applications such as switching regulators, converters, solenoid and relay drivers.

- Silicon Gate for Fast Switching Speeds — Switching Times Specified at 100°C
- Designer's Data — I_{DSS} , $V_{DS(on)}$, $V_{GS(th)}$ and SOA Specified at Elevated Temperature
- SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads



MTH8N90

TMOS POWER FETs
8 AMPERES
 $r_{DS(on)} = 1.8$ OHMS
900 VOLTS



MAXIMUM RATINGS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	900	Vdc
Drain-Gate Voltage ($R_{GS} = 1\text{ M}\Omega$)	V_{DGR}	900	Vdc
Gate-Source Voltage — Continuous — Non-Repetitive ($t_p \leq 50\ \mu\text{s}$)	V_{GS} V_{GSM}	± 20 ± 40	Vdc
Drain Current — Continuous — Pulsed	I_D I_{DM}	8 22	Adc
Total Power Dissipation Derate above 25°C	P_D	180 1.44	Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	-65 to 150	°C

THERMAL CHARACTERISTICS

Thermal Resistance — Junction to Case — Junction to Ambient	$R_{\theta JC}$ $R_{\theta JA}$	0.7 30	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8" from case for 5 seconds	T_L	275	°C

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

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ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit	
OFF CHARACTERISTICS					
Drain-Source Breakdown Voltage ($V_{GS} = 0, I_D = 250 \mu\text{A}$)	$V_{(BR)DSS}$	900	—	Vdc	
Zero Gate Voltage Drain Current ($V_{DS} = \text{Rated } V_{DSS}, V_{GS} = 0$) ($V_{DS} = 0.8 \text{ Rated } V_{DSS}, V_{GS} = 0, T_J = 125^\circ\text{C}$)	I_{DSS}	—	250 1000	μA dc	
Gate-Body Leakage Current, Forward ($V_{GSF} = 20 \text{ Vdc}, V_{DS} = 0$)	I_{GSSF}	—	100	nA dc	
Gate-Body Leakage Current, Reverse ($V_{GSR} = 20 \text{ Vdc}, V_{DS} = 0$)	I_{GSSR}	—	100	nA dc	
ON CHARACTERISTICS*					
Gate Threshold Voltage ($V_{DS} = V_{GS}, I_D = 1 \text{ mA}$) $T_J = 100^\circ\text{C}$	$V_{GS(th)}$	2 1.5	4.5 4	Vdc	
Static Drain-Source On-Resistance ($V_{GS} = 10 \text{ Vdc}, I_D = 4 \text{ A}$ dc)	$r_{DS(on)}$	—	1.8	Ohms	
Drain-Source On-Voltage ($V_{GS} = 10 \text{ V}$) ($I_D = 8 \text{ A}$ dc) ($I_D = 4 \text{ A}$ dc, $T_J = 100^\circ\text{C}$)	$V_{DS(on)}$	—	17 15	Vdc	
Forward Transconductance ($V_{DS} = 15 \text{ V}, I_D = 4 \text{ A}$)	g_{FS}	3	—	mhos	
DYNAMIC CHARACTERISTICS					
Input Capacitance	($V_{DS} = 25 \text{ V}, V_{GS} = 0,$ $f = 1 \text{ MHz}$) See Figure 10	C_{iss}	2000 (Typ)	pF	
Output Capacitance		C_{oss}	175 (Typ)		
Reverse Transfer Capacitance		C_{rss}	100 (Typ)		
SWITCHING CHARACTERISTICS* ($T_J = 100^\circ\text{C}$)					
Turn-On Delay Time	($V_{DD} = 25 \text{ V}, I_D = 4 \text{ Amps}$ $R_{gen} = 50 \text{ ohms}$) See Figures 12 and 13	$t_{d(on)}$	55 (Typ)	ns	
Rise Time		t_r	175 (Typ)		
Turn-Off Delay Time		$t_{d(off)}$	440 (Typ)		
Fall Time		t_f	180 (Typ)		
Total Gate Charge	($V_{DS} = 0.8 \text{ Rated } V_{DSS},$ $I_D = 8 \text{ Amps}, V_{GS} = 10 \text{ V}$) See Figures 11 and 14	Q_g	110 (Typ)	nC	
Gate-Source Charge		Q_{gs}	18 (Typ)		
Gate-Drain Charge		Q_{gd}	50 (Typ)		
SOURCE DRAIN DIODE CHARACTERISTICS*					
Forward On-Voltage	($I_S = 8 \text{ Amps}, V_{GS} = 0$)	V_{SD}	1.1 (Typ)	1.5	Vdc
Forward Turn-On Time	($I_S = 8 \text{ A}, di/dt = 100 \text{ A}/\mu\text{s},$ $V_R = 70 \text{ V}$, See Figures 15 and 16)	t_{on}	Limited by stray inductance		
Reverse Recovery Time		t_{rr}	1200 (Typ)	—	ns
INTERNAL PACKAGE INDUCTANCE					
Internal Drain Inductance (Measured from the contact screw on tab to center of die) (Measured from the drain lead 0.25" from package to center of die)	L_d	4 (Typ) 5 (Typ)	—	—	nH
Internal Source Inductance (Measured from the source lead 0.25" from package to source bond pad.)	L_s	10 (Typ)	—	—	nH

*Pulse Test: Pulse Width $\leq 300 \mu\text{s}$, Duty Cycle $\leq 2\%$.

TYPICAL ELECTRICAL CHARACTERISTICS

Figure 1. On-Region Characteristics

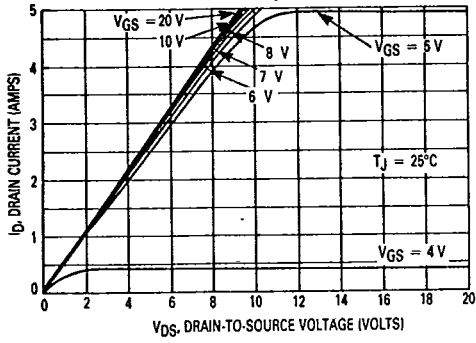


Figure 2. Gate-Threshold Voltage Variation With Temperature

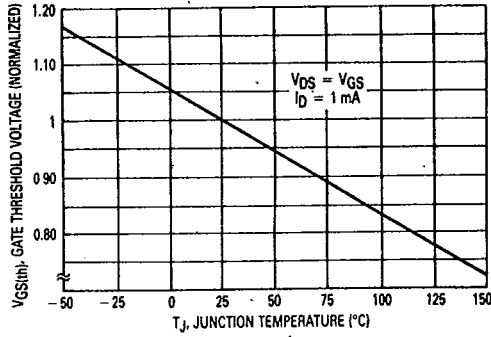


Figure 3. Transfer Characteristics

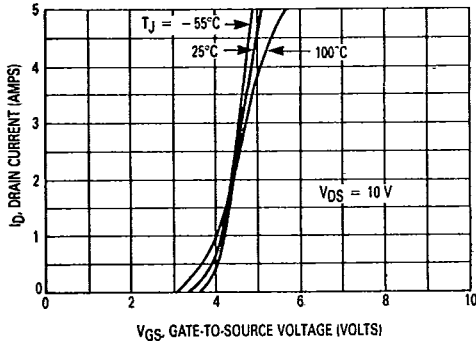


Figure 4. Breakdown Voltage Variation With Temperature

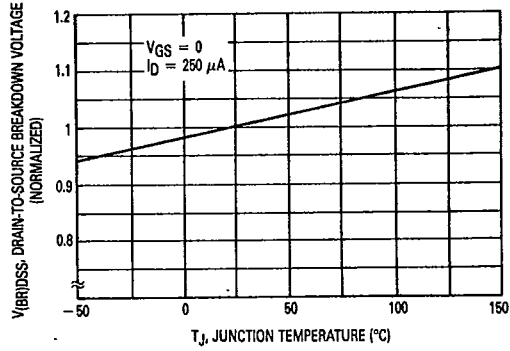


Figure 5. On-Resistance versus Drain Current

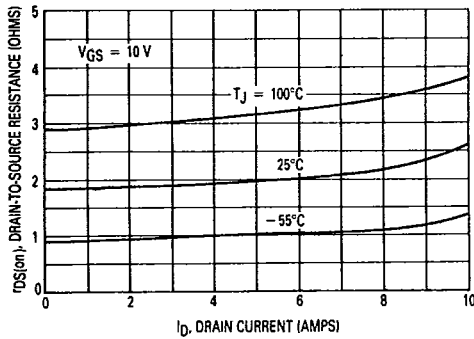
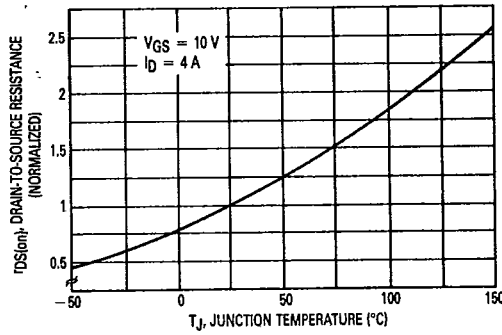


Figure 6. On-Resistance Variation With Temperature



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SAFE OPERATING AREA INFORMATION

Figure 7. Maximum Rated Forward Biased Safe Operating Area

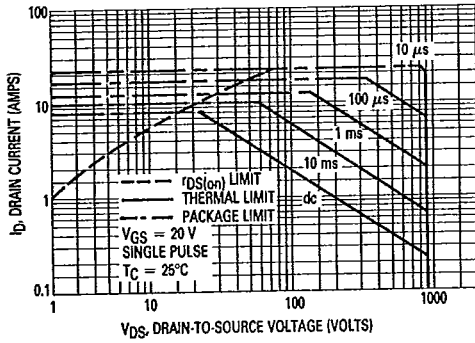
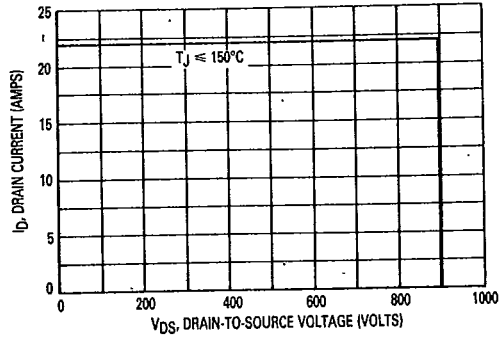


Figure 8. Maximum Rated Switching Safe Operating Area



FORWARD BIASED SAFE OPERATING AREA

The FBSOA curves define the maximum drain-to-source voltage and drain current that a device can safely handle when it is forward biased, or when it is on, or being turned on. Because these curves include the limitations of simultaneous high voltage and high current, up to the rating of the device, they are especially useful to designers of linear systems. The curves are based on a case temperature of 25°C and a maximum junction temperature of 150°C. Limitations for repetitive pulses at various case temperatures can be determined by using the thermal response curves. Motorola Application Note, AN569, "Transient Thermal Resistance-General Data and Its Use" provides detailed instructions.

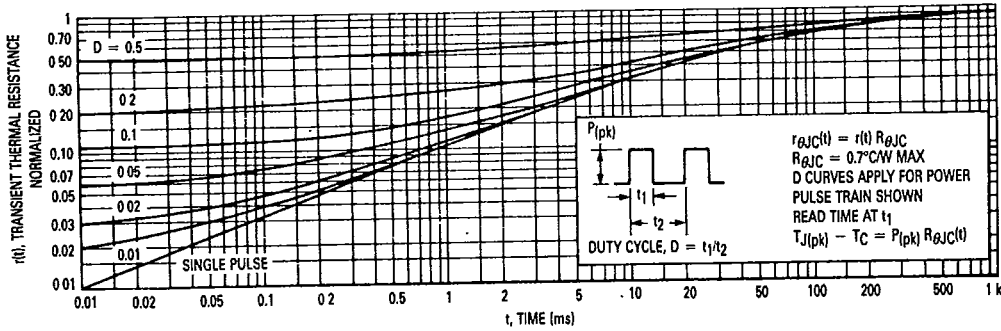
SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 8 is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, I_{DM} and the breakdown voltage, $V(BR)DSS$. The switching SOA shown in Figure 8 is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

The power averaged over a complete switching cycle must be less than:

$$\frac{T_{J(max)} - T_C}{R_{\theta JC}}$$

Figure 9. Thermal Response



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Figure 10. Capacitance Variation

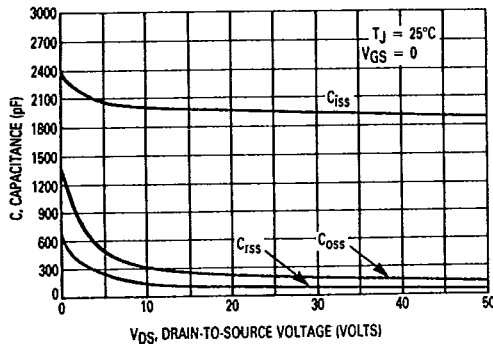
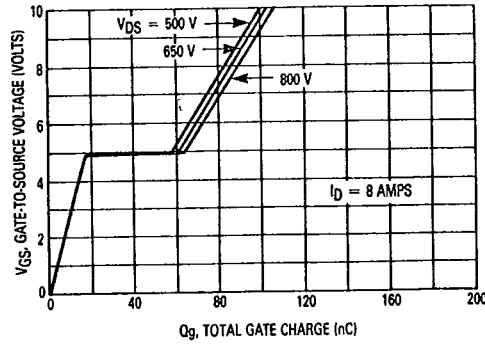


Figure 11. Gate Charge versus Gate-to-Source Voltage



RESISTIVE SWITCHING

Figure 12. Switching Test Circuit

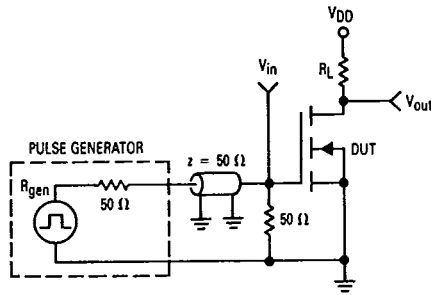


Figure 13. Switching Waveforms

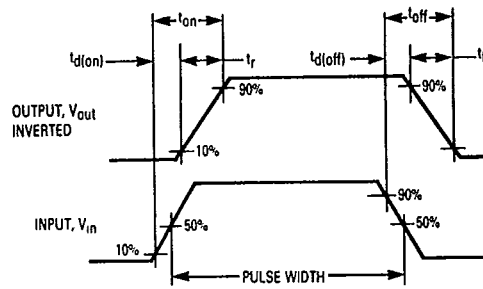


Figure 14. Gate Charge Test Circuit

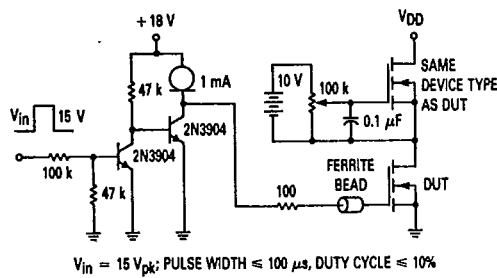


Figure 15. TMOS Diode Switching Test Circuit

NOTE: DUT is Shown as an N-Channel TMOS but can also be a P-Channel when appropriately connected. DUT Driver is the same device as DUT Diode (or Complement for P-Channel DUT Diode)

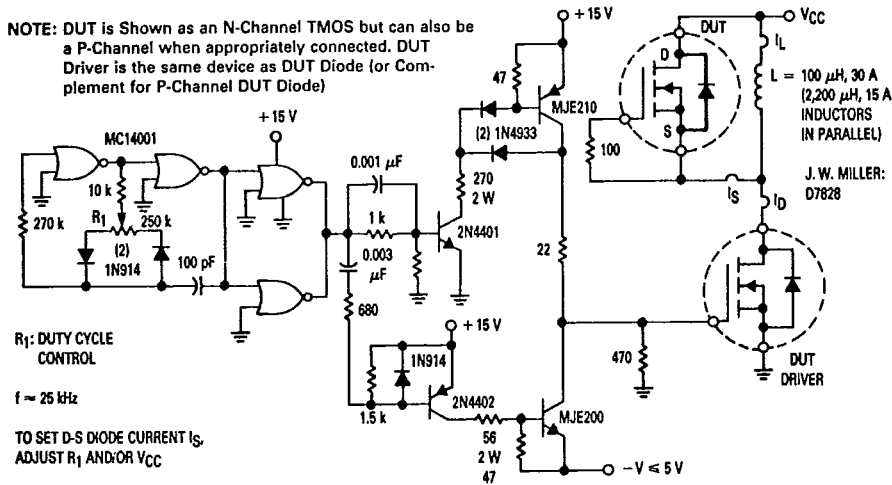
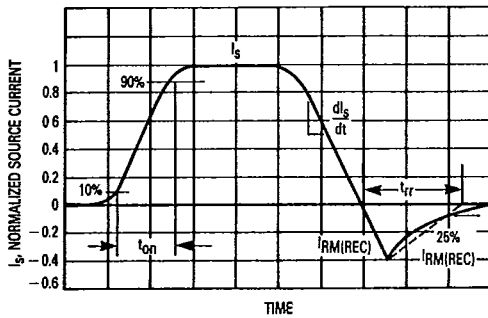


Figure 16. Diode Switching Waveform



OUTLINE DIMENSIONS

CASE 340-02 TO-218AC

STYLE 2:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	20.32	21.08	0.800	0.830
B	15.49	15.90	0.610	0.628
C	4.19	5.08	0.165	0.200
D	1.02	1.85	0.040	0.065
E	1.25	1.65	0.053	0.065
G	5.21	5.72	0.205	0.225
H	2.65	2.94	0.104	0.114
J	0.51	0.71	0.020	0.028
K	12.70	15.49	0.500	0.610
L	15.88	16.51	0.625	0.650
N	12.19	12.70	0.480	0.500
Q	4.04	4.22	0.159	0.166

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.