Product Preview

MC13191/D
Rev. 1.0, 05/2004

2.4 GHz, Low Power Transceiver

MOTOROLA intelligence everywhere™ | digital dna™

MC13191

(Scale 1:1)

Package Information
Plastic Package
Case 1311-03
(QFN-32)

Ordering Information

Device	Device Marking	Package
MC13191	13191	QFN-32

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The MC13191 is a short range, low power, 2.4 GHz band transceiver designed for low-cost, simple point-to-point and star network applications.

The MC13191 includes a complete packet modem capable of formatting data into packets with 125 byte payload. It has an over the air data rate of 250 kbps using O-QPSK modulation and Direct Sequence Spread Spectrum (DSSS) coding.

When combined with an appropriate microcontroller unit (MCU) as a baseband processor, the MC13191 provides a complete and cost effective wireless node for point to point and simple star network applications. Interface with the MCU is accomplished via a four wire serial peripheral interface (SPI) which allows interface to a variety of processors.

Applications include:

- Security - wireless security systems
- Medical/Personal Health Care - patient monitoring
- PC Peripherals - Human Interface Devices (HID) such as keyboards, mice, joysticks, etc.
- Toys - wireless and interactive toys
- Vertical proprietary applications

1 Features

- Recommended power supply range: 2.0 to 3.4 V
- 16 Channels
- 0 dBm (Typical), up to 3.6 dBm maximum output power
- Buffered Transmit and Receive Data Packets for Simplified Use with Low Cost Microcontrollers
- Supports 250 kbps O-QPSK Data in 2.0 MHz Channels and Full Spread-Spectrum Encode
- Link Quality and Energy Detect functions
- Three Power Down Modes for Power Conservation:
  - < 1 µA Off Current
  - 3.0 µA Typical Hibernate Current
  - 40 µA Typical Doze Current
- RX sensitivity of -91 dBm (Typical) at 1.0% Packet Error Rate
- Two internal timer comparators are available to reduce MCU resource requirements
- Clock output is available for use by MCU
- Seven General Purpose Input/Output ports (GPIO) are available
- Operating Temperature Range: -40°C to 85°C
- Small form factor QFN-32 Package:
  - Meets Moisture Sensitivity Level (MSL) 3
  - 260°C Peak Reflow temperature
  - Meets lead free requirements

2 Block Diagrams

Figure 1 shows a simplified block diagram of the MC13191. Figure 2 shows the basic system block diagram for the MC13191 in an application. Interface with the IC is accomplished through a 4-wire Serial Peripheral Interface (SPI). The application software resides on the host processor.

The host can be anything from a simple 8-bit device up to a sophisticated 32-bit processor depending on application requirements.

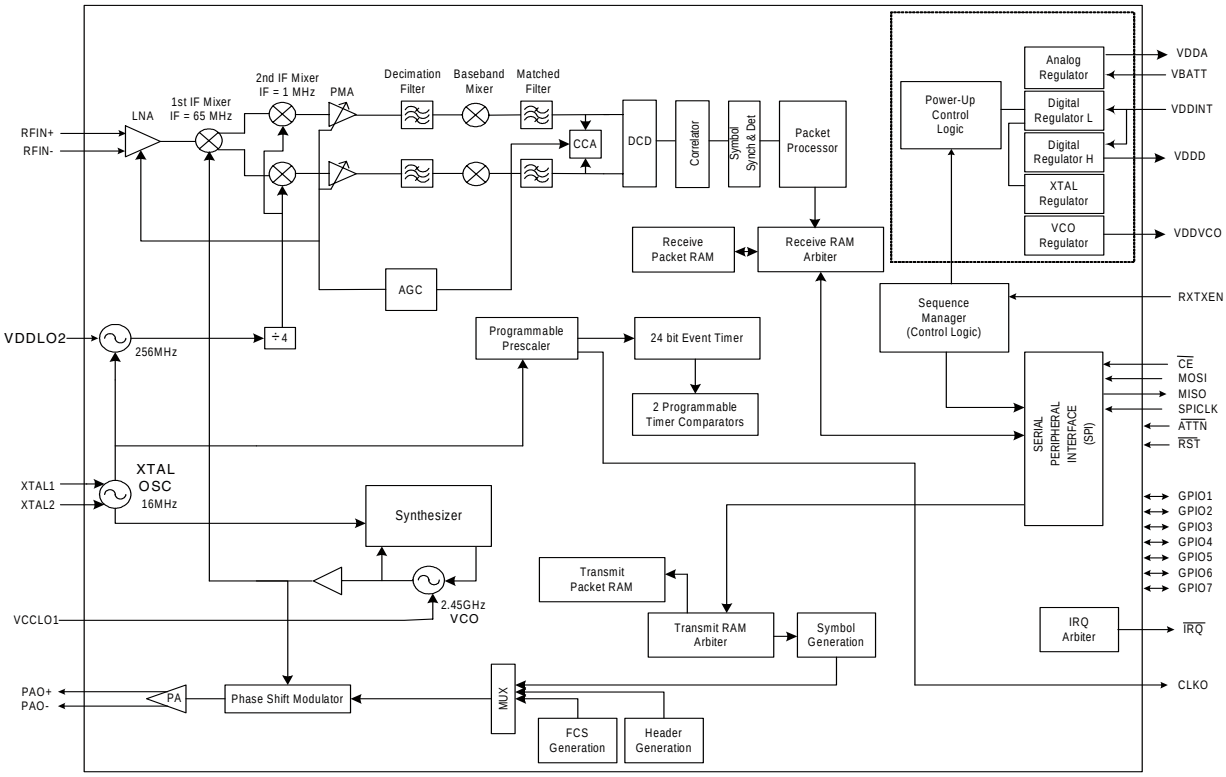

Figure 1. MC13191 Simplified Block Diagram

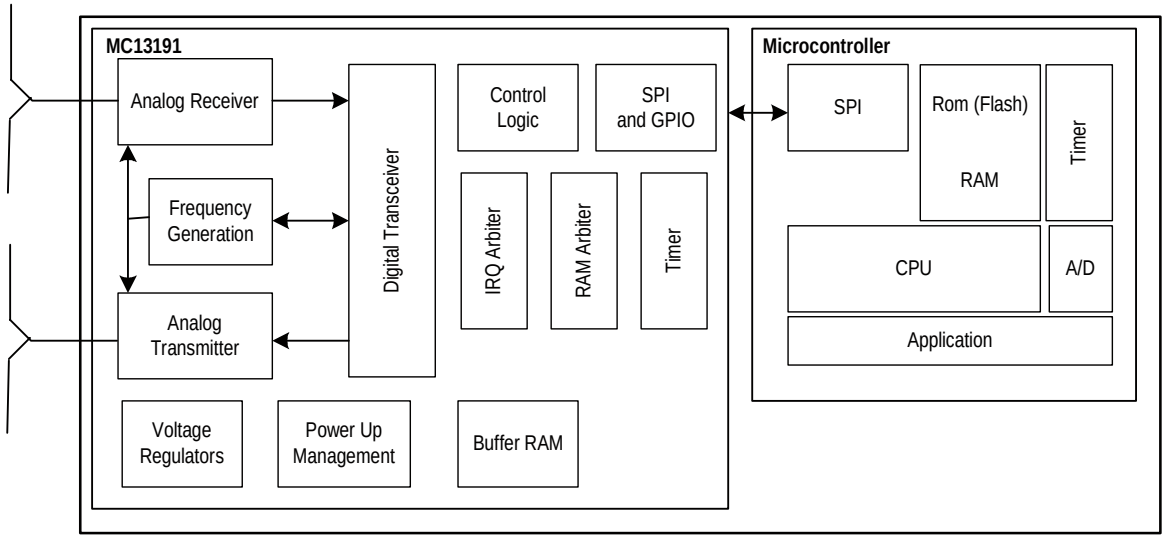

Figure 2. System Level Block Diagram

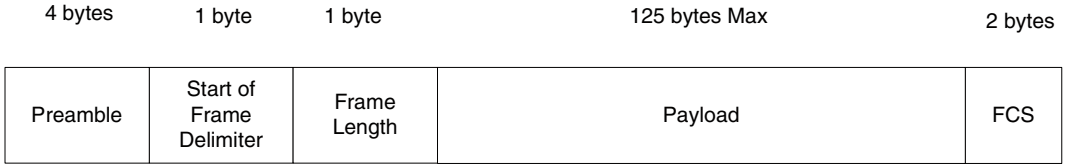

Figure 3. MC13191 Packet Structure

3 Theory of Operation

3.1 Packet Structure

Figure 3 shows the packet structure of the MC13191. Payloads of up to 125 bytes are supported. The MC13191 adds a four byte preamble, a one byte start of frame delimiter (SFD), and a one byte frame length indicator before the data. A Frame Check Sequence (FCS) is calculated and appended to the end of the data.

3.2 Receive Path Description

In the receive signal path, the RF input is converted to low IF In-phase and Quadrature (I & Q) signals through two down conversion stages. The digital back end “de-spreads” the Direct Sequence Spread Spectrum (DSSS) Offset QPSK (O-QPSK) signal, determines the symbols and packets, and detects the data. The preamble, SFD, and frame length are parsed and used. A two-byte FCS is calculated and compared to the FCS value appended to the transmitted data, generating a Cyclical Redundancy Check (CRC) result. Link Quality is measured over a 64 µs period after the packet preamble and stored in ROM.

The MC13191 processes incoming data as an entire packet. The MCU is notif1ied that an entire packet has been received via an interrupt.

3.3 Transmit Path Description

The transmit path functionality is the exact reverse of the receive path. The data stored in RAM is retrieved, formed into a packet, spread, and then up converted to the transmit frequency. Data is processed as an entire packet and is loaded into the TX buffer. The channel can be checked with the Energy Detect routine which loads a value into SPI. The MCU then requests that the MC13191 transmit the data. The MCU is notified that the packet has successfully been transmitted via an interrupt.

4 Electrical Characteristics

4.1 Maximum Ratings

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{BATT}, V_{DDINT}	3.6	Vdc
Junction Temperature	T_J	125	°C
Storage Temperature Range	T_{stg}	-55 to 125	°C

Note: Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the limits in the Electrical Characteristics or Recommended Operating Conditions tables.

Note: Meets Human Body Model (HBM) = 2 kV and Machine Model (MM) = 200 V except RFin = 100 V MM, PAout = 50 V MM & 1 kV HBM, and VBATT = 100 V MM. RF pins have no ESD protection including PAO + and PAO -.

4.2 Recommended Operating Conditions

Table 2. Recommended Operating Conditions

Characteristic	Symbol	Min	Typ	Max	Unit
Power Supply Voltage	V_{BATT}, V_{DDINT}	2.0	2.7	3.4	Vdc
Input Frequency	f_{in}	2.405	-	2.480	GHz
Ambient Temperature Range	T_A	-40	25	85	°C
Logic Input Voltage Low	V_{il}	0	-	30% V_{DDINT}	V
Logic Input Voltage High	V_{ih}	70% V_{DDINT}	-	V_{DDINT}	V
SPI Clock Rate	f_{SPI}	-	-	8.0	MHz
RF Input Power	P_{max}	-	-20	0	dBm
Crystal Reference Oscillator Frequency (±40 ppm over temperature range)	f_{ref}	16 MHz Only			

4.3 DC Electrical Characteristics

Table 3. DC Electrical Characteristics

(V_{CC} = 2.7 V, T_A = 25°C, unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Power Supply Current (V_{BATT} + V_{DDINT})	$I_{leakage}$				
Off	I_{CCH}	-	<1.0	-	µA
Hibernate	I_{CCD}	-	3.0	-	µA
Doze (No CLKO)	I_{CCI}	-	40	-	µA
Idle	I_{CCT}	-	500.0	-	µA
Transmit Mode	I_{CCR}	-	34	-	mA
Receive Mode		-	37	-	mA
Input Current Low (V_{in} = 0V)	I_{il}	-	-1.0	-	µA
Input Current High (V_{in} = V_{DDINT})	I_{ih}	-	1.0	-	µA
Output High Voltage	V_{oh}	80% V_{DDINT}	-	V_{DDINT}	V
Output Low Voltage	V_{ol}	0	-	20% V_{DDINT}	V

4.4 AC Electrical Characteristics

Table 4. Receiver AC Electrical Characteristics

Characteristic	Symbol	Min	Typ	Max	Unit
Sensitivity for 1% Packet Error Rate (PER)	$SENS_{per}$	-	-91	-	dBm
Saturation (maximum input level)	$SENS_{max}$	-	0	-	dBm
Adjacent Channel Interference for 1% PER (desired signal -82 dBm)		-	23	-	dB
Alternate Channel Interference for 1% PER (desired signal -82 dBm)		-	35	-	dB
Frequency Error Tolerance		-	-	200	kHz
Symbol Rate Error Tolerance		-	-	80	ppm
In-band Spurious Reception		-	28	-	dB

Table 5. Transmitter AC Electrical Characteristics

Characteristic	Symbol	Min	Typ	Max	Unit
Nominal Output Power	P_{out}	-	0	-	dBm
Error Vector Magnitude	EVM		27	45	%
Power Control Range		-	20	-	dB
Over the Air Data Rate	T_{bit}	-	250	-	kbps

5 Functional Description

5.1 MC13191 Operational States

The MC13191 has a number of operational states that allow for low-current operation. Entry from the Off to Idle state occurs when $\overline{RST}$ is de-asserted. Once in Idle, the SPI is active and controls the IC. Transition to Off, Hibernate, and Doze is controlled through the SPI. These states are summarized, along with the transition times, in Table 6. Current drain in the various states is listed in Table 3, DC Electrical Characteristics.

Table 6. MC13191 Mode Definitions and Transition Times

Mode	Definition	Transition Time To or From Idle
Off	All IC functions including SPI Off, Leakage only. $\overline{RST}$ asserted.	23.332 ms to Idle
Hibernate	Crystal Reference Oscillator Off, SPI not functional. IC Responds to $\overline{ATTN}$.	18.332 ms to Idle
Doze	Crystal Reference Oscillator On but CLKO output available only if Register 7, Bit 9 = 1 for frequencies of 1 MHz or less, SPI not functional. Responds to $\overline{ATTN}$ and can be programmed to enter Idle State through an internal timer comparator.	332 µs to Idle
Idle	Crystal Reference Oscillator On with CLKO output available. SPI active.	
Receive	Crystal Reference Oscillator On. Receiver On. SPI should not be accessed.	144 µs from Idle
Transmit	Crystal Reference Oscillator On. Transmitter On. SPI should not be accessed.	144 µs from Idle

5.2 Serial Peripheral Interface (SPI)

Control of the MC13191 and data transfers are accomplished by means of a 4-wire Serial Peripheral Interface (SPI). This section details the operation of the SPI.

5.2.1 General

The MC13191 operates as a slave device only. Data to be written into the IC is presented on the Master Out/Slave In (MOSI) pin of the device, while data read from the device is presented to the master device on the Master In/Slave Out (MISO) pin. Synchronization of the data is accomplished by the return-to-zero Serial Clock (SPICLK) input and is framed by the Chip Enable ($\overline{CE}$) pin. Data on MOSI is always clocked into the IC on the leading edge of SPICLK and data is clocked out of the IC at MISO on the falling edge of SPICLK. The master device should transfer MISO data to its internal registers on the trailing edge of SPICLK. A typical interconnection to a microprocessor is illustrated in Figure 4.

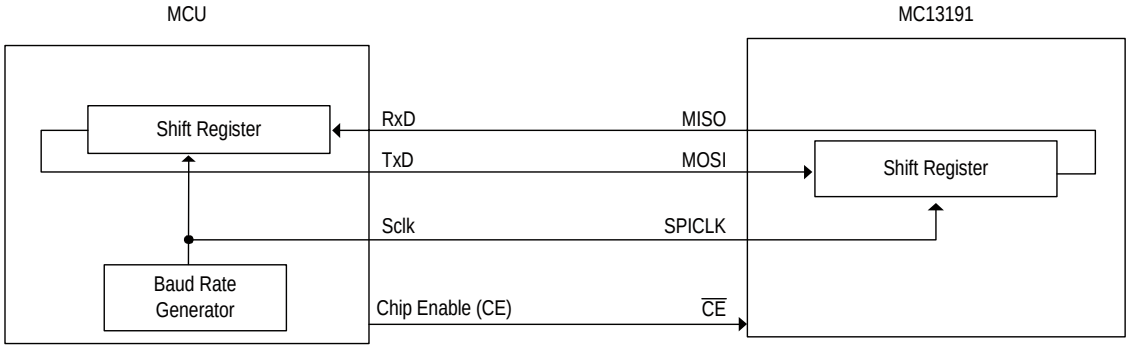

Figure 4. SPI Interface

MISO is programmable through SPI to be either high impedance (default) or low impedance when $\overline{CE}$ is negated.

Although the SPI is fully static, internal memory, timer and interrupt arbiters require an internal clock, CLK_{core}, derived from the crystal reference oscillator, to communicate from the SPI registers to internal registers and memory.

Figure 5 and Table 7 show the SPI timing diagram and timing specifications.

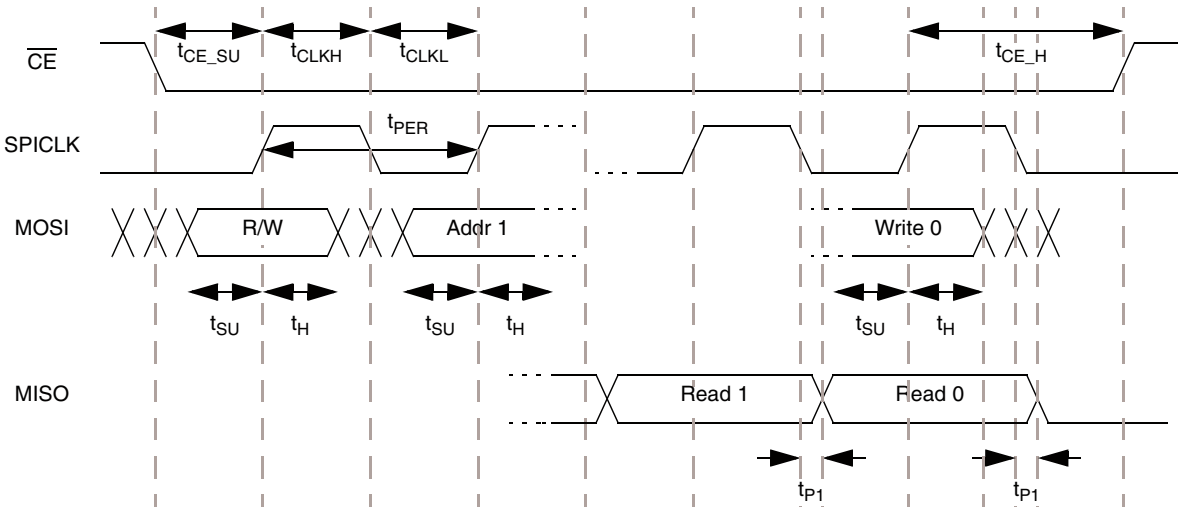

Figure 5. SPI Parametric Timing Diagram.

Table 7. SPI Parametric Timing Specifications

Symbol	Parameter	Min	Typ	Max	Unit
$1/t_{PER}$	SPICLK frequency			8.0	MHz
t_{CLKH}	Pulse Width, SPICLK high		0.5 * t_{PER}		ns
t_{CLKL}	Pulse Width, SPICLK low		0.5 * t_{PER}		ns
t_{CE_SU}	Setup Time, $\overline{CE}$ low to rising SPICLK		0.5 * t_{PER}		ns
t_{CE_H}	Hold Time, rising SPICLK to $\overline{CE}$ high	1.0 * t_{PER}			ns
t_{SU}	Setup Time, MOSI to rising SPICLK		0.5 * t_{PER}		ns
t_H	Hold Time, MOSI to rising SPICLK		0.5 * t_{PER}		ns
t_{P1}	Propagation Delay, MISO to rising SPICLK	0			ns
t_{P2}	Propagation Delay, MISO to rising $\overline{CE}$	0			ns

NOTE:

The minimum duration of a singular SPI access, at the maximum SPICLK rate of 8 MHz is 3.0µs.

6 Contact Connections

Table 8. Contact Function Description

Contact #	Contact Name	Type	Description	Functionality
1	RFIN-	RF Input	LNA negative differential input	2.4 to 2.5 GHz
2	RFIN+	RF Input	LNA positive differential input	2.4 to 2.5 GHz
3	Not Used		Tie to Ground	
4	Not Used		Tie to Ground	
5	PAO+	RF Output /DC Input	Power Amplifier Positive Output. Open drain. Connect to V_{DDA}.	2.4 to 2.5 GHz
6	PAO-	RF Output/DC Input	Power Amplifier Negative Output. Open drain. Connect to V_{DDA}.	2.4 to 2.5 GHz
7	Not used		Tie to Ground	
8	GPIO4	Digital Input/ Output	General Purpose Input/Output 4.	**When digital output:** Vol= 20%VDDINT Voh=80%VDDINT **When digital input:** Vil= 30%VDDINT Vih=70%VDDINT 1 mA max source/ sink.
9	GPIO3	Digital Input/ Output	General Purpose Input/Output 3	**When digital output:** Vol= 20%VDDINT Voh=80%VDDINT **When digital input:** Vil= 30%VDDINT Vih=70%VDDINT 1 mA max source/ sink.
10	GPIO2	Digital Input/ Output	General Purpose Input/Output 2.	**When digital output:** Vol= 20%VDDINT Voh=80%VDDINT **When digital input:** Vil= 30%VDDINT Vih=70%VDDINT 1 mA max source/ sink.

Table 8. Contact Function Description (Continued)

Contact #	Contact Name	Type	Description	Functionality
11	GPIO1	Digital Input/ Output	General Purpose Input/Output1.	**When digital output:** Vol= 20%VDDINT Voh=80%VDDINT **When digital input:** Vil= 30%VDDINT Vih=70%VDDINT 1 mA max source/ sink.
12	$\overline{\text{RST}}$	Digital Input	Active Low Reset Pin. While held low, the IC is “off” and all internal information is lost from RAM and SPI registers. When high, IC goes to IDLE State, with SPI in default state.	Vil= 30%VDDINT Vih=70%VDDINT
13	RXTXEN	Digital Input	Active High. Low to high transition initiates RX or TX sequence depending on SPI setting. If held high (e.g., tied to VBATT), SPI setting start RX or TX sequence.	Vil= 30%VDDINT Vih=70%VDDINT
14	$\overline{\text{ATTN}}$	Digital Input	Active Low Attention pin. Transitions IC from either Hibernate or Doze states to Idle.	Vil=30%VDDINT Vih=70%VDDINT
15	CLKO	Digital Output	Clock output to host CPU. Programmable frequencies of: 16, 8, 4, 2, 1 MHz, and 62.5 kHz, 32.786+ kHz (default), and 16.393+ kHz	Vol= 20%VDDINT Voh=80%VDDINT freq=16MHz (20/80 DC) 20 pF. All others (50/50 DC)
16	SPICLK	Digital Clock Input	External clock input for the SPI interface.	Vil= 30%VDDINT Vih=70%VDDINT freq= 8 MHz (max)
17	MOSI	Digital Input	Master Out/Slave In. Dedicated SPI data input.	Vil= 30%VDDINT Vih=70%VDDINT freq=8 Mbps (max)
18	MISO	Digital Output	Master In/Slave Out. Dedicated SPI data output.	Vol= 20%VDDINT Voh=80%VDDINT 1 mA max source/ sink.
19	$\overline{\text{CE}}$	Digital Input	Active Low Chip Enable. Activates SPI.	Vil= 30%VDDINT Vih=70%VDDINT
20	$\overline{\text{IRQ}}$	Digital Output	Active Low Interrupt Request	Open drain device. 40 kΩ internal pull-up. Interrupt can be serviced every 6 µs with <20 pF load. External pull-up must be >4 kΩ.

Table 8. Contact Function Description (Continued)

Contact #	Contact Name	Type	Description	Functionality
21	VDDD	Bypass	Digital supply bypass	Decouple 0.1 to 0.47 µF to ground.
22	VDDINT	Input	Digital interface supply & digital regulator input – Connect to Battery	2.0 to 3.4 V Decouple 0.47 to 1 µF to ground.
23	GPIO5	Digital Input/ Output	General Purpose Input/Output 5	**When digital output:** Vol= 20%VDDINT Voh=80%VDDINT **When digital input:** Vil= 30%VDDINT Vih=70%VDDINT 1 mA max source/ sink.
24	GPIO6	Digital Input/ Output	General Purpose Input/Output 6	**When digital output:** Vol= 20%VDDINT Voh=80%VDDINT **When digital input:** Vil= 30%VDDINT Vih=70%VDDINT 1 mA max source/ sink.
25	GPIO7	Digital Input/ Output	General Purpose Input/Output 7	**When digital output:** Vol= 20%VDDINT Voh=80%VDDINT **When digital input:** Vil= 30%VDDINT Vih=70%VDDINT 1 mA max source/ sink.
26	XTAL1	Input	Crystal Reference oscillator input	Connect to 16 MHz crystal and load capacitor
27	XTAL2	Output	Crystal Reference oscillator output	Connect to 16 MHz crystal and load capacitor
28	VDDLO2	Input/Bypass	LO2 VDD supply - Connect to VDDA externally	Decouple 100 to 1000 pF to ground
29	VDDLO1	Input/Bypass	LO1 VDD supply pad - Connect to VDDA externally	Decouple 100 to 1000 pF to ground
30	VDDVCO	Bypass	VCO regulated supply bypass	Decouple 100 to 1000 pF to ground

Table 8. Contact Function Description (Continued)

Contact #	Contact Name	Type	Description	Functionality
31	VBATT	Input	Analog voltage regulators Input - Connect to Battery	Decouple 1 µF and 100 pF ground
32	VDDA	Output	Analog regulated supply Output – Connect to VDDLO1 and VDDLO2 externally	Decouple 100 to 1000 pF to ground
EP	Ground		External paddle / flag ground	Connect to ground

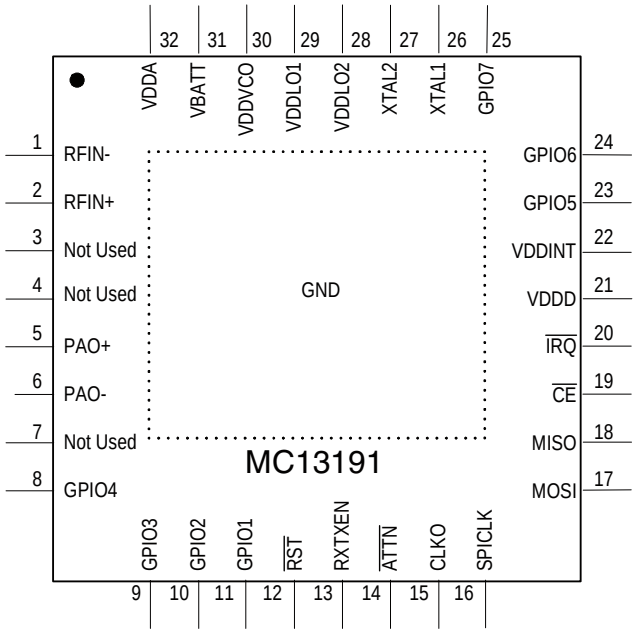

Figure 6. Contact Connections (Top View)

7 Applications Information

Figure 7 shows a basic application schematic for interfacing the MC13191 with an MCU. Table 9 lists the Bill of Materials.

The MC13191 has differential RF inputs and outputs. These are well suited to balanced PCB antenna structures. Alternatively, chip antennas or other single-ended structures can be used with commercially available chip baluns or microstrip equivalents. PAO+ and PAO- require connection to VDDA, the analog regulator output. This is best accomplished with microstrip lines which are decoupled to act as harmonic traps. The 16 MHz crystal should be mounted close to the MC13192 because the crystal trim default assumes the listed Toyocom crystal and the 9 pF capacitors shown are used. If a different crystal is used, it should have a load capacitance of 9 pF or less. Bypassing capacitors are critical and should be placed close to the device. Unused GPIOs and contacts should be grounded as shown.

The SPI connections to the MCU include $\overline{\text{IRQ}}$, $\overline{\text{CE}}$, MOSI, MISO and SPICLK. The SPI can run at any frequency of 8 MHz or less. Optionally, CLKO can provide a clock to the MCU. The CLKO frequency is programmable via the SPI and has a default of 32.786+ kHz. The $\overline{\text{ATTN}}$ line can be driven by a GPIO from the MCU or can be negated by a switch or other hardware. The latter approach allows the MCU to be put in a sleep mode and then awakened by CLKO when the $\overline{\text{ATTN}}$ line wakes up the MC13191. RXTXEN can be used to initiate receive or transmit sequences under MCU control. In this case, RXTXEN must be controlled by an MCU GPIO with the optional connection shown. Otherwise, RXTXEN is held high and receive or transmit sequences are initiated by an SPI command. Device reset ($\overline{\text{RST}}$) can be controlled through an optional connection to an MCU GPIO or by an external pull-down.

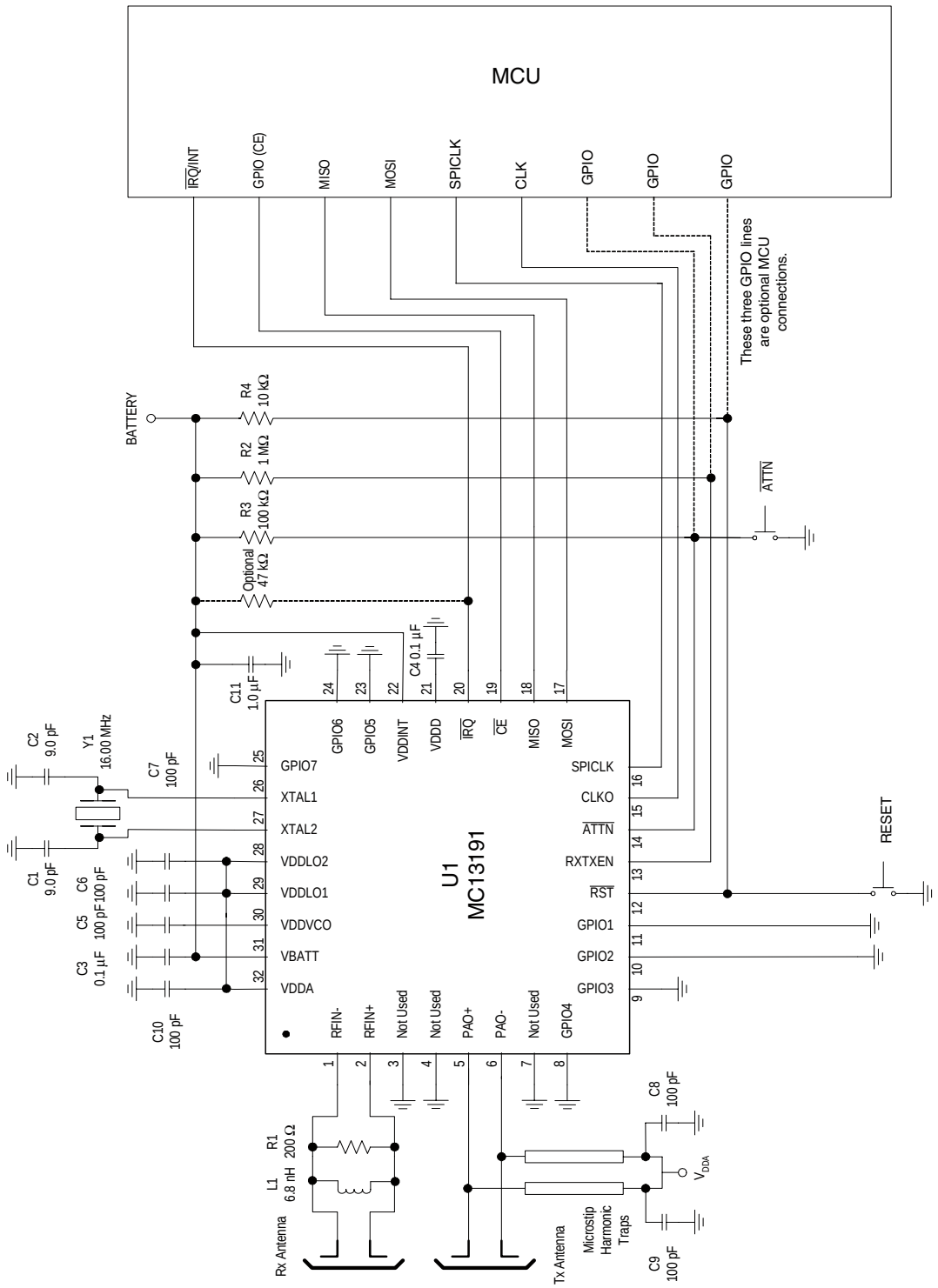

Figure 7. MC13191 Applied With an MCU

Table 9. MC13191 to MCU Bill of Materials (BOM)

Item Number	Label/Value	Attributes	Designation
1	9 pF	SMD0201	C1
2	9 pF	SMD0201	C2
3	0.1 uF	SMD0201	C3
4	0.1 uF	SMD0201	C4
5	100 pF	SMD0201	C5
6	100 pF	SMD0201	C6
7	100 pF	SMD0201	C7
8	100 pF	SMD0201	C8
9	100 pF	SMD0201	C9
10	100 pF	SMD0201	C10
11	1.0 uF	SMD0201	C11
12	6.8 nH	SMD0201	L1
13	200 Ω	SMD0201	R1
14	1 MΩ	SMD0201	R2
15	100 kΩ	SMD0201	R3
16	10 kΩ	SMD0201	R4
17	MC13191	QFN	U1
18	16.000 MHz	TOYOCOM TSX-10A, 9 pF load	Y1

8 Packaging Information

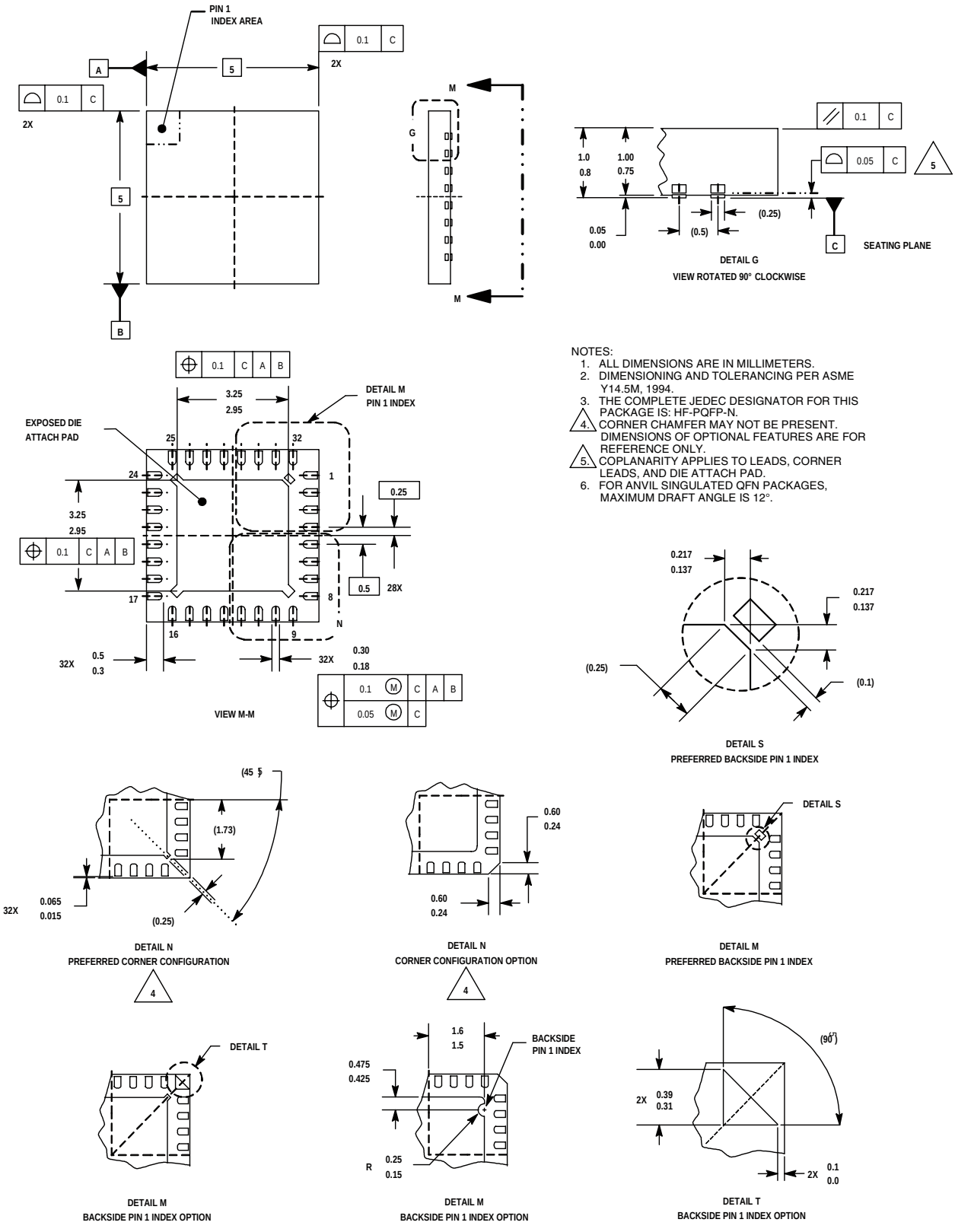

Figure 8. Outline Dimensions for QFN-32, 5x5 mm (Case 1311-03, Issue E)

NOTES

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