19-2828; Rev 0; 4/03

MAXIM

Programmable DC-Balance 21-Bit Serializers

General Description

The MAX9209/MAX9211/MAX9213/MAX9215 serialize 21 bits of LVTTL/LVCMOS parallel input data to three LVDS outputs. A parallel rate clock on a fourth LVDS output provides timing for deserialization.

The MAX9209/MAX9211/MAX9213/MAX9215 feature programmable DC balance, which allows isolation between the serializer and deserializer using AC-coupling. The DC balance circuits on each channel code the data, limiting the imbalance of transmitted ones and zeros to a defined range. The companion MAX9210/MAX9212/MAX9214/MAX9216 deserializers decode the data. When DC balance is not programmed, the serializers are compatible with non-DC-balanced, 21-bit serializers like the DS90CR215 and DS90CR217.

Two frequency ranges and two DC-balance default conditions are available for maximum replacement flexibility and compatibility with existing non-DC-balanced serializers.

The MAX9209/MAX9211/MAX9213/MAX9215 are available in TSSOP and space-saving thin QFN packages, and operate from a single +3.3V supply over the -40°C to +85°C temperature range.

Applications

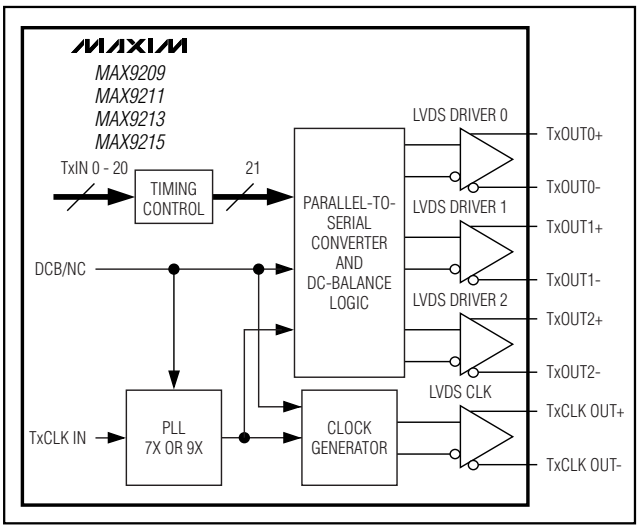
Automotive Navigation Systems

Automotive DVD Entertainment Systems

Digital Copiers

Laser Printers

Functional Diagram



Pin Configurations appear at end of data sheet.

Features

- **Programmable DC-Balanced or Non-DC-Balanced Operation**
- **DC Balance Allows AC-Coupling for Ground-Shift Tolerance**
- **As Low as 8MHz Operation**
- **Pin Compatible with DS90CR215 and DS90CR217 in Non-DC-Balanced Mode**
- **Integrated 110Ω (DC-Balanced) and 410Ω (Non-DC-Balanced) Output Resistors**
- **5V Tolerant LVTTL/LVCMOS Data Inputs**
- **PLL Requires No External Components**
- **Up to 1.785Gbps Throughput**
- **LVDS Outputs Meet IEC 61000-4-2 Level 4 ESD Requirements**
- **LVDS Outputs Conform to ANSI TIA/EIA-644 LVDS Standard**
- **Low-Profile 48-Lead TSSOP and Space-Saving QFN Packages**
- **-40°C to +85°C Operating Temperature Range**
- **+3.3V Supply**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX9209ETM*	-40°C to +85°C	48 Thin QFN-EP**
MAX9209EUM*	-40°C to +85°C	48 TSSOP
MAX9211ETM*	-40°C to +85°C	48 Thin QFN-EP**
MAX9211EUM*	-40°C to +85°C	48 TSSOP
MAX9213ETM*	-40°C to +85°C	48 Thin QFN-EP**
MAX9213EUM	-40°C to +85°C	48 TSSOP
MAX9215ETM*	-40°C to +85°C	48 Thin QFN-EP**
MAX9215EUM*	-40°C to +85°C	48 TSSOP

**Future product—contact factory for availability.*

***EP = Exposed pad.*

For pricing, delivery, and ordering information, please contact Maxim/Dallas Direct! at 1-888-629-4642, or visit Maxim's website at www.maxim-ic.com.

Programmable DC-Balance 21-Bit Serializers

ABSOLUTE MAXIMUM RATINGS

V_{CC} to GND .....-0.5V to +4.0V
LVDS Outputs (TxOUT_, TxCLK OUT_) to GND ...-0.5V to +4.0V
5V Tolerant LVTTL/LVCMOS Inputs
(TxIN_, TxCLK IN, $\overline{PWRDWN}$) to GND .....-0.5V to +6.0V
(DCB/NC) to GND .....-0.5V to (V_{CC} + 0.5V)
LVDS Outputs (TxOUT_, TxCLK OUT_)
Short to GND and Differential Short .....Continuous
Continuous Power Dissipation (T_A = +70°C)
48-Pin TSSOP (derate 16mW/°C above +70°C) 1282mW
48-Lead QFN (derate 26.3mW/°C above +70°C) 2105mW
Storage Temperature Range .....-65°C to +150°C
Junction Temperature .....+150°C
ESD Protection Human Body Model
(R_D = 1.5kΩ, C_S = 100pF)
All Pins .....±2kV
IEC 61000-4-2 Level 4 (R_D = 330Ω, C_S = 150pF)
Contact Discharge LVDS Outputs
(TxOUT_, TxCLK OUT_) .....±8kV
Air-Grap Discharge LVDS Outputs
(TxOUT_, TxCLK OUT_) .....±15kV
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = +3.0V to +3.6V, R_L = 100Ω ±1%, $\overline{PWRDWN}$ = high, DCB/NC = high or low, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{CC} = +3.3V, T_A = +25°C.) (Notes 1, 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SINGLE-ENDED INPUTS (TxIN_, TxCLK IN, $\overline{PWRDWN}$, DCB/NC)						
High-Level Input Voltage	V_{IH}	TxIN_, TxCLK IN, $\overline{PWRDWN}$	2.0		5.5	V
		DCB/NC	2.0		V_{CC} + 0.3	
Low-Level Input Voltage	V_{IL}		-0.3		+0.8	V
Input Current	I_{IN}	V_{IN} = high or low, $\overline{PWRDWN}$ = high or low	-20		+20	µA
Input Clamp Voltage	V_{CL}	I_{CL} = -18mA		-0.9	-1.5	V
LVDS OUTPUTS (TxOUT_, TxCLK OUT)						
Differential Output Voltage	V_{OD}	Figure 1	250	350	450	mV
Change in V_{OD} Between Complementary Output States	ΔV_{OD}	Figure 1		2	25	mV
Output Offset Voltage	V_{OS}	Figure 1	1.125	1.25	1.375	V
Change in V_{OS} Between Complementary Output States	ΔV_{OS}	Figure 1		10	30	mV
Output Short-Circuit Current	I_{OS}	V_{OUT+} or V_{OUT-} = 0V or V_{CC}, non-DC-balanced mode	-10	±5.7	+10	mA
		V_{OUT+} or V_{OUT-} = 0V or V_{CC}, DC-balanced mode	-15	±8.2	+15	
Magnitude of Differential Output Short-Circuit Current	I_{OSD}	V_{OD} = 0V, non-DC-balanced mode (Note 3)		5.7	10	mA
		V_{OD} = 0V, DC-balanced mode (Note 3)		8.2	15	
Differential Output Resistance	R_O	DC-balanced mode	78	110	147	Ω
		Non-DC-balanced mode	292	410	547	
Output High-Impedance Current	I_{OZ}	$\overline{PWRDWN}$ = low or V_{CC} = 0V, V_{OUT+} = 0V or 3.6V, V_{OUT-} = 0V or 3.6V	-0.5	±0.1	+0.5	µA

DC ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +3.0V to +3.6V, R_L = 100Ω ±1%, $\overline{PWRDWN}$ = high, DCB/NC = high or low, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{CC} = +3.3V, T_A = +25°C.) (Notes 1, 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Worst-Case Supply Current	I_{CCW}	MAX9213/MAX9215 worst-case pattern, C_L = 5pF, Figure 2	16MHz, DC balanced		46	64	mA
			34MHz, DC balanced		59	87	
			66MHz, DC balanced		94	108	
			20MHz, Non-DC balanced		36	49	
			33MHz, Non-DC balanced		45	62	
			40MHz, Non-DC balanced		49	70	
			66MHz, Non-DC balanced		68	89	
			85MHz, Non-DC balanced		83	100	
Power-Down Supply Current	I_{CCZ}	$\overline{PWRDWN}$ = low			17	50	µA

AC ELECTRICAL CHARACTERISTICS

(V_{CC} = +3.0V to +3.6V, R_L = 100Ω ±1%, C_L = 5pF, $\overline{PWRDWN}$ = high, DCB/NC = high or low, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{CC} = +3.3V, T_A = +25°C.) (Notes 4, 5)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
LVDS Low-to-High Transition Time	LLHT	Figure 3		150	260	350	ps
LVDS High-to-Low Transition Time	LHLT	Figure 3		150	260	350	ps
TxCLK IN Transition Time	TCIT	Figure 4				4	ns
Output Pulse Position	TPPosN	N = 0, 1, 2, 3, 4, 5, 6; non-DC-balanced mode, Figure 6 (Note 6), MAX9213/MAX9215	20MHz	N/7 x TCIP - 0.25	N/7 x TCIP	N/7 x TCIP + 0.25	ns
			40MHz	N/7 x TCIP - 0.15	N/7 x TCIP	N/7 x TCIP + 0.15	
			85MHz	N/7 x TCIP - 0.1	N/7 x TCIP	N/7 x TCIP + 0.1	
		N = 0, 1, 2, 3, 4, 5, 6, 7, 8; DC-balanced mode, Figure 6 (Note 6), MAX9213/MAX9215	16MHz	N/9 x TCIP - 0.25	N/9 x TCIP	N/9 x TCIP + 0.25	
			34MHz	N/9 x TCIP - 0.15	N/9 x TCIP	N/9 x TCIP + 0.15	
			66MHz	N/9 x TCIP - 0.1	N/9 x TCIP	N/9 x TCIP + 0.1	

Programmable DC-Balance 21-Bit Serializers

AC ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +3.0V to 3.6V, R_L = 100Ω ±1%, C_L = 5pF, $\overline{PWRDWN}$ = high, DCB/NC = high or low, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{CC} = +3.3V, T_A = +25°C.) (Notes 4, 5)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
TxCLK IN High Time	TCIH	Figure 7	0.3 x TCIP		0.7 x TCIP	ns
TxCLK IN Low Time	TCIL	Figure 7	0.3 x TCIP		0.7 x TCIP	ns
TxIN to TxCLK IN Setup	TSTC	Figure 7	2.2			ns
TxIN to TxCLK IN Hold	THTC	Figure 7	0			ns
TxCLK IN to TxCLK OUT Delay	TCCD	Non-DC-balanced mode, Figure 8	3.5	4.5	6.0	ns
		DC-balanced mode, Figure 8	4.7	5.9	7.2	
Serializer Phase-Locked Loop Set	TPLLS	Figure 9			32800 x TCIP	ns
Serializer Power-Down Delay	TPDD	Figure 10		14	50	ns
TxCLK IN Cycle-to-Cycle Jitter (Input Clock Requirement)	TJIT				2	ns
Magnitude of Differential Output Voltage	V_{OD}	595Mbps data rate, worst-case pattern	250			mV

Note 1: Current into a pin is defined as positive. Current out of a pin is defined as negative. All voltages are referenced to ground except V_{OD} , ΔV_{OD}, and ΔV_{OS}.

Note 2: Maximum and minimum limits over temperature are guaranteed by design and characterization. Devices are production tested at T_A = +25°C.

Note 3: Guaranteed by design.

Note 4: TCIP is the period of TxCLK IN.

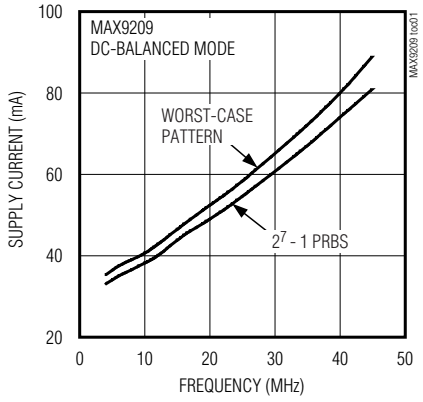
Note 5: AC parameters are guaranteed by design and characterization, and are not production tested. Limits are set at ±6 sigma.

Note 6: Pulse position TPPosN is characterized using 2^7 - 1 PRBS data.

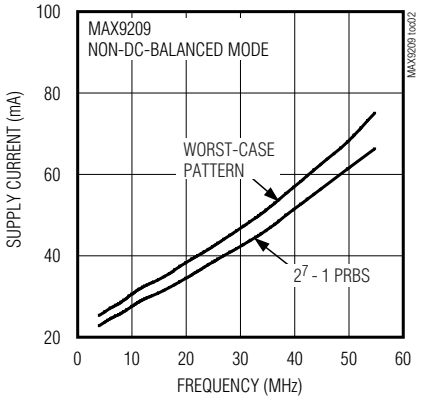
Typical Operating Characteristics

(V_{CC} = +3.3V, R_L = 100Ω ±1%, C_L = 5pF, $\overline{PWRDWN}$ = high, T_A = +25°C, unless otherwise noted.)

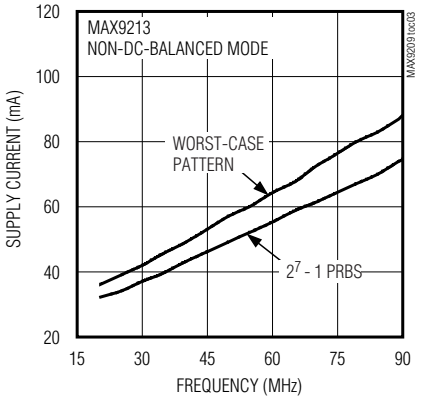
WORST-CASE PATTERN AND PRBS SUPPLY CURRENT vs. FREQUENCY



WORST-CASE PATTERN AND PRBS SUPPLY CURRENT vs. FREQUENCY



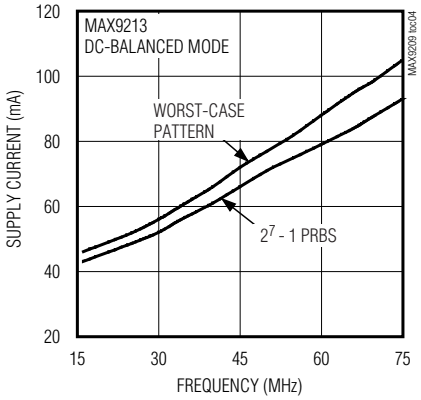
WORST-CASE AND PRBS SUPPLY CURRENT vs. FREQUENCY



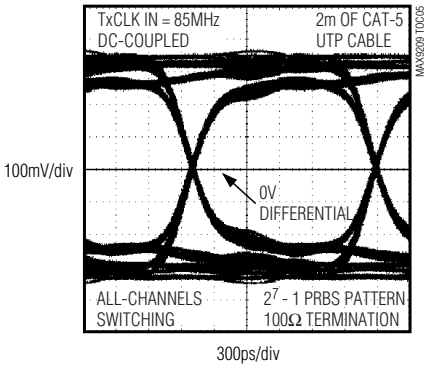
Typical Operating Characteristics (continued)

(V_{CC} = +3.3V, R_L = 100Ω ±1%, C_L = 5pF, $\overline{PWRDWN}$ = high, T_A = +25°C, unless otherwise noted.)

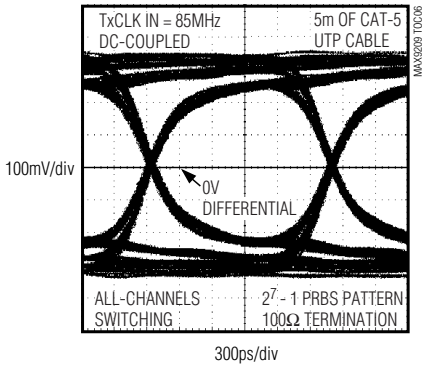
WORST-CASE PATTERN AND PRBS SUPPLY CURRENT vs. FREQUENCY



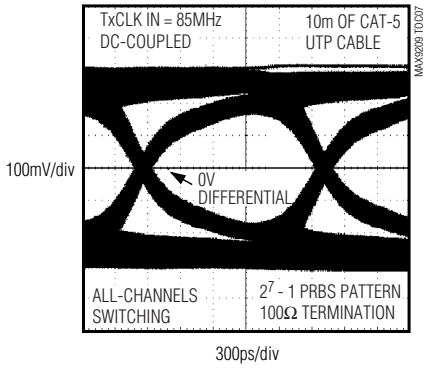
MAX9213 EYE DIAGRAM—NON-DC-BALANCED MODE



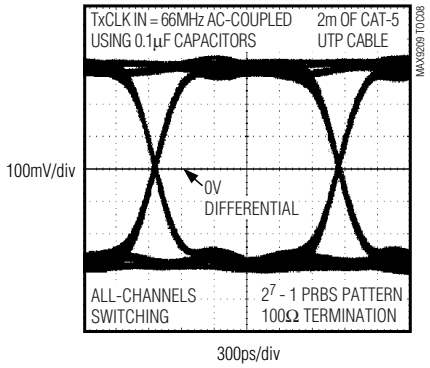
MAX9213 EYE DIAGRAM—NON-DC-BALANCED MODE



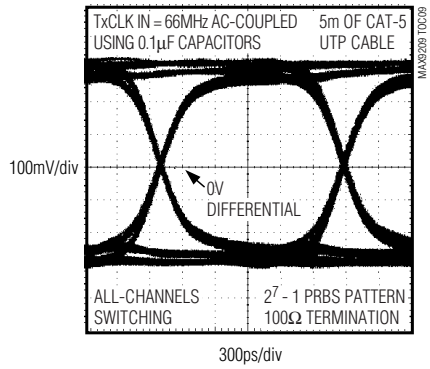
MAX9213 EYE DIAGRAM—NON-DC-BALANCED MODE



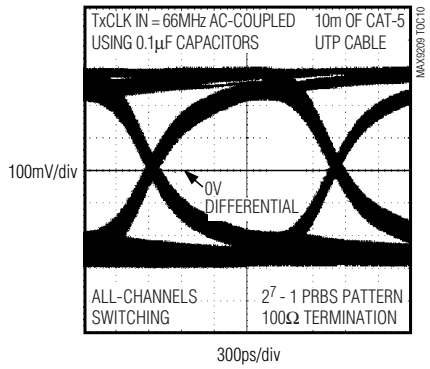
MAX9213 EYE DIAGRAM—DC-BALANCED MODE



MAX9213 EYE DIAGRAM—DC-BALANCED MODE



MAX9213 EYE DIAGRAM—DC-BALANCED MODE



Programmable DC-Balance 21-Bit Serializers

Pin Description

PIN		NAME	FUNCTION
TSSOP	QFN		
1, 3, 4, 44, 45, 47, 48,	38, 39, 41, 42, 43, 45, 46	TxIN0–TxIN6	5V Tolerant LVTTL/LVCMOS Channel 0 Data Inputs. Internally pulled down to GND.
2, 8, 14, 21	2, 8, 15, 44	V_{CC}	Digital Supply Voltage
5, 11, 17, 24, 46	5, 11, 18, 40, 47	GND	Ground
6, 7, 9, 10, 12, 13, 15	1, 3, 4, 6, 7, 9, 48	TxIN7–TxIN13	5V Tolerant LVTTL/LVCMOS Channel 1 Data Inputs. Internally pulled down to GND.
16, 18, 19, 20, 22, 23, 25	10, 12, 13, 14, 16, 17, 19	TxIN14–TxIN20	5V Tolerant LVTTL/LVCMOS Channel 2 Data Inputs. Internally pulled down to GND.
26	20	TxCLK IN	5V Tolerant LVTTL/LVCMOS Parallel Rate Clock Input. Internally pulled down to GND.
27	21	$\overline{PWRDWN}$	5V Tolerant LVTTL/LVCMOS Power-Down Input. Internally pulled down to GND. Outputs are high impedance when $\overline{PWRDWN}$ = low or open.
28, 30	22, 24	PLL GND	PLL Ground
29	23	PLL V_{CC}	PLL Supply Voltage
31, 36, 42	25, 30, 36	LVDS GND	LVDS Ground
32	26	TxCLK OUT+	Noninverting LVDS Parallel Rate Clock Output
33	27	TxCLK OUT-	Inverting LVDS Parallel Rate Clock Output
34	28	TxOUT2+	Noninverting Channel 2 LVDS Serial Data Output
35	29	TxOUT2-	Inverting Channel 2 LVDS Serial Data Output
37	31	LVDS V_{CC}	LVDS Supply Voltage
38	32	TxOUT1+	Noninverting Channel 1 LVDS Serial Data Output
39	33	TxOUT1-	Inverting Channel 1 LVDS Serial Data Output
40	34	TxOUT0+	Noninverting Channel 0 LVDS Serial Data Output
41	35	TxOUT0-	Inverting Channel 0 LVDS Serial Data Output
43	37	DCB/NC	LVTTL/LVCMOS DC-Balance Programming Input: MAX9209: pulled up to V_{CC} MAX9211: pulled down to GND MAX9213: pulled up to V_{CC} MAX9215: pulled down to GND See Table 1.
—	EP	EP	Exposed Paddle. Solder to ground.

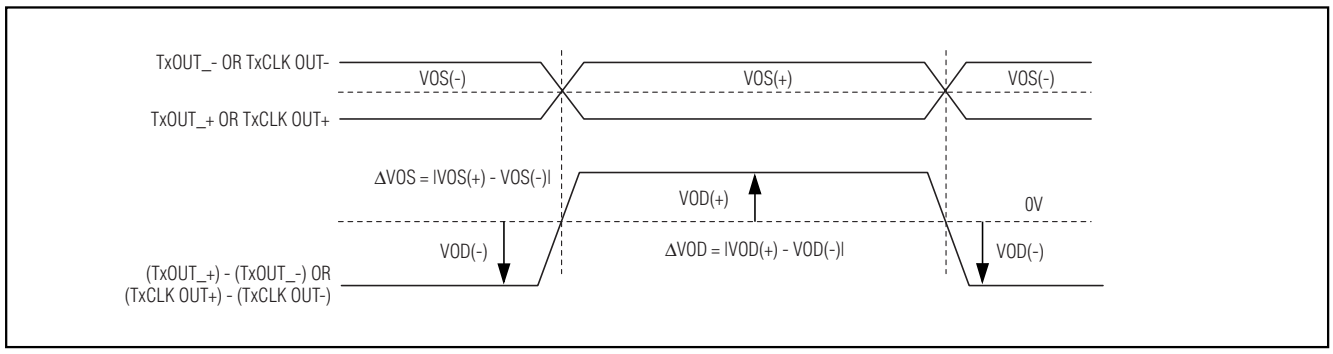


Figure 1. LVDS Output DC Parameters

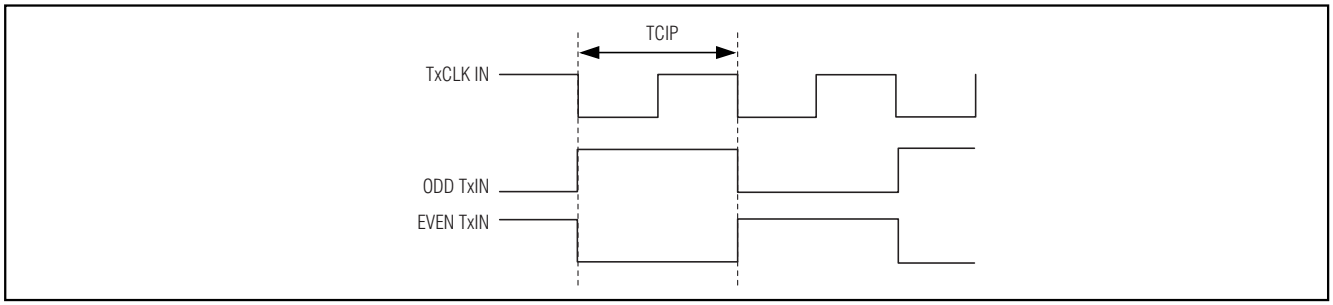


Figure 2. Worst-Case Test Pattern

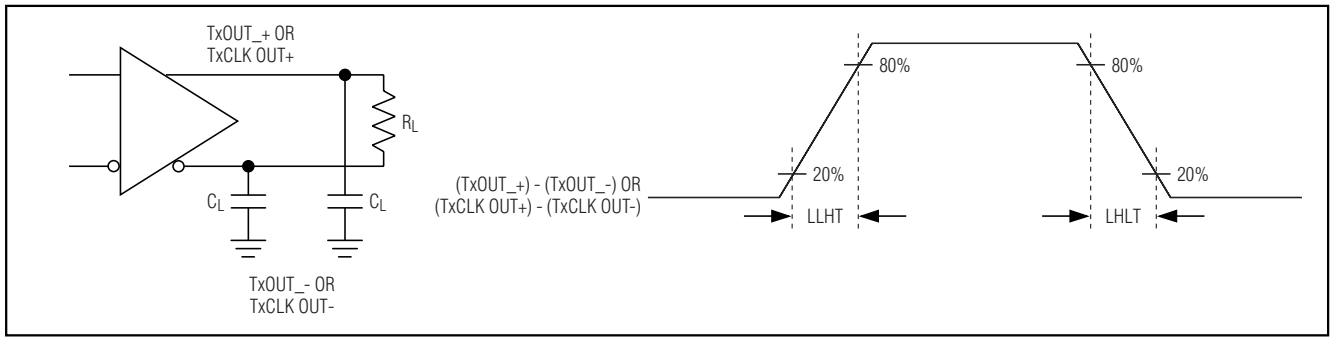


Figure 3. LVDS Output Load and Transition Times

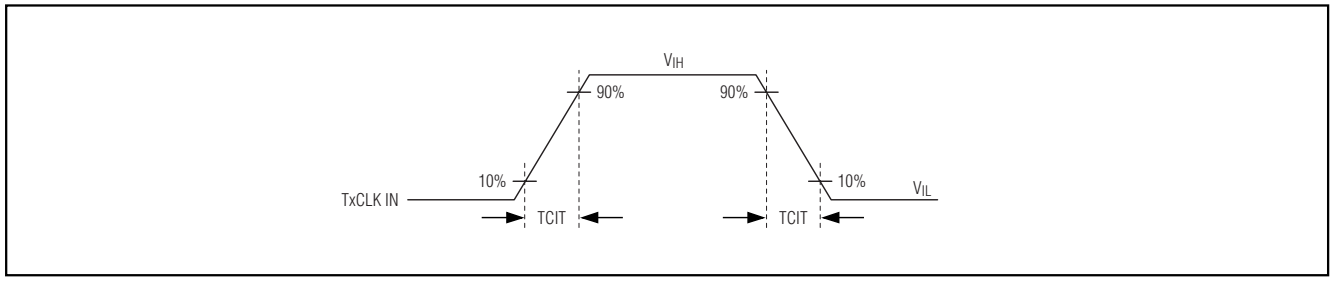


Figure 4. Clock Transition Time Waveform

Programmable DC-Balance 21-Bit Serializers

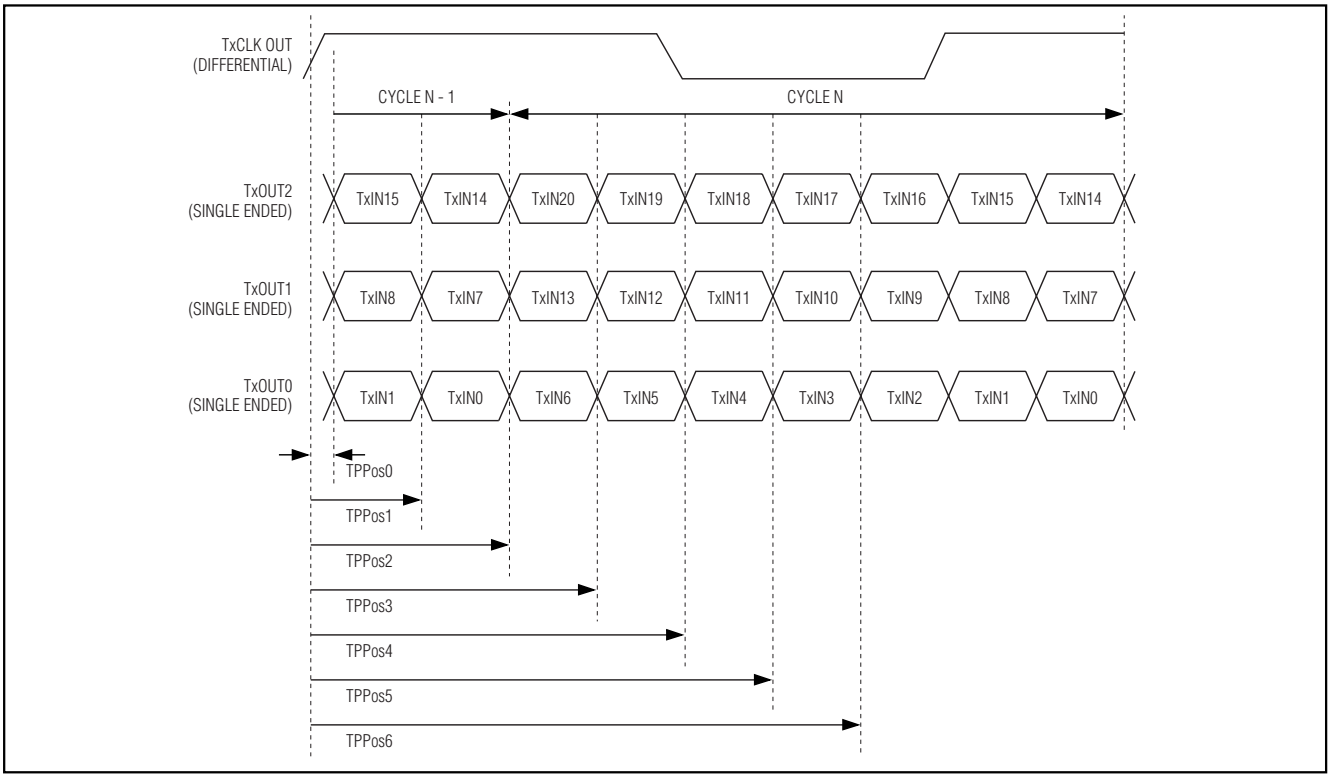


Figure 5. Non-DC-Balanced Mode LVDS Output Pulse Position Measurement

Detailed Description

The MAX9209/MAX9211 operate at a parallel clock frequency of 8MHz to 34MHz in DC-balanced mode and 10MHz to 40MHz in non-DC-balanced mode. The MAX9213/MAX9215 operate at a parallel clock frequency of 16MHz to 66MHz in DC-balanced mode and 20MHz to 85MHz in non-DC-balanced mode.

DC-balanced or non-DC-balanced operation is controlled by the DCB/NC pin (see Table 1). In non-DC-balanced mode, each channel serializes 7 bits every cycle of the parallel clock. In DC-balanced mode, 9 bits are serialized every clock cycle (7 data bits + 2 DC-balance bits). The highest data rate in DC-balanced mode for the MAX9213 or MAX9215 is 66MHz x 9 = 594Mbps. In non-DC-balanced mode, the maximum data rate is 85MHz x 7 = 595Mbps. A bit time is 1 divided by the data rate, for example, 1/595Mbps = 1.68ns.

DC Balance

Through data coding, the DC-balance circuits limit the imbalance of ones and zeros transmitted on each channel. If +1 is assigned to each binary 1 transmitted and -1 is assigned to each binary zero transmitted, the variation in the running sum of assigned values is called the digital sum variation (DSV). The maximum DSV for the MAX9209/MAX9211/MAX9213/MAX9215 data chan-

Table 1. DC-Balance Programming

DEVICE	DCB/NC	OPERATING MODE	OPERATING FREQUENCY (MHz)
MAX9209	High or open	DC balanced	8 to 34
	Low	Non-DC balanced	10 to 40
MAX9211	High	DC balanced	8 to 34
	Low or open	Non-DC balanced	10 to 40
MAX9213	High or open	DC balanced	16 to 66
	Low	Non-DC balanced	20 to 85
MAX9215	High	DC balanced	16 to 66
	Low or open	Non-DC balanced	20 to 85

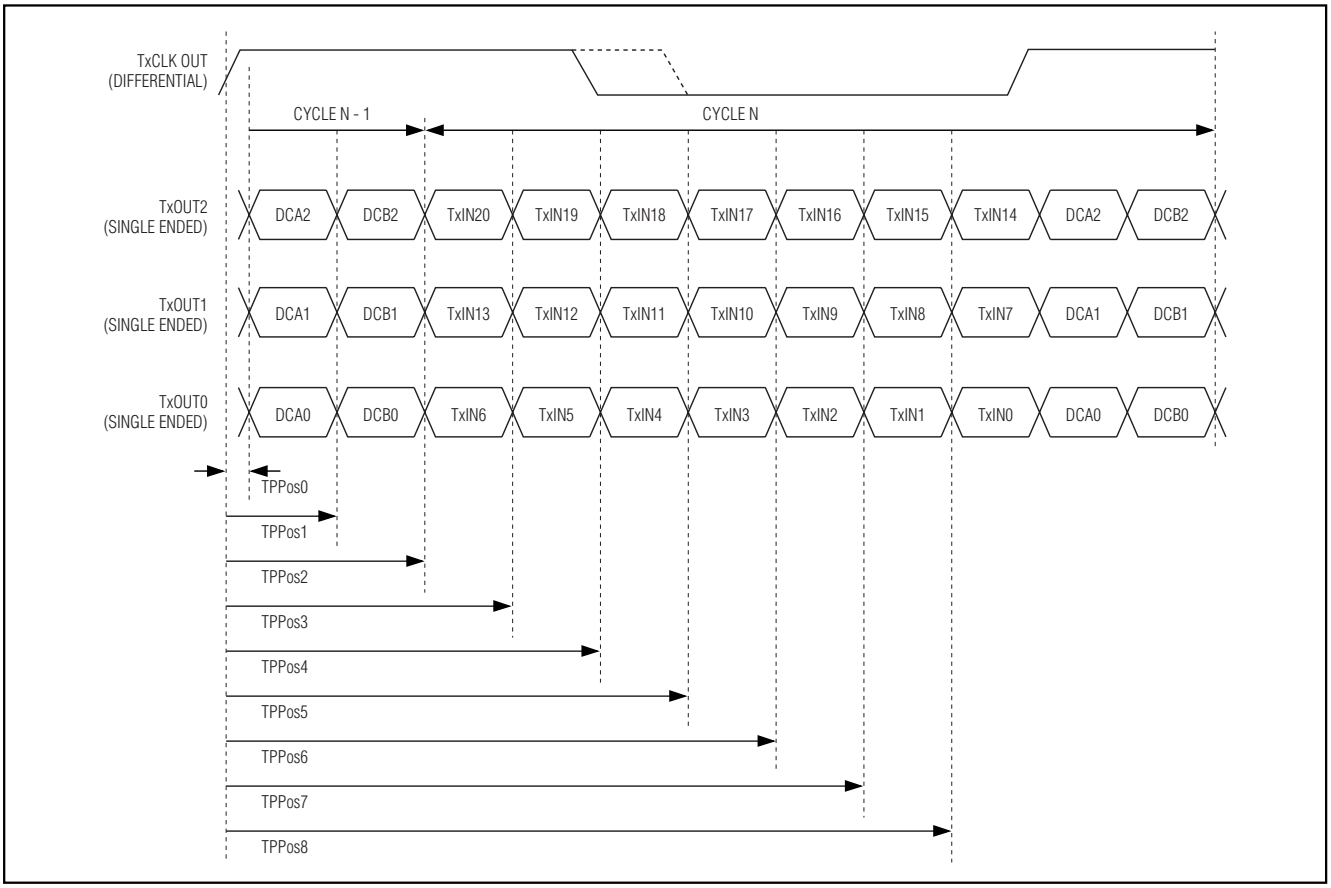


Figure 6. DC-Balanced Mode LVDS Output Pulse Position Measurement

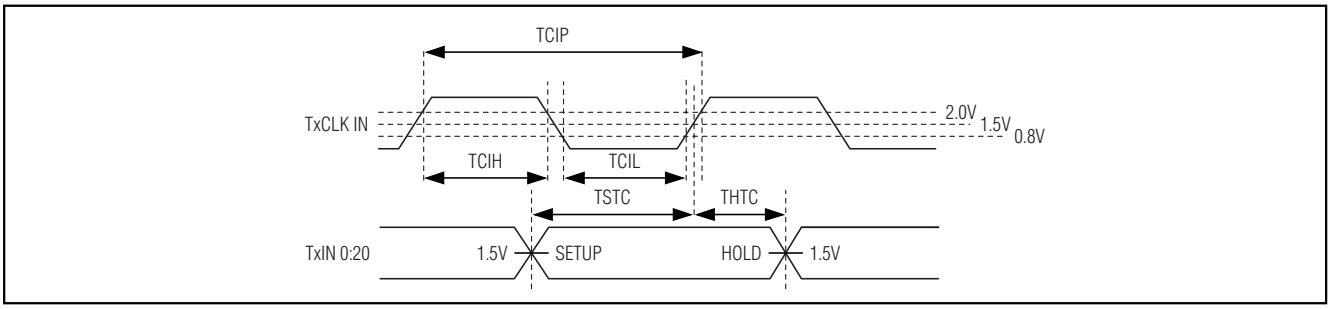


Figure 7. Setup and Hold, High and Low Times

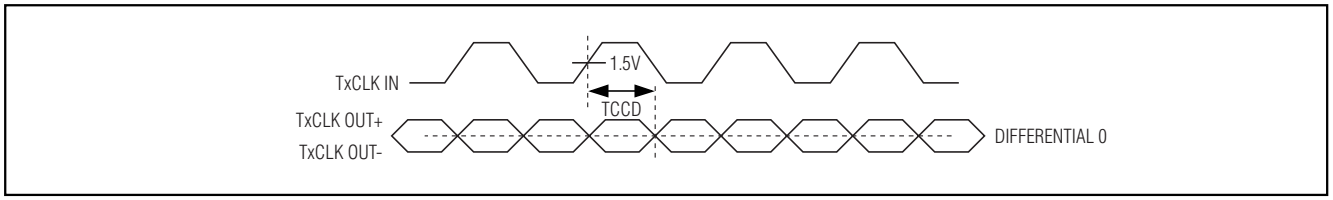


Figure 8. Clock-In to Clock-Out Delay

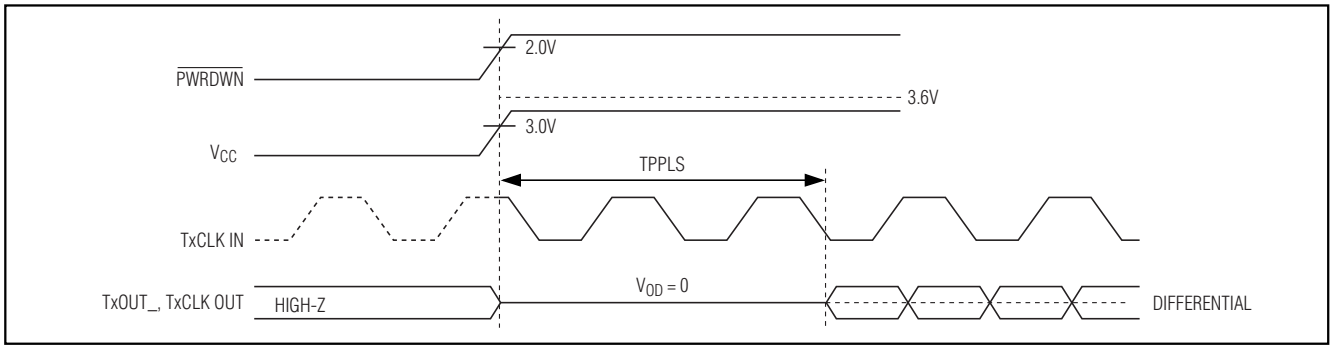


Figure 9. PLL Set Time

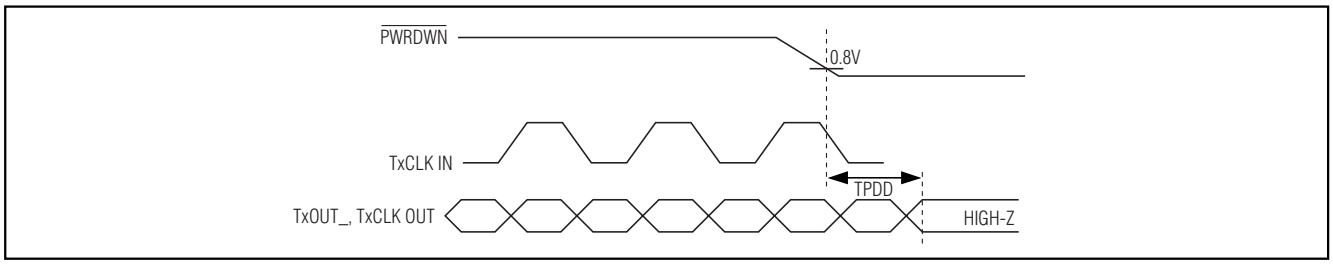


Figure 10. Power-Down Delay

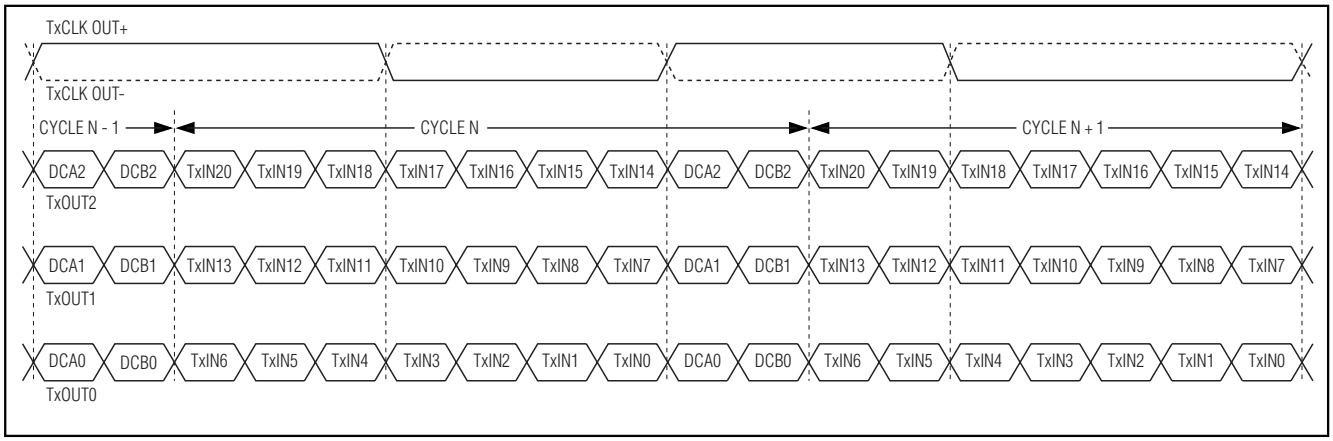


Figure 11. DC-Balanced Mode Inputs Mapped to LVDS Outputs

nels is 10. At most, 10 more zeros than ones, or 10 more ones than zeros, are transmitted. The maximum DSV for the clock channel is 5. Limiting the DSV and choosing the correct coupling capacitors maintain differential signal amplitude and reduce jitter due to droop on AC-coupled links.

To obtain DC balance on the data channels, the parallel input data is inverted or not inverted, depending on the sign of the digital sum at the word boundary. Two complementary bits are appended to each group of 7 parallel input data bits to indicate to the MAX9210/MAX9212/MAX9214/MAX9216 deserializers whether the data bits are inverted (Figure 11). The deserializer restores the original state of the parallel data. The LVDS clock signal alternates duty cycles of 4/9 and 5/9, which maintains DC balance. Figure 12 shows the non-DC-balanced mode inputs mapped to LVDS outputs.

AC-Coupling Benefits

Bit errors experienced with DC-coupling can be eliminated by increasing the receiver common-mode voltage range by AC-coupling. AC-coupling increases the

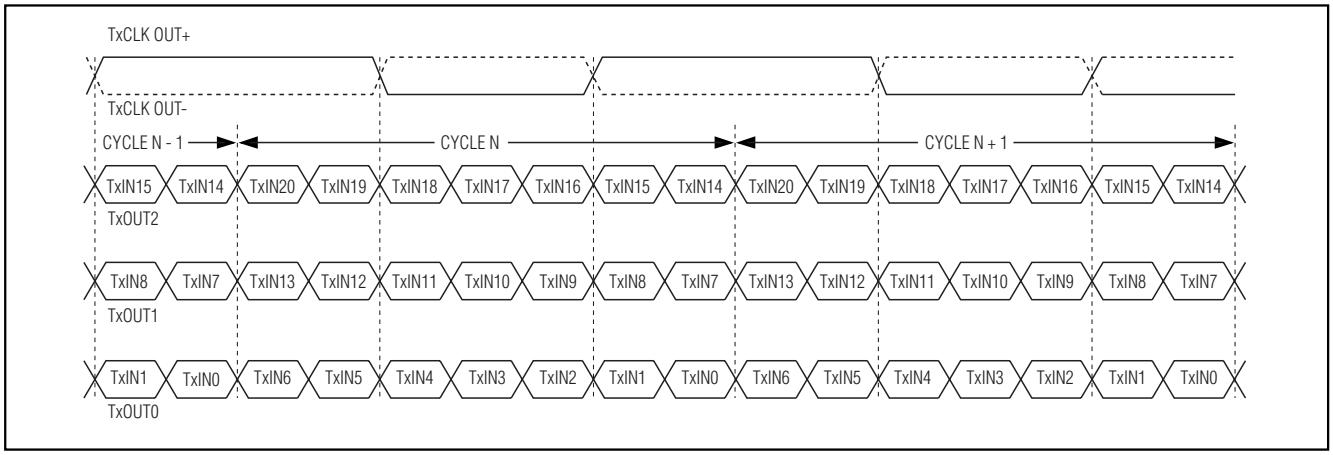


Figure 12. Non-DC-Balanced Mode Inputs Mapped to LVDS Outputs

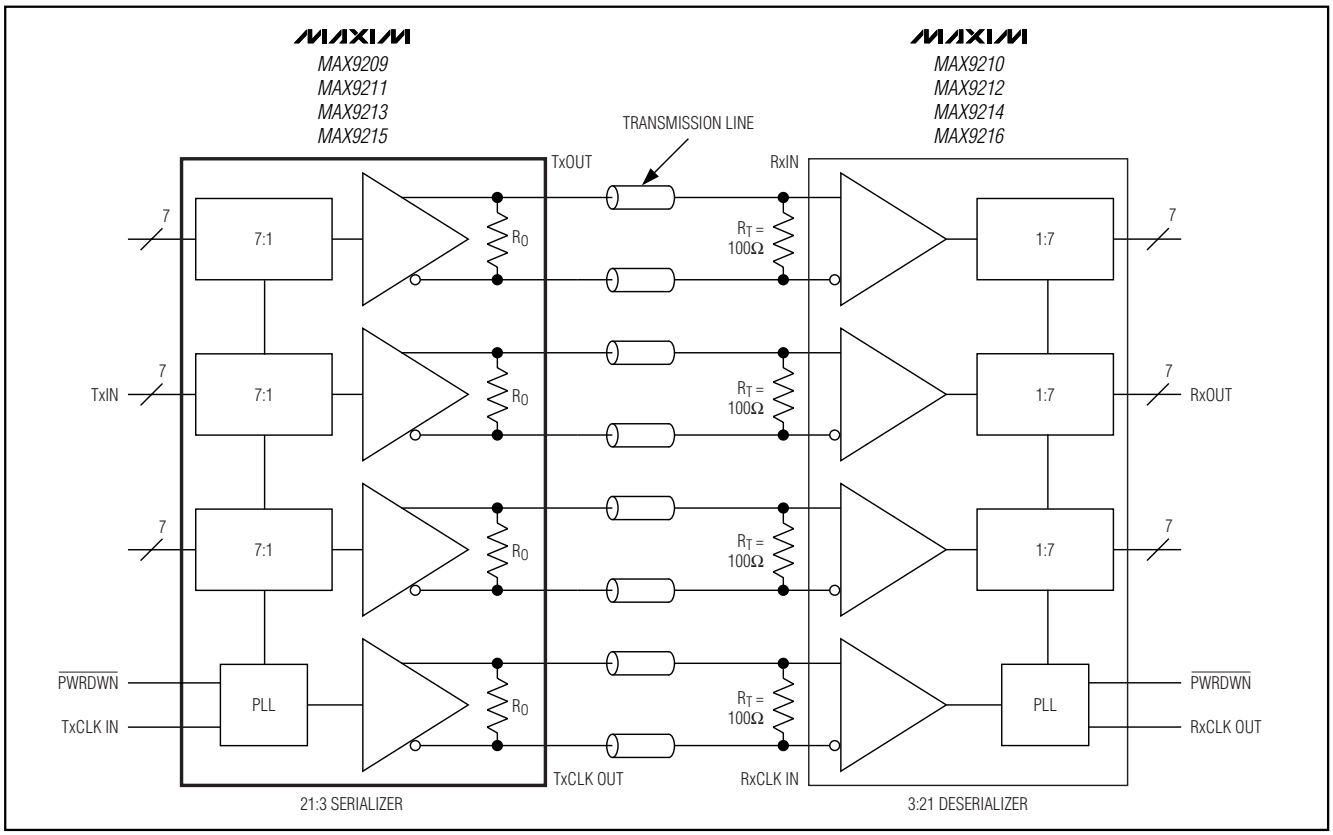


Figure 13. DC-Coupled Link, Non-DC-Balanced Mode

common-mode voltage range of an LVDS receiver to nearly the voltage rating of the capacitor. The typical LVDS driver output is 350mV centered on an offset voltage of 1.25V, making single-ended output voltages of 1.425V and 1.075V. An LVDS receiver accepts signals from 0V to 2.4V, allowing approximately ±1V common-mode difference between the driver and receiver on a DC-coupled link (2.4V - 1.425V = 0.975V and 1.075V - 0V = 1.075V). Figure 13 shows the DC-coupled link, non-DC-balanced mode.

Programmable DC-Balance 21-Bit Serializers

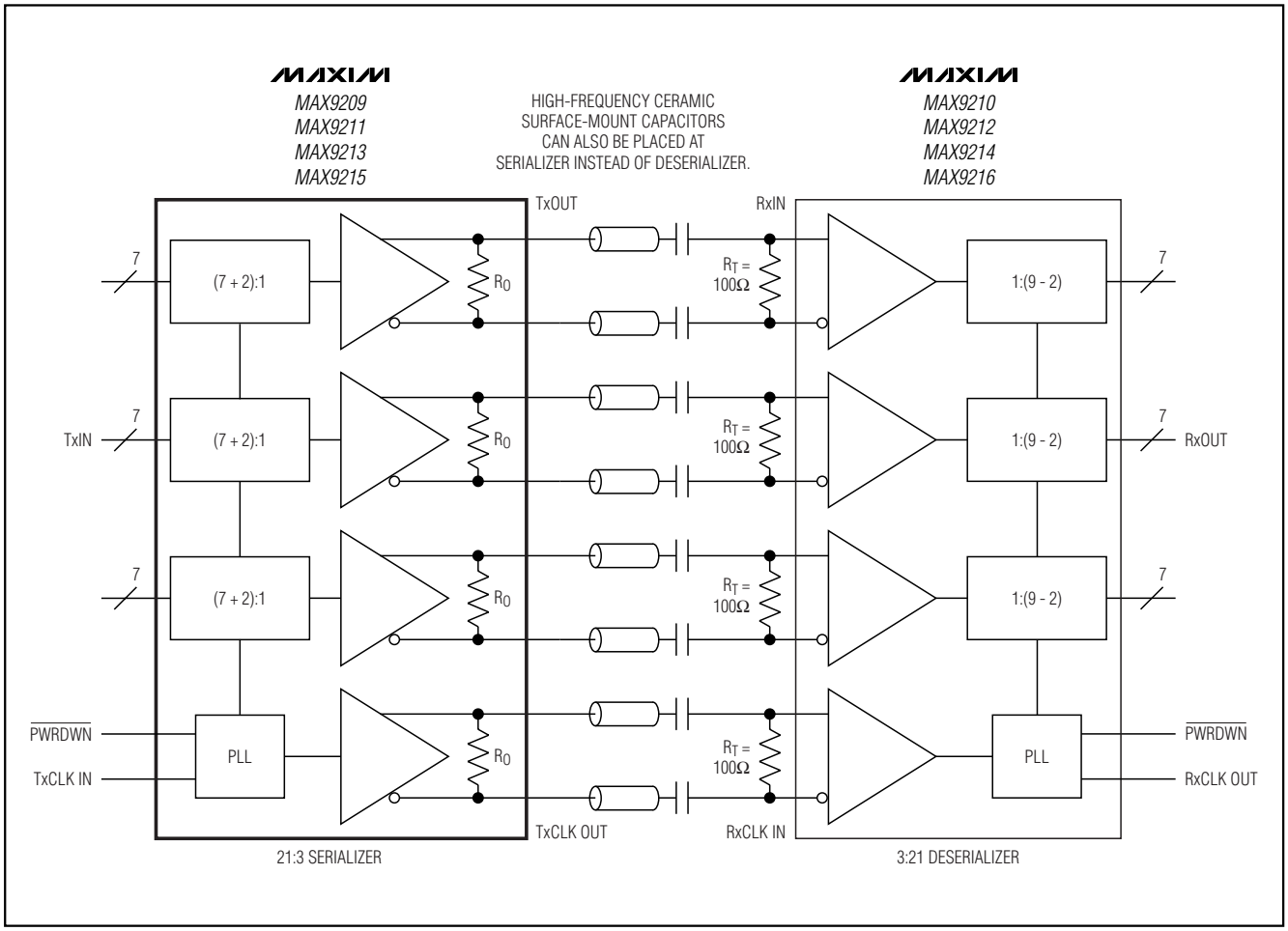


Figure 14. Two Capacitors per Link, AC-Coupled, DC-Balanced Mode

Common-mode voltage differences may be due to ground potential variation or common-mode noise. If there is more than ±1V of difference, the receiver is not guaranteed to read the input signal correctly and may cause bit errors. AC-coupling filters low-frequency ground shifts and common-mode noise and passes high-frequency data. A common-mode voltage difference up to the voltage rating of the coupling capacitor (minus half the differential swing) is tolerated. DC-balanced coding of the data is required to maintain the differential signal amplitude and limit jitter on an AC-coupled link. A capacitor in series with each output of the LVDS driver is sufficient for AC-coupling. However, two capacitors—one at the serializer output and one at the deserializer input—provide protection in case either end of the cable is shorted to a high voltage.

5V Tolerant Inputs

All signal and control inputs except DCB/NC are 5V tolerant and are internally pulled down to GND. The DCB/NC pin has a pulldown on MAX9211/MAX9215 and a pullup on the MAX9209/MAX9213.

DCB/NC Pin Default Conditions

The MAX9209/MAX9211/MAX9213/MAX9215 have programmable DC balance/non-DC balance. See Table 1 for DCB/NC default settings and operating modes.

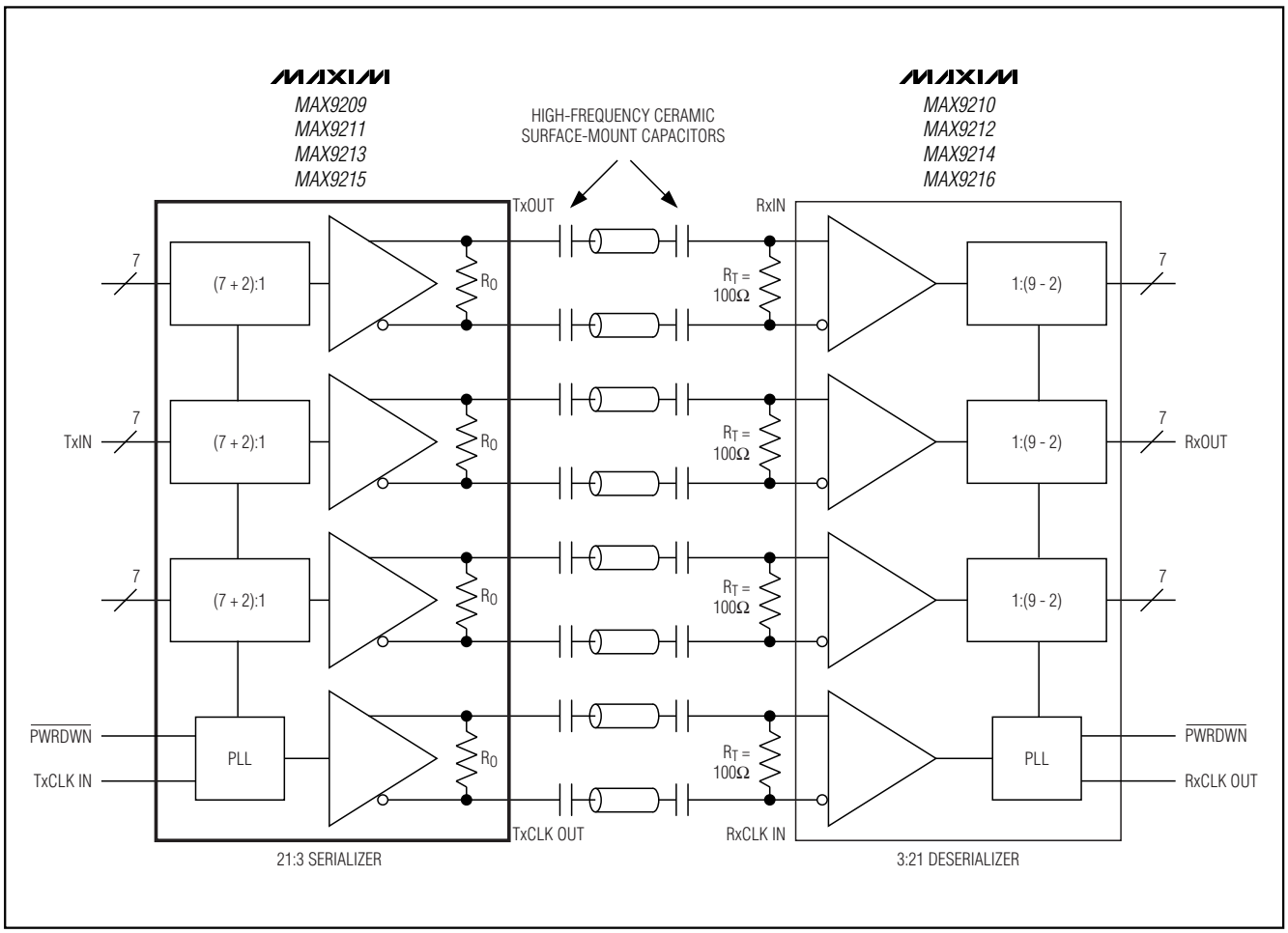


Figure 15. Four Capacitors per Link, AC-Coupled, DC-Balanced Mode

Applications Information

Selection of AC-Coupling Capacitors

Voltage droop and the DSV of transmitted symbols cause signal transitions to start from different voltage levels. Because the transition time is finite, starting the signal transition from different voltage levels causes timing jitter. The time constant for an AC-coupled link needs to be chosen to reduce droop and jitter to an acceptable level.

The RC network for an AC-coupled link consists of the LVDS receiver termination resistor (R_T), the LVDS driver output resistor (R_O), and the series AC-coupling capacitors (C). The RC time constant for two equal-value series capacitors is (C x (R_T + R_O))/2 (Figure 14). The RC time constant for four equal-value series capacitors is (C x (R_T + R_O))/4 (Figure 15).

R_T is required to match the transmission line impedance (usually 100Ω) and R_O is determined by the LVDS driver design, with a minimum value of 78Ω (see the *DC Electrical Characteristics* table). This leaves the capacitor selection to change the system time constant.

In the following example, the capacitor value for a droop of 2% is calculated. Jitter due to this droop is then calculated assuming a 1ns transition time:

$$C = -(2 \times t_B \times DSV) / (\ln (1 - D) \times (R_T + R_O)) \quad \text{(Eq 1)}$$

where:
C = AC-coupling capacitor (F)
t_B = bit time (s)
DSV = digital sum variation (integer)
ln = natural log
D = droop (% of signal amplitude)
R_T = termination resistor (Ω)

Programmable DC-Balance 21-Bit Serializers

R_O = output resistance (Ω)

Equation 1 is for two series capacitors (Figure 14). The bit time (t_B) is the period of the parallel clock divided by 9. The DSV is 10. See equation 3 for four series capacitors (Figure 15).

The capacitor for 2% maximum droop at 8MHz parallel rate clock is:

$$C = -(2 \times t_B \times DSV) / (\ln (1 - D) \times (R_T + R_O))$$
$$C = -(2 \times 13.9ns \times 10) / (\ln (1 - .02) \times (100\Omega + 78\Omega))$$
$$C = 0.0773\mu F$$

Jitter due to droop is proportional to the droop and transition time:

$$t_J = t_T \times D \text{ (Eq 2)}$$

where:
t_J = jitter (s)
t_T = transition time (s) (0% to 100%)
D = droop (% of signal amplitude)

Jitter due to 2% droop and assumed 1ns transition time is:

$$t_J = 1ns \times 0.02$$
$$t_J = 20ps$$

The transition time in a real system depends on the frequency response of the cable driven by the serializer. The capacitor value decreases for a higher frequency parallel clock and for higher levels of droop and jitter. Use high-frequency, surface-mount ceramic capacitors.

Equation 1 altered for four series capacitors (Figure 15) is:

$$C = -(4 \times t_B \times DSV) / (\ln (1 - D) \times (R_T + R_O)) \text{ (Eq 3)}$$

Integrated Termination

The MAX9209/MAX9211/MAX9213/MAX9215 have an integrated output termination resistor across each of the four LVDS outputs. These resistors damp reflections from induced noise and mismatches between the transmission line impedance and termination resistor at the deserializer input. In DC-balanced mode, the differential output resistance is part of the RC time constant. In non-DC-balanced mode, the output termination is increased to 410Ω (typ) to reduce power. In power-down mode ($\overline{PWRDWN}$ = low) or when the power supply is off, the output resistor is switched out and the LVDS outputs are high impedance.

PWRDWN and Power-Off

Driving $\overline{PWRDWN}$ low stops the PLL, switches out the integrated output termination resistors, puts the LVDS outputs in high impedance, and reduces supply current to 50µA or less. Driving $\overline{PWRDWN}$ high starts the PLL lock to the input clock and switches in the output termination resistors. The LVDS outputs are not driven until the PLL locks. The differential output resistance pulls the outputs together and the LVDS outputs are high impedance to ground. If the power supply is turned off, the output resistors are switched out and the LVDS outputs are high impedance.

Input Clock

There is no required timing sequence for the application or reapplication of the parallel rate clock (TxCLK IN) relative to $\overline{PWRDWN}$, or a power-supply ramp for proper PLL lock. The PLL lock time is set by an internal counter. The maximum time to lock is 32,800 clock periods. Power and clock should be stable to meet the lock-time specification. When the PLL is locking, the LVDS outputs are not active and have a differential output resistance of R_O.

Power-Supply Bypassing

There are separate power domains for LVDS, PLL, and digital circuits. Bypass each LVDS V_{CC}, PLL V_{CC}, and V_{CC} pin with high-frequency surface-mount ceramic 0.1µF and 0.001µF capacitors in parallel as close to the device as possible, with the smallest value capacitor closest to the supply pin.

LVDS Outputs

The LVDS outputs are current sources. The voltage swing is proportional to the load impedance. The outputs are rated for a differential load of 100Ω ±1%.

Cables and Connectors

Interconnect for LVDS typically has a differential impedance of 100Ω. Use cables and connectors that have matched differential impedance to minimize impedance discontinuities.

Twisted-pair and shielded twisted-pair cables offer superior signal quality compared to ribbon cable and tend to generate less EMI due to magnetic field canceling effects. Balanced cables pick up noise as common mode, which is rejected by the LVDS receiver.

Board Layout

Keep the LVTTL/LVCMOS input and LVDS output signals separated to prevent crosstalk. A four-layer PC board with separate layers for power, ground, LVDS outputs, and digital signals is recommended.

IEC 61000-4-2 Level 4 ESD Protection

The IEC 61000-4-2 standard specifies ESD tolerance for electronic systems. The IEC 61000-4-2 model (Figure 16) specifies a 150pF capacitor that is discharged into the device through a 330Ω resistor. The MAX9209/MAX9211/MAX9213/MAX9215 LVDS outputs are rated for IEC61000-4-2 level 4 (±8kV contact discharge and ±15kV air discharge). IEC 61000-4-2 discharges higher peak current and more energy than the Human Body Model (HBM) due to the lower series resistance and larger capacitor. The HBM (Figure 17) specifies a 100pF capacitor that is discharged into the device through a 1.5kΩ resistor. All pins are rated for ±2kV HBM.

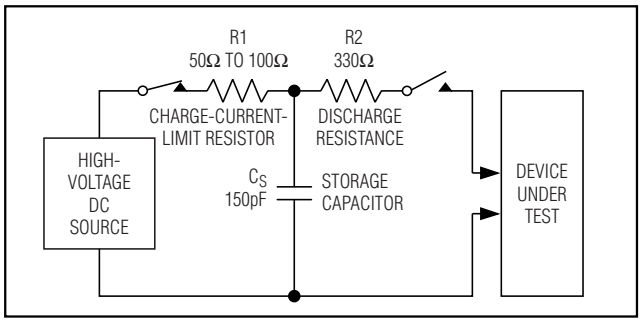


Figure 16. IEC 61000-4-2 Contact Discharge ESD Test Circuit

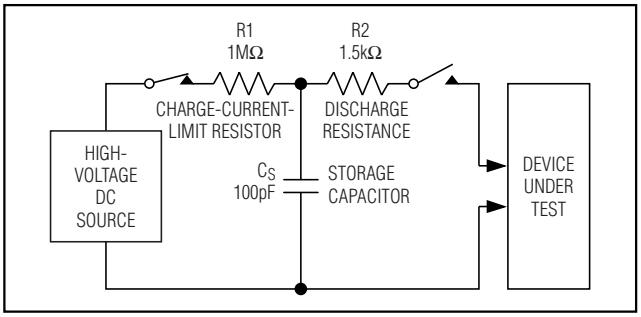
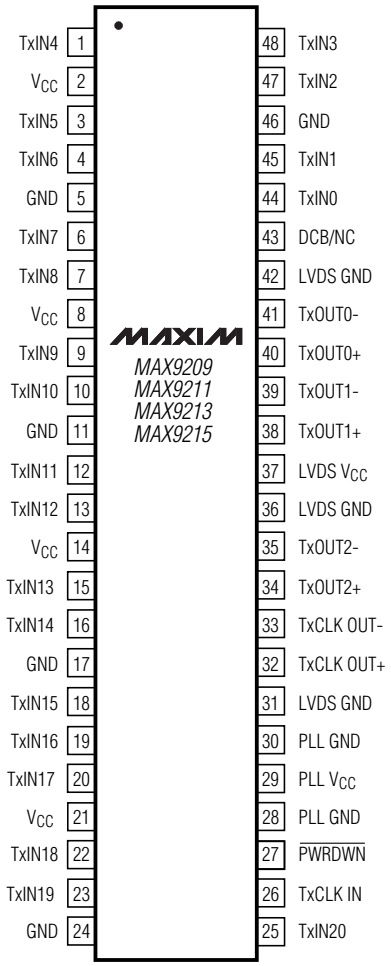


Figure 17. Human Body ESD Test Circuit

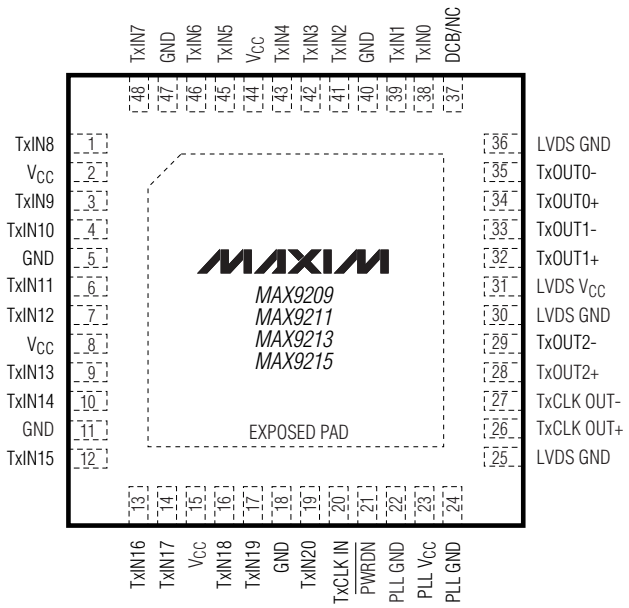
Programmable DC-Balance 21-Bit Serializers

Pin Configurations

TOP VIEW



TSSOP



Thin QFN

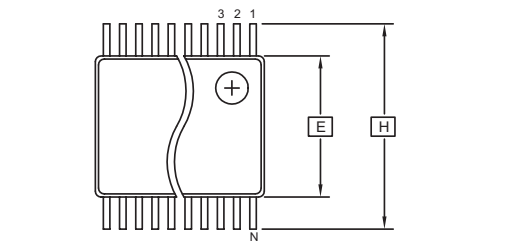
Chip Information

MAX9209 TRANSISTOR COUNT: 9458
MAX9211 TRANSISTOR COUNT: 9458
MAX9213 TRANSISTOR COUNT: 9458
MAX9215 TRANSISTOR COUNT: 9458
PROCESS: CMOS

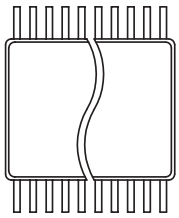
Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)

48L TSSOP.EPS

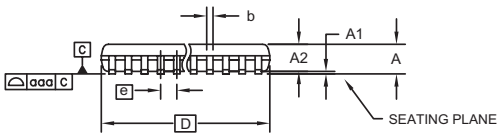


TOP VIEW

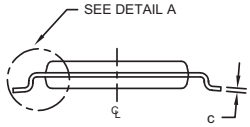


BOTTOM VIEW

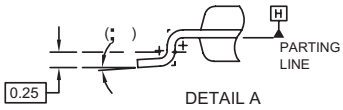
SYMBOL	COMMON DIMENSIONS		
	MIN.	NOM.	MAX.
A	--	--	1.10
A1	0.05	--	0.15
A2	0.55	0.90	0.95
aaa		0.10	
b	0.17	--	0.27
b1	0.17	0.20	0.23
bbb		0.08	
c	0.09	--	0.20
c1	0.09	0.127	0.16
D	12.40	12.50	12.60
E	6.00	6.10	6.20
e		0.50 BSC	
H		8.10 BSC	
L	0.50	0.60	0.75
N		48	
ø	0°	--	8°



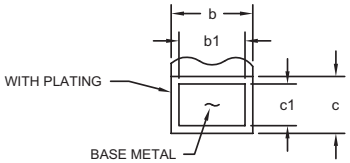
SIDE VIEW



END VIEW



DETAIL A



SECTION C-C

NOTES:

1. DIMENSIONS D & E ARE REFERENCE DATUMS AND DO NOT INCLUDE MOLD FLASH.
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED 0.15MM ON D SIDE, AND 0.25MM ON E SIDE.
3. CONTROLLING DIMENSION: MILLIMETERS.
4. THIS PART IS COMPLIANT WITH JEDEC SPECIFICATION MO-153, VARIATIONS, ED.
5. "N" REFERS TO NUMBER OF LEADS.
6. THE LEAD TIPS MUST LIE WITHIN A SPECIFIED ZONE. THIS TOLERANCE ZONE IS DEFINED BY TWO PARALLEL PLANES. ONE PLANE IS THE SEATING PLANE, DATUM (-C-), THE OTHER PLANE IS AT THE SPECIFIED DISTANCE FROM (-C-) IN THE DIRECTION INDICATED.

MAXIM
PROPRIETARY INFORMATION

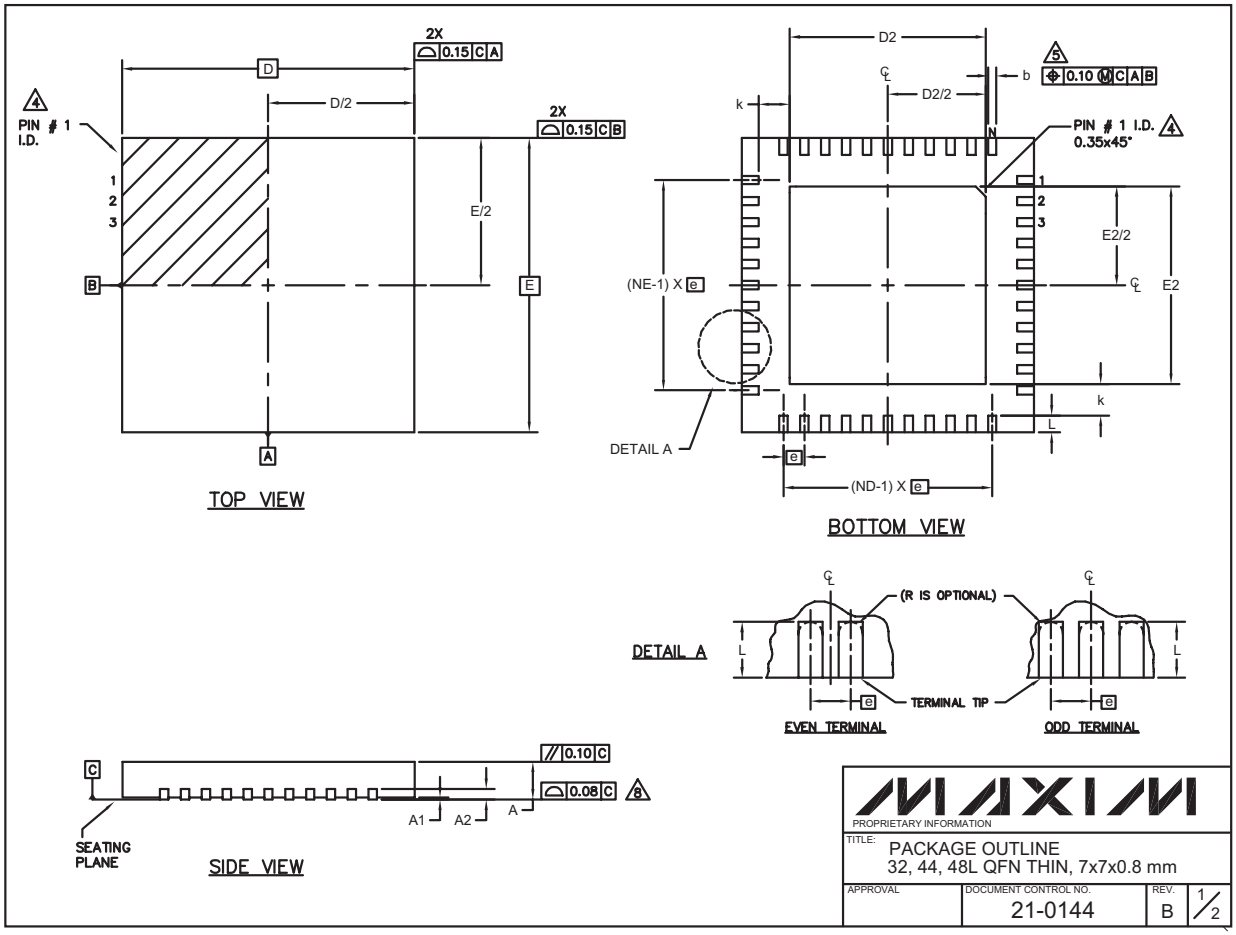
TITLE: PACKAGE OUTLINE, 48L TSSOP, 6.1mm BODY

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0155	A	1/2

Programmable DC-Balance 21-Bit Serializers

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)



Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)

COMMON DIMENSIONS

PKG	32L 7x7			44L 7x7			48L 7x7			CUSTOM PKG. (T4877-1) 48L 7x7		
SYMBOL	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80
A1	0	0.02	0.05	0	0.02	0.05	0	0.02	0.05	0	0.02	0.05
A2	0.20 REF.			0.20 REF.			0.20 REF.			0.20 REF.		
b	0.25	0.30	0.35	0.20	0.25	0.30	0.20	0.25	0.30	0.20	0.25	0.30
D	6.90	7.00	7.10	6.90	7.00	7.10	6.90	7.00	7.10	6.90	7.00	7.10
E	6.90	7.00	7.10	6.90	7.00	7.10	6.90	7.00	7.10	6.90	7.00	7.10
e	0.65 BSC.			0.50 BSC.			0.50 BSC.			0.50 BSC.		
k	0.25	-	-	0.25	-	-	0.25	-	-	0.25	-	-
L	0.45	0.55	0.65	0.45	0.55	0.65	0.30	0.40	0.50	0.45	0.55	0.65
N	32			44			48			44		
ND	8			11			12			10		
NE	8			11			12			12		

EXPOSED PAD VARIATIONS

PKG. CODES	DEPOPULATED LEADS	D2			E2			JEDEC MO220 REV. C
		MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	
T3277-1	-	4.55	4.70	4.85	4.55	4.70	4.85	-
T4477-1	-	4.55	4.70	4.85	4.55	4.70	4.85	WKKD-1
T4877-1**	13, 24, 37, 48	4.20	4.30	4.40	4.20	4.30	4.40	-
T4877-2	-	5.45	5.60	5.63	5.45	5.60	5.63	WKKD-2

** NOTE: T4877-1 IS A CUSTOM 48L PKG. WITH 4 LEADS DEPOPULATED. TOTAL NUMBER OF LEADS ARE 44.

NOTES:

1. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M–1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
3. N IS THE TOTAL NUMBER OF TERMINALS.
4. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JESD 95–1 SPP–012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
5. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25 mm AND 0.30 mm FROM TERMINAL TIP.
6. ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.
7. DEPOPULATION IS POSSIBLE IN A SYMMETRICAL FASHION.
8. COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
9. DRAWING CONFORMS TO JEDEC MO220.
10. WARPAGE SHALL NOT EXCEED 0.10 mm.

MAXIM

PROPRIETARY INFORMATION

TITLE: PACKAGE OUTLINE 32, 44, 48L QFN THIN, 7x7x0.8 mm

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0144	B	2/2

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