Preliminary Data Sheet
January 1998

microelectronics group

Lucent Technologies
Bell Labs Innovations

LG1628AXA SONET/SDH 2.488 Gbits/s Transimpedance Amplifier

Features

- High data rate: 2.5 Gbits/s
- High gain: 5.8 kΩ transimpedance
- Complementary 50 Ω outputs
- Low noise
- Ultrawide dynamic range
- Single –5.2 V ECL power supply

Applications

- SONET/SDH receivers
- SONET/SDH test equipment
- Digital video transmission

Functional Description

The Lucent Technologies Microelectronics Group LG1628AXA is a hybrid integrated circuit that combines the Lucent LG1628A gallium arsenide (GaAs) transimpedance amplifier chip with an external Si dual operational amplifier and necessary filtering to achieve an ultrawide dynamic range amplifier. The LG1628AXA is capable of handling input currents from 3 μA_{avg} to 4 mA_{avg} (patent pending). Amplifier operation is from a single –5.2 V power supply. The targeted transmission system is SONET OC-48 and SDH STM-16.

A complete receiver/regenerator can be constructed with an LG1628AXA followed by an LG1605 limiting amplifier and LG1600 clock and data regenerator.

Figure 1 shows the block diagram of the LG1628AXA transimpedance amplifier. The amplifier consists of a 4.2 kΩ differential transimpedance stage followed by a limiting buffer that provides complementary 50 Ω outputs.

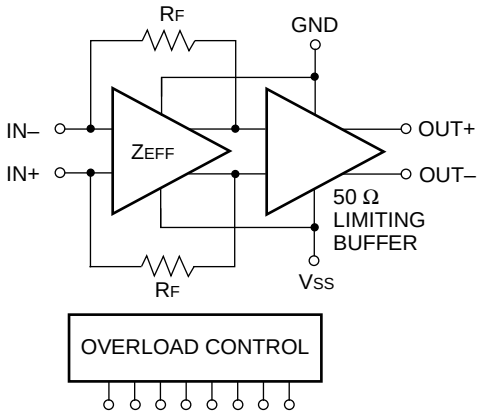

Figure 1. LG1628AXA Functional Diagram

Die Pad Configuration

The die pad configuration is shown in Figure 2.

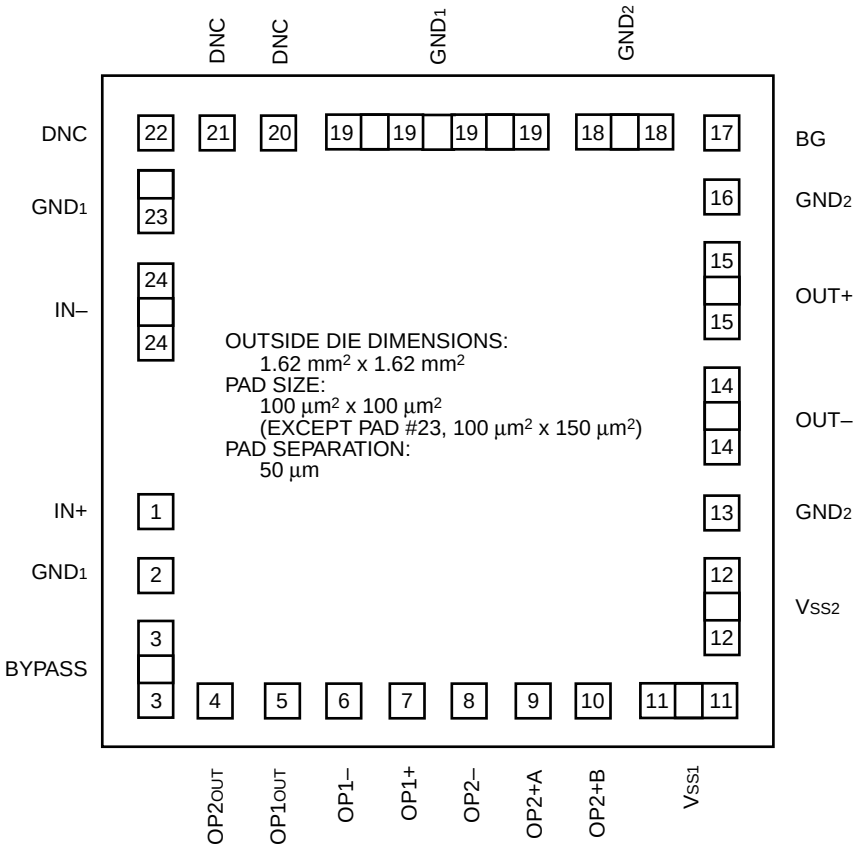

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Figure 2. Die Pad Configuration

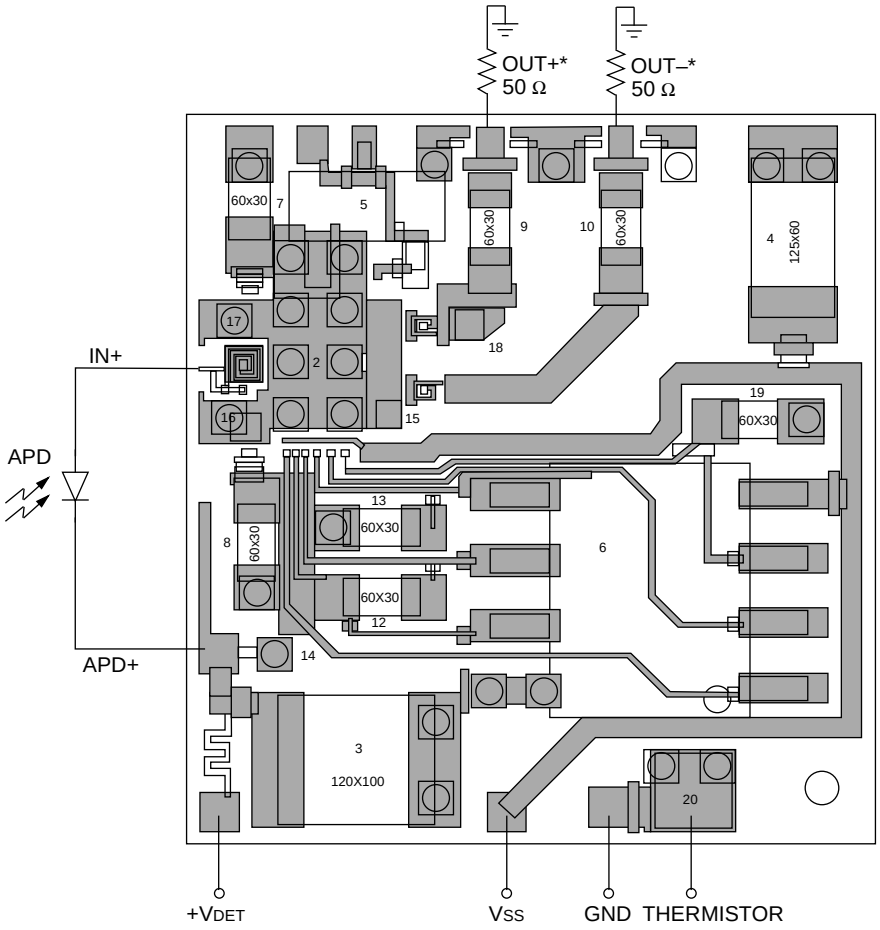
Die Pad Configuration (continued)

The pad descriptions for the LG1628AXA are given in Table 1.

Table 1. Pad Descriptions

Pad	Symbol	Description
1	IN+	Amplifier input; connect to detector anode, current should enter this node.
2, 19, 23	GND_1	Ground.
3	BYPASS	Connections between these nodes and an external dual op amp form the overload control circuitry. See the test circuit in Figure 4 for wiring details. To operate the amplifier without overload control connect $OP2_{OUT}$ to V_{SS}, $OP1_{OUT}$ to GND, and leave BYPASS and the remaining op amp connections open (Figure 5).
4	$OP2_{OUT}$	
5	$OP1_{OUT}$	
6	OP1–	
7	OP1+	
8	OP2–	
9	OP2+A	
10	OP2+B	
11	V_{SS1}	Supply voltage; –5.2 Vdc nominal.
12	V_{SS2}	Supply voltage; –5.2 Vdc nominal.
13, 16, 18	GND_2	Ground.
14	OUT–	Inverted data output (produces low-level output for current entering IN+).
15	OUT+	Noninverted data output (produces high-level output for current entering IN+).
17	BG	Connection for external –2.5 Vdc voltage reference (typically use an Si bandgap).
20, 21, 22	DNC	Do not connect; internal test point or reserved for future use.
24	IN–	Inverting input; must provide ac bypass to ground when using overload control.

Typical Connections and Padout of the Hybrid Integrated Circuit



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* OUT– is delayed approximately 25 ps with respect to OUT+ due to the longer microstrip line associated with OUT–. An extra delay should be added to OUT+ before connecting to the next circuit.

Figure 3. Typical Connections to the HIC (See Figure 4 for a Schematic of the Circuitry on the HIC.)

Table 2. HIC Pad Functional Description

Symbol	Description
IN+	Amplifier input; connect to detector anode, current should enter this node.
APD+	RF bypassed connection for the cathode of the APD.
+V_{DET}	APD power supply connection.
V_{SS}	Supply voltage; –5.2 Vdc nominal.
GND	Ground (back of HIC is also ground).
Thermistor	Negative temperature coefficient thermistor for APD gain control.
OUT+	Noninverted data output (produces high-level output for current entering IN+).
OUT–	Inverted data output (produces low-level output for current entering IN+).

Absolute Maximum Ratings

Stresses in excess of the absolute maximum ratings can cause permanent or latent damage to the device. These are absolute stress ratings only. Functional operation of the device is not implied at these or any other conditions in excess of those given in the operational sections of the data sheet. Exposure to absolute maximum ratings for extended periods can adversely affect device reliability.

Table 3. Absolute Maximum Ratings

Parameter	Min	Max	Unit
Supply Voltage Range (V_{SS})	–7	0.5	V
Power Dissipation	—	1	W
Voltage (all pins)	0.5	V_{SS}	V
Storage Temperature Range	–40	125	°C
Operating Temperature Range	0	100	°C

Recommended Operating Conditions

Table 4. Recommended Operating Conditions

Parameter	Symbol	Min	Max	Unit
Ambient Temperature	T_A	0	85	°C
Power Supply	V_{SS}	–4.7	–5.7	V

Handling Precautions

Although protection circuitry has been designed into this device, proper precautions should be taken to avoid exposure to electrostatic discharge (ESD) during handling and mounting. Lucent Technologies Microelectronics Group employs a human-body model (HBM) and a charged-device model (CDM) for ESD-susceptibility testing and protection design evaluation. No industry-wide standard has been adopted for the CDM. However, a standard HBM (resistance = 1500 Ω, capacitance = 100 pF) is widely used and, therefore, can be used for comparison purposes. The HBM ESD threshold presented here was obtained by using these circuit parameters.

Table 5. ESD Threshold

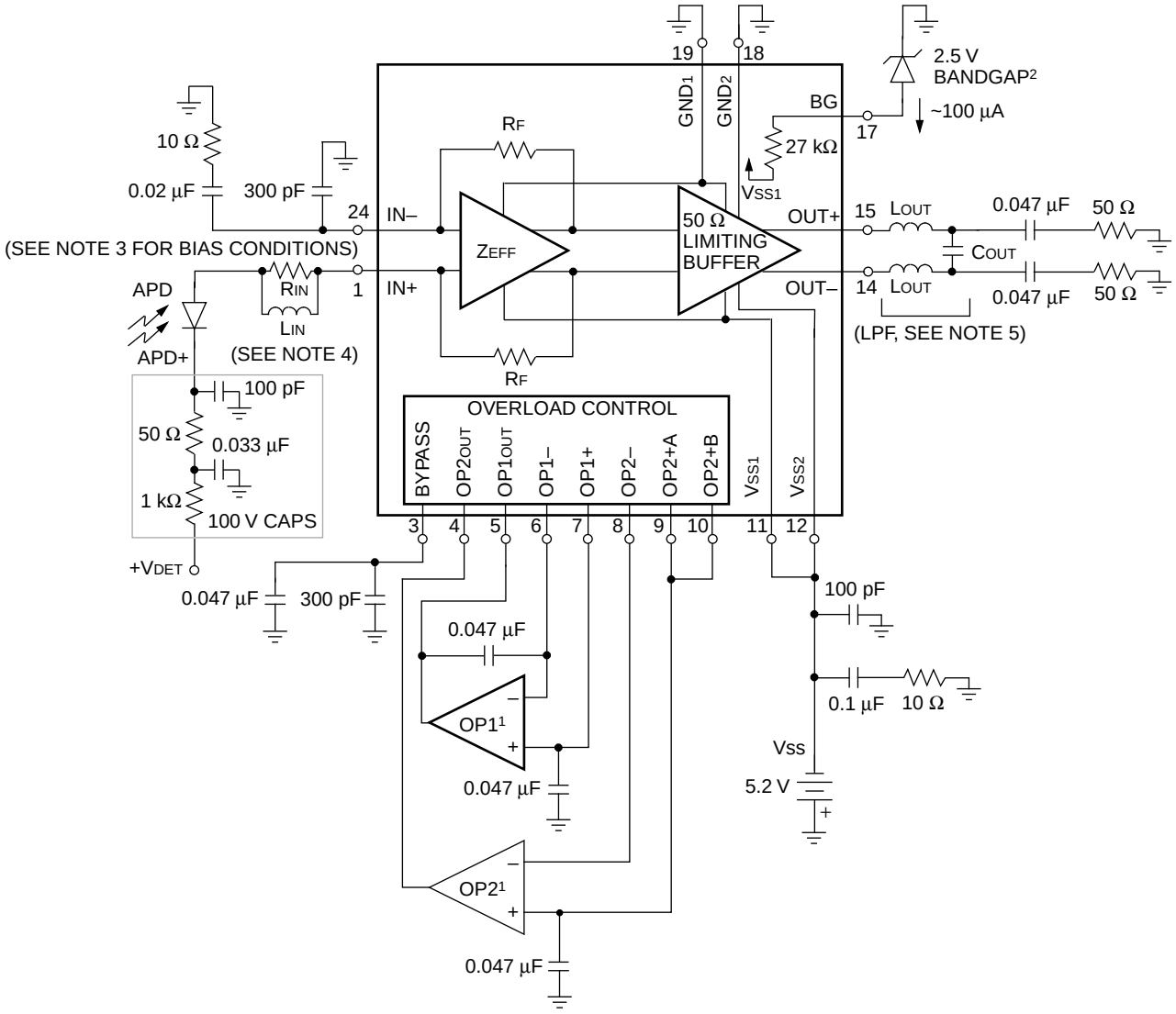
HBM ESD Threshold	
Device	**Voltage**
LG1628AXA	>500 V

Electrical Characteristics

T_A = 25 °C, V_{SS} = –5.2 V, $C_{DETECTOR}$ = 0.5 pF, R_{LOAD} = 50 Ω, unless otherwise indicated.

Parameter	Symbol	Min	Typ	Max	Unit
Power Supply Voltage	V_{SS}	–5.7	–5.2	–4.7	V
Power Supply Current	I_{SS}	—	140	—	mA
Effective Small-signal Transimpedance (Single-ended input to either OUT+ or OUT– each driving a 50 Ω load, differential gain is twice this value.)	T_Z	—	5.8	—	kΩ
Small-signal Bandwidth	BW	1.5	1.6	—	GHz
Transimpedance Peaking	T_{PK}	—	0	1	dB
Output Return Loss	S_{22}	10	15	—	dB
Input Noise Current (100 kHz—2.5 GHz)	I_{NOISE}	—	300	350	nArms
Operating Temperature Range	T_{OP}	0	—	85	°C

Test Circuit with Overload Control



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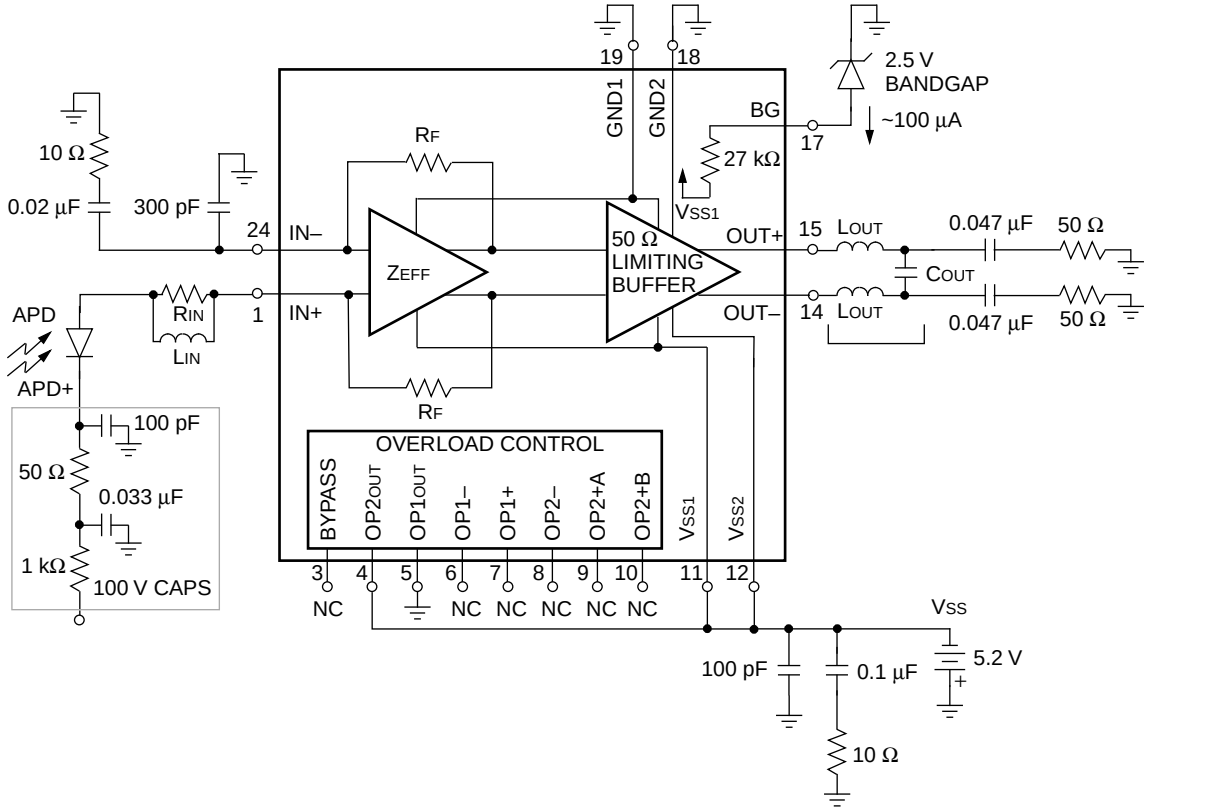
1. Operational amplifiers OP1 and OP2 should have the following characteristics (suggested op amps are the LMC6082IM or OP291GS, both are available as dual op amps in an 8-pin SOIC package):
   a. Single 5 V supply operation.
   b. Maximum input offset voltage of 1 mV.
   c. Low-level output includes negative rail.
   d. High-level output to within 2 V of the positive rail.
   e. Gain bandwidth product ≥1.8 MHz.
   f. Large signal voltage gain ≥100 V/mV.
2. An on-chip 75 kΩ resistor to the negative supply is provided for biasing the voltage reference. Approximately 100 µA of current will be drawn. (Suggested bandgap reference is the LM4040BIM–2.5, available in an SOT-23 package.)
3. Node IN+ is nominally at –3.3 Vdc. APD supply voltage $+V_{det}$ should be adjusted appropriately.
4. RINLIN may be necessary to achieve stability depending on the physical arrangement of the APD and its associated electrical parasitics (series inductance and other resonances). The amplifier will be stable with a 0.5 pF detector capacitance in series with a 0.5 nH inductor, but packaged detectors usually do not behave so ideally at frequencies above a few gigahertz. A parallel RL network consisting of a 200 Ω resistor and a 6 nH inductor is provided on HIC and may be optionally used with a slight noise penalty. Good isolation from output to input is also essential for amplifier stability.
5. A low-pass filter is provided on the LG1628AXA HIC to reduce higher-frequency noise contributions (Butterworth N = 2, Zo = 50 and fc = 4.25 GHz, LOUT = 2.65 nH, COUT = 0.5 pF).

Figure 4. Optical Receiver with Overload Control

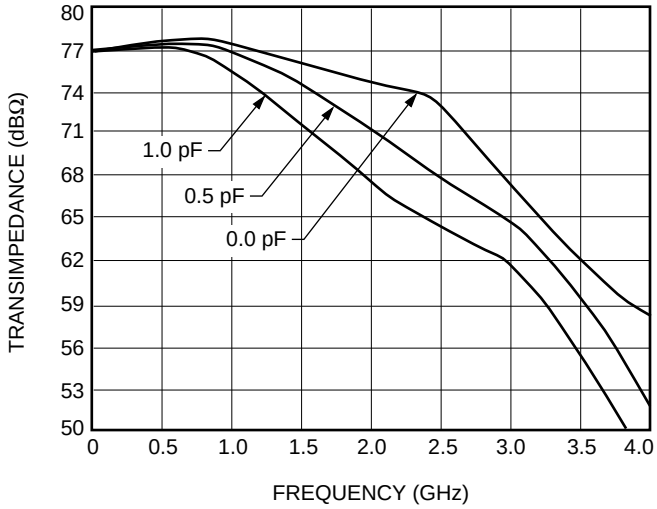
Test Circuit with Overload Control Disabled



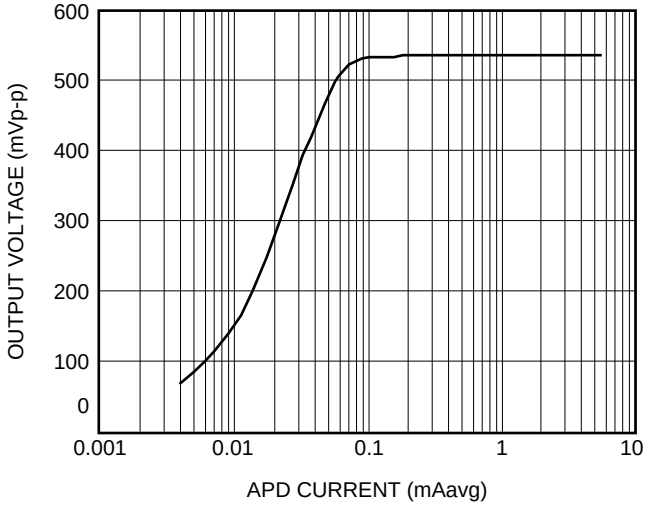
Note: Notes 2, 3, 4, and 5 from the previous page (Figure 4) apply to this drawing.

Figure 5. Optical Receiver with Overload Control Disabled

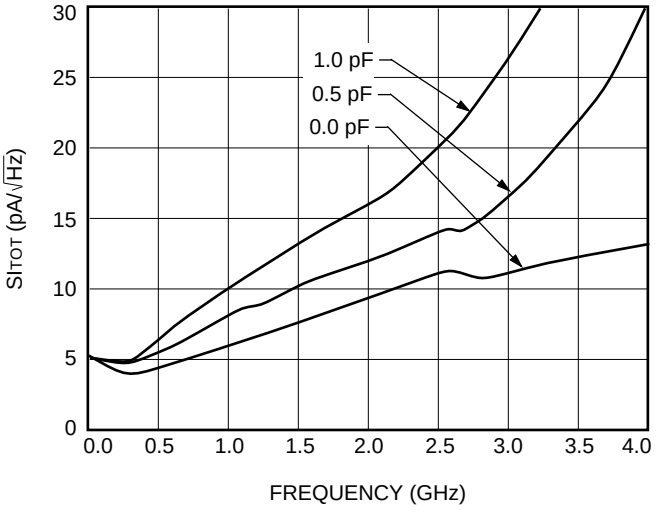
Characteristic Curves (at T_A = 25 °C, V_{SS} = –5.2 V, $C_{DETECTOR}$ = 0.0 pF, 0.5 pF, 1.0 pF, R_{LOAD} = 50 Ω)



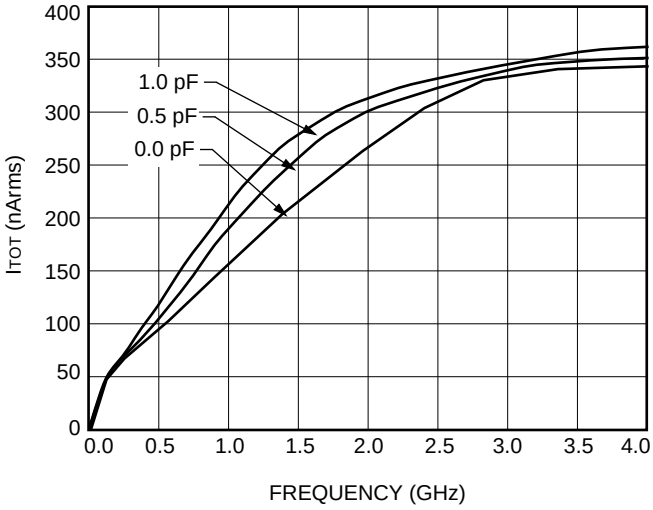
A. Small-Signal Transimpedance



B. Overload Characteristics[1]



C. Input Spectral Noise Density



D. Total Input Noise Current

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1. >25 dB dynamic range requires an external Si dual operational amplifier. The detector polarity is such that current enters the LG1628A (i.e., the detector anode is connected to the LG1628A).

Figure 6. Characteristic Curves as Measured on the LG1628AXA Hybrid Integrated Circuit

Dimensional Drawing of the Hybrid Integrated Circuit (HIC)

Dimensions are in inches. Ceramic thickness is 0.025 inches.

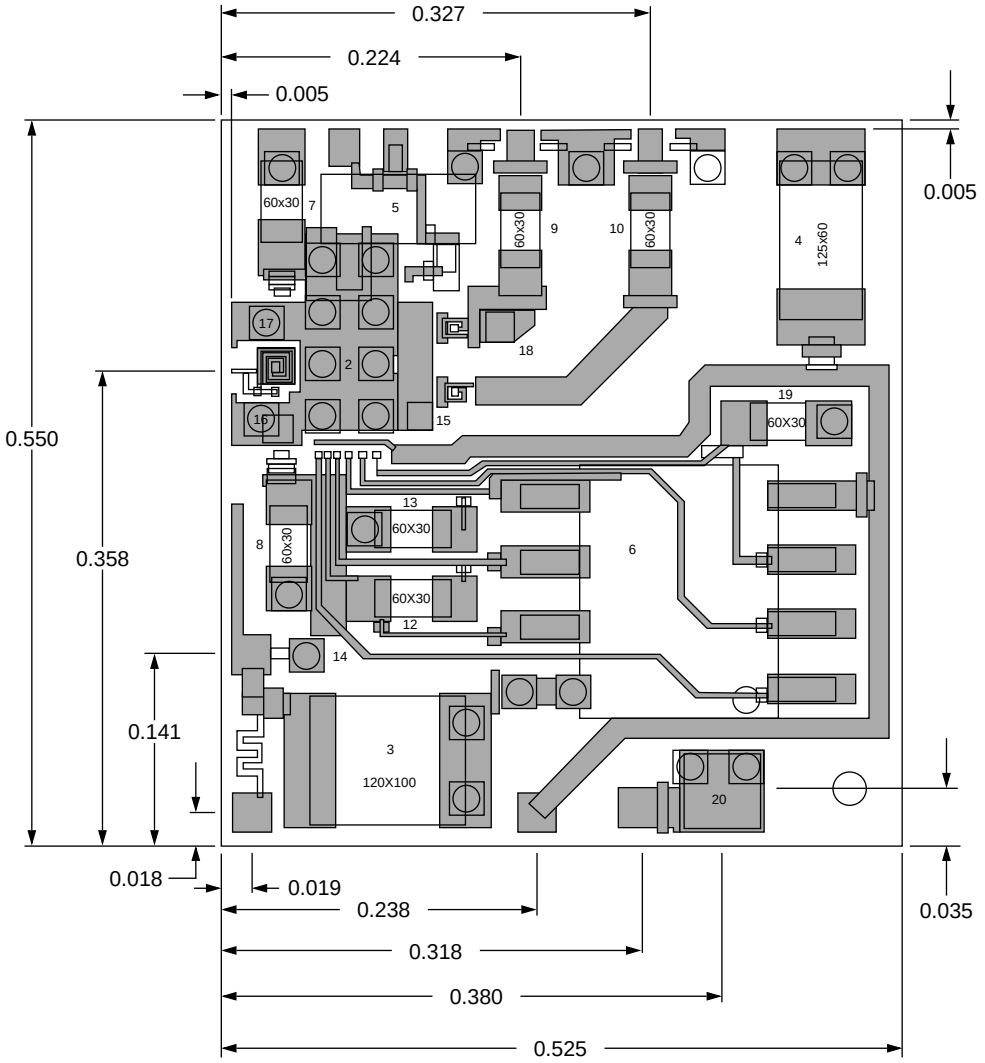

Figure 7. HIC Dimensions and Location of Bonding Pads

Ordering Information

Device Code	Package	Temperature	Comcode (Ordering Number)
LG1628AXA	Hybrid Integrated Circuit Differential Output	0 °C to 85 °C	107791469
LG1628BXA*	Hybrid Integrated Circuit Single-ended Output	0 °C to 85 °C	108052085

* Second output on BXA is terminated through to ground 50 Ω on hybrid.

Notes

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