SONY

CXD3406GA

Timing Generator and Signal Processor for Frame Readout CCD Image Sensor

Description

The CXD3406GA is a timing generator and CCD signal processor IC for the ICX252/262 CCD image sensor.

Features

- Timing generator functions
  - Horizontal drive frequency 12 to 18MHz (Base oscillation frequency 24 to 36MHz)
  - Supports frame readout/draft (sextuple speed)/ AF (Auto focus drive)
  - High-speed/low-speed shutter function
  - Horizontal and vertical drivers for CCD image sensor
- CCD signal processor functions
  - Correlated double sampling
  - Programmable gain amplifier (PGA) allows gain adjustment over a wide range (–6 to +42dB)
  - 10-bit A/D converter
- Chip Scale Package (CSP):
  CSP allows vast reduction in the CCD camera block footprint

Applications

Digital still cameras

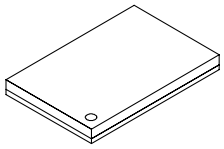
Structure

Silicon gate CMOS IC

Applicable CCD Image Sensors

ICX252 (1/1.8", 3240K pixels)
ICX262 (1/1.8", 3240K pixels)

96 pin LFLGA (Plastic)



Absolute Maximum Ratings

• Supply voltage		
$V_{DD}a$, $V_{DD}b$, $V_{DD}c$, $V_{DD}d$	V_{SS} – 0.3 to +7.0	V
$V_{DD}e$, $V_{DD}f$, $V_{DD}g$	V_{SS} – 0.3 to +4.0	V
VL	–10.0 to V_{SS}	V
VH	VL – 0.3 to +26.0	V
• Input voltage (analog)		
V_{IN}	V_{SS} – 0.3 to V_{DD} + 0.3	V
• Input voltage (digital)		
V_I	V_{SS} – 0.3 to V_{DD} + 0.3	V
• Output voltage		
V_{O1}	V_{SS} – 0.3 to V_{DD} + 0.3	V
V_{O2}	VL – 0.3 to V_{SS} + 0.3	V
V_{O3}	VL – 0.3 to VH + 0.3	V
• Operating temperature		
Topr	–20 to +75	°C
• Storage temperature		
Tstg	–55 to +125	°C

Recommended Operating Conditions

• Supply voltage		
$V_{DD}b$	3.0 to 5.5	V
$V_{DD}a$, $V_{DD}c$, $V_{DD}d$	3.0 to 3.6	V
VM	0.0	V
VH	14.5 to 15.5	V
VL	–7.0 to –8.0	V
$V_{DD}e$, $V_{DD}f$, $V_{DD}g$	3.0 to 3.6	V
• Operating temperature		
Topr	–20 to +75	°C

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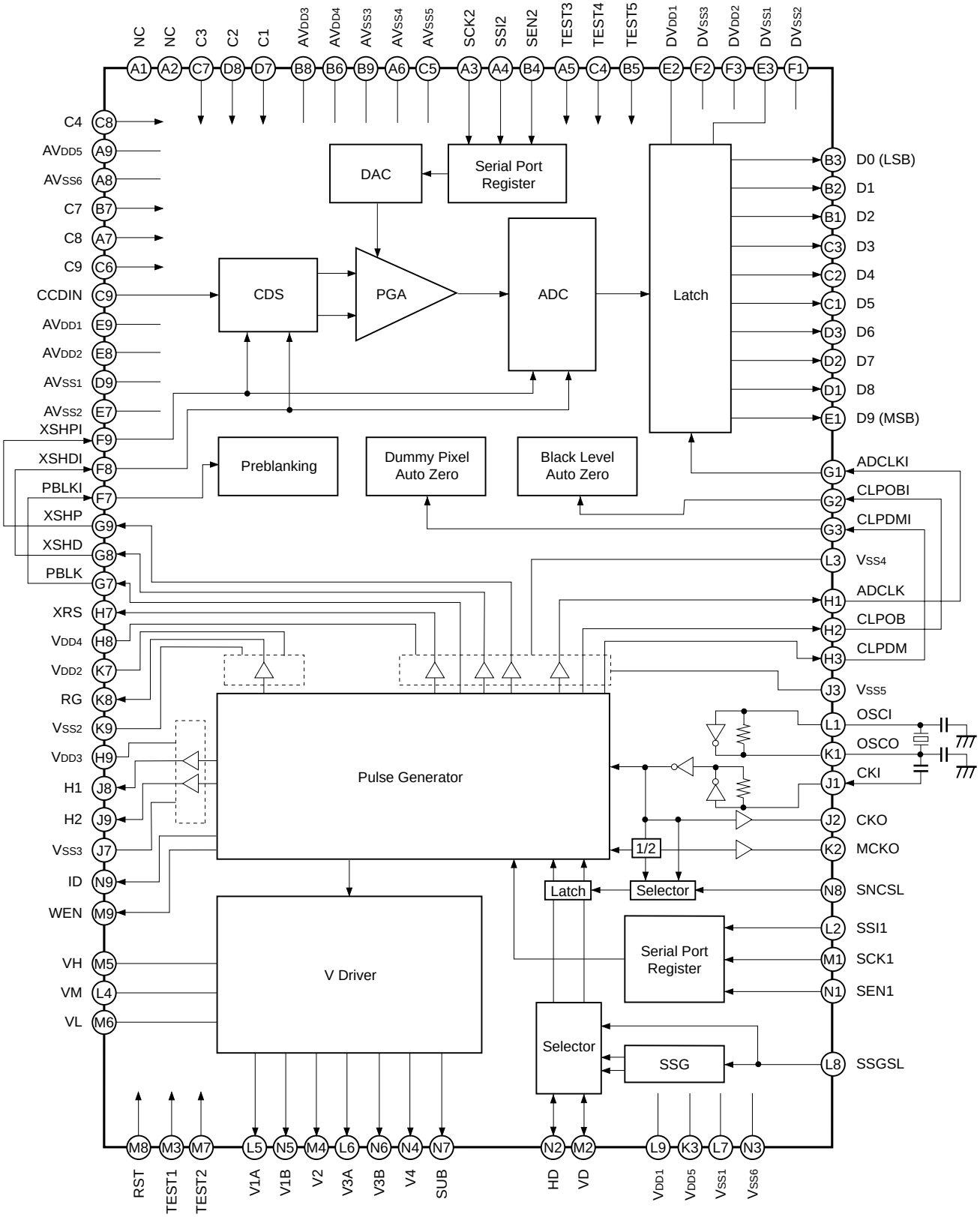
Block Diagram



Pin Configuration (Top View)

	1	2	3	4	5	6	7	8	9
A	NC	NC	SCK2	SSI2	TEST3	AV_{SS4}	C8	AV_{SS6}	AV_{DD5}
B	D2	D1	D0	SEN2	TEST5	AV_{DD4}	C7	AV_{DD3}	AV_{SS3}
C	D5	D4	D3	TEST4	AV_{SS5}	C9	C3	C4	CCDIN
D	D8	D7	D6				C1	C2	AV_{SS1}
E	D9	DV_{DD1}	DV_{SS1}				AV_{SS2}	AV_{DD2}	AV_{DD1}
F	DV_{SS2}	DV_{SS3}	DV_{DD2}				PBLKI	XSHDI	XSHPI
G	ADCLKI	CLPOBI	CLPDMI				PBLK	XSHD	XSHP
H	ADCLK	CLPOB	CLPDM				XRS	V_{DD4}	V_{DD3}
J	CKI	CKO	V_{SS5}				V_{SS3}	H1	H2
K	OSCO	MCKO	V_{DD5}				V_{DD2}	RG	V_{SS2}
L	OSCI	SSI1	V_{SS4}	VM	V1A	V3A	V_{SS1}	SSGSL	V_{DD1}
M	SCK1	VD	TEST1	V2	VH	VL	TEST2	RST	WEN
N	SEN1	HD	V_{SS6}	V4	V1B	V3B	SUB	SNCSL	ID

Pin Description

Pin No.	Symbol	I/O	Description
A1	NC	—	No connected.
A2	NC	—	No connected.
A3	SCK2	I	CCD signal processor block serial interface clock input. (Schmitt trigger)
A4	SSI2	I	CCD signal processor block serial interface data input. (Schmitt trigger)
A5	TEST3	I	CCD signal processor block test input 3. Connect to DV_{SS}.
A6	AV_{SS4}	—	CCD signal processor block analog GND.
A7	C8	—	Capacitor connection.
A8	AV_{SS6}	—	CCD signal processor block analog GND.
A9	AV_{DD5}	—	CCD signal processor block analog power supply.
B1	D2	O	ADC output.
B2	D1	O	ADC output.
B3	D0	O	ADC output (LSB).
B4	SEN2	I	CCD signal processor block serial interface enable input. (Schmitt trigger)
B5	TEST5	I	CCD signal processor block test input 5. Connect to DV_{DD}.
B6	AV_{DD4}	—	CCD signal processor block analog power supply.
B7	C7	—	Capacitor connection.
B8	AV_{DD3}	—	CCD signal processor block analog power supply.
B9	AV_{SS3}	—	CCD signal processor block analog GND.
C1	D5	O	ADC output.
C2	D4	O	ADC output.
C3	D3	O	ADC output.
C4	TEST4	I	CCD signal processor block test input 4. Connect to DV_{SS}.
C5	AV_{SS5}	—	CCD signal processor block analog GND.
C6	C9	—	Capacitor connection.
C7	C3	—	Capacitor connection.
C8	C4	—	Capacitor connection.
C9	CCDIN	I	CCD output signal input.
D1	D8	O	ADC output.
D2	D7	O	ADC output.
D3	D6	O	ADC output.
D7	C1	—	Capacitor connection.
D8	C2	—	Capacitor connection.
D9	AV_{SS1}	—	CCD signal processor block analog GND.
E1	D9	O	ADC output (MSB).
E2	DV_{DD1}	—	CCD signal processor block digital power supply. (Power supply for ADC)

Pin No.	Symbol	I/O	Description
E3	DV_{SS1}	—	CCD signal processor block digital GND. (GND for ADC)
E7	AV_{SS2}	—	CCD signal processor block analog GND.
E8	AV_{DD2}	—	CCD signal processor block analog power supply.
E9	AV_{DD1}	—	CCD signal processor block analog power supply.
F1	DV_{SS2}	—	CCD signal processor block digital GND.
F2	DV_{SS3}	—	CCD signal processor block digital GND.
F3	DV_{DD2}	—	CCD signal processor block digital power supply.
F7	PBLKI	I	Pulse input for horizontal and vertical blanking period pulse cleaning. (Schmitt trigger)
F8	XSHDI	I	CCD data level sample-and-hold pulse input. (Schmitt trigger)
F9	XSHPI	I	CCD precharge level sample-and-hold pulse input. (Schmitt trigger)
G1	ADCLKI	I	Clock input for analog/digital conversion. (Schmitt trigger)
G2	CLPOBI	I	CCD optical black signal clamp pulse input. (Schmitt trigger)
G3	CLPDMI	I	CCD dummy signal clamp pulse input. (Schmitt trigger)
G7	PBLK	O	Pulse output for horizontal and vertical blanking period pulse cleaning.
G8	XSHD	O	CCD data level sample-and-hold pulse output.
G9	XSHP	O	CCD precharge level sample-and-hold pulse output.
H1	ADCLK	O	Clock output for analog/digital conversion.
H2	CLPOB	O	CCD optical black signal clamp pulse output.
H3	CLPDM	O	CCD dummy signal clamp pulse output.
H7	XRS	O	Sample-and-hold pulse output for analog/digital conversion phase alignment.
H8	V_{DD4}	—	Timing generator block digital power supply. (Power supply for CDS block)
H9	V_{DD3}	—	Timing generator block 3.0 to 5.0V power supply. (Power supply for H1/H2)
J1	CKI	I	Inverter input.
J2	CKO	O	Inverter output.
J3	V_{SS5}	—	Timing generator block digital GND.
J7	V_{SS3}	—	Timing generator block digital GND.
J8	H1	O	CCD horizontal register clock output.
J9	H2	O	CCD horizontal register clock output.
K1	OSCO	O	Inverter output for oscillation. When not used, leave open or connect a capacitor.
K2	MCKO	O	System clock output for signal processor IC.
K3	V_{DD5}	—	Timing generator block digital power supply. (Power supply for common logic block)
K7	V_{DD2}	—	Timing generator block digital power supply. (Power supply for RG)
K8	RG	O	CCD reset gate pulse output.
K9	V_{SS2}	—	Timing generator block digital GND.
L1	OSCI	I	Inverter input for oscillation. When not used, fix to low.

Pin No.	Symbol	I/O	Description
L2	SSI1	I	Timing generator block serial interface data input. Schmitt trigger input/No protective diode on power supply side.
L3	V_{SS4}	—	Timing generator block digital GND.
L4	VM	—	Timing generator block digital GND. (GND for vertical driver)
L5	V1A	O	CCD vertical register clock output.
L6	V3A	O	CCD vertical register clock output.
L7	V_{SS1}	—	Timing generator block digital GND.
L8	SSGSL	I	Internal SSG enable. High: Internal SSG valid, Low: External SYNC valid (With pull-down resistor)
L9	V_{DD1}	—	Timing generator block digital power supply.(Power supply for common logic block)
M1	SCK1	I	Timing generator block serial interface clock input. Schmitt trigger input/No protective diode on power supply side.
M2	VD	I/O	Vertical sync signal input/output.
M3	TEST1	I	Timing generator block test input 1. Normally fix to GND. (With pull-down resistor)
M4	V2	O	CCD vertical register clock output.
M5	VH	—	Timing generator block 15.0V power supply. (Power supply for vertical driver)
M6	VL	—	Timing generator block –7.5V power supply. (Power supply for vertical driver)
M7	TEST2	I	Timing generator block test input 2. Normally fix to GND. (With pull-down resistor)
M8	RST	I	Timing generator block reset input. High: Normal operation, Low: Reset control Normally apply reset during power-on. Schmitt trigger input/No protective diode on power supply side
M9	WEN	O	Memory write timing pulse output.
N1	SEN1	I	Timing generator block serial interface strobe input. Schmitt trigger input/No protective diode on power supply side
N2	HD	I/O	Horizontal sync signal input/output.
N3	V_{SS6}	—	Timing generator block digital GND.
N4	V4	O	CCD vertical register clock output.
N5	V1B	O	CCD vertical register clock output.
N6	V3B	O	CCD vertical register clock output.
N7	SUB	O	CCD electronic shutter pulse output.
N8	SNCSL	I	Control input used to switch sync system. High: CKI sync, Low: MCKO sync (With pull-down resistor)
N9	ID	O	Vertical direction line identification pulse output.

Electrical Characteristics

Timing Generator Block Electrical Characteristics

DC Characteristics (Within the recommended operating conditions)

Item	Pins	Symbol	Conditions	Min.	Typ.	Max.	Unit
Supply voltage 1	V_{DD2}	$V_{DD}a$		3.0	3.3	3.6	V
Supply voltage 2	V_{DD3}	$V_{DD}b$		3.0	3.3	5.5	V
Supply voltage 3	V_{DD4}	$V_{DD}c$		3.0	3.3	3.6	V
Supply voltage 4	V_{DD1}, V_{DD5}	$V_{DD}d$		3.0	3.3	3.6	V
Input voltage 1*1	RST	V_{i+}		0.8V_{DD}d			V
		V_{i-}				0.2V_{DD}d	V
Input voltage 2*2	SSI1, SCK1, SEN1	V_{i+}		0.8V_{DD}d			V
		V_{i-}				0.2V_{DD}d	V
Input voltage 3*3	TEST1, TEST2	V_{IH1}		0.7V_{DD}d			V
		V_{IL1}				0.2V_{DD}d	V
Input voltage 4*4	SNCSL, SSGSL	V_{IH2}		0.7V_{DD}d			V
		V_{IL2}				0.3V_{DD}d	V
Input/output voltage	VD, HD	V_{IH3}		0.8V_{DD}d			V
		V_{IL3}				0.2V_{DD}d	V
		V_{OH1}	Feed current where I_{OH} = –1.2mA	V_{DD}d – 0.8			V
		V_{OL1}	Pull-in current where I_{OL} = 2.4mA			0.4	V
Output voltage 1	H1, H2	V_{OH2}	Feed current where I_{OH} = –22.0mA	V_{DD}b – 0.8			V
		V_{OL2}	Pull-in current where I_{OL} = 14.4mA			0.4	V
Output voltage 2	RG	V_{OH3}	Feed current where I_{OH} = –3.3mA	V_{DD}a – 0.8			V
		V_{OL3}	Pull-in current where I_{OL} = 2.4mA			0.4	V
Output voltage 3	XSHP, XSHD, XRS, PBLK, CLPOB, CLPDM, ADCLK	V_{OH4}	Feed current where I_{OH} = –3.3mA	V_{DD}c – 0.8			V
		V_{OL4}	Pull-in current where I_{OL} = 2.4mA			0.4	V
Output voltage 4	CKO	V_{OH5}	Feed current where I_{OH} = –6.9mA	V_{DD}d – 0.8			V
		V_{OL5}	Pull-in current where I_{OL} = 4.8mA			0.4	V
Output voltage 5	MCKO	V_{OH6}	Feed current where I_{OH} = –3.3mA	V_{DD}d – 0.8			V
		V_{OL6}	Pull-in current where I_{OL} = 2.4mA			0.4	V
Output voltage 6	ID, WEN	V_{OH7}	Feed current where I_{OH} = –2.4mA	V_{DD}d – 0.8			V
		V_{OL7}	Pull-in current where I_{OL} = 4.8mA			0.4	V
Output current 1	V1A, V1B, V3A, V3B, V2, V4	I_{OL}	V1A/B, V2, V3A/B, V4 = –8.25V	10.0			mA
		I_{OM1}	V1A/B, V2, V3A/B, V4 = –0.25V			–5.0	mA
		I_{OM2}	V1A/B, V3A/B = 0.25V	5.0			mA
		I_{OH}	V1A/B, V3A/B = 14.75V			–7.2	mA
Output current 2	SUB	I_{OSL}	SUB = –8.25V	5.4			mA
		I_{OSH}	SUB = 14.75V			–4.0	mA

*1 This input pin is a schmitt trigger input and it does not have protective diode of the power supply side in the IC.
*2 These input pins are schmitt trigger inputs.
*3 These input pins are with pull-down resistor in the IC.
*4 These input pins are with pull-down resistor in the IC and they do not have protective diode of the power supply side in the IC.

Note) The above table indicates the condition for 3.3V drive.

Inverter I/O Characteristics for Oscillation (Within the recommended operating conditions)

Item	Pins	Symbol	Conditions	Min.	Typ.	Max.	Unit
Logical Vth	OSCI	LVth			$V_{DD}d/2$		V
Input voltage	OSCI	V_{IH}		$0.7V_{DD}d$			V
		V_{IL}				$0.3V_{DD}d$	V
Output voltage	OSCO	V_{OH}	Feed current where I_{OH} = –3.6mA	$V_{DD}d$ – 0.8			V
		V_{OL}	Pull-in current where I_{OL} = 2.4mA			0.4	V
Feedback resistor	OSCI, OSCO	RFB	$V_{IN} = V_{DD}d$ or V_{SS}	500k	2M	5M	Ω
Oscillation frequency	OSCI, OSCO	f		20		50	MHz

Inverter Input Characteristics for Base Oscillation Clock Duty Adjustment

(Within the recommended operating conditions)

Item	Pins	Symbol	Conditions	Min.	Typ.	Max.	Unit
Logical Vth	CKI	LVth			$V_{DD}d/2$		V
Input voltage		V_{IH}		$0.7V_{DD}d$			V
		V_{IL}				$0.3V_{DD}d$	V
Input amplitude		V_{IN}	fmax 50MHz sine wave	0.3			Vp-p

Note) Input voltage is the input voltage characteristics for direct input from an external source. Input amplitude is the input amplitude characteristics in the case of input through a capacitor.

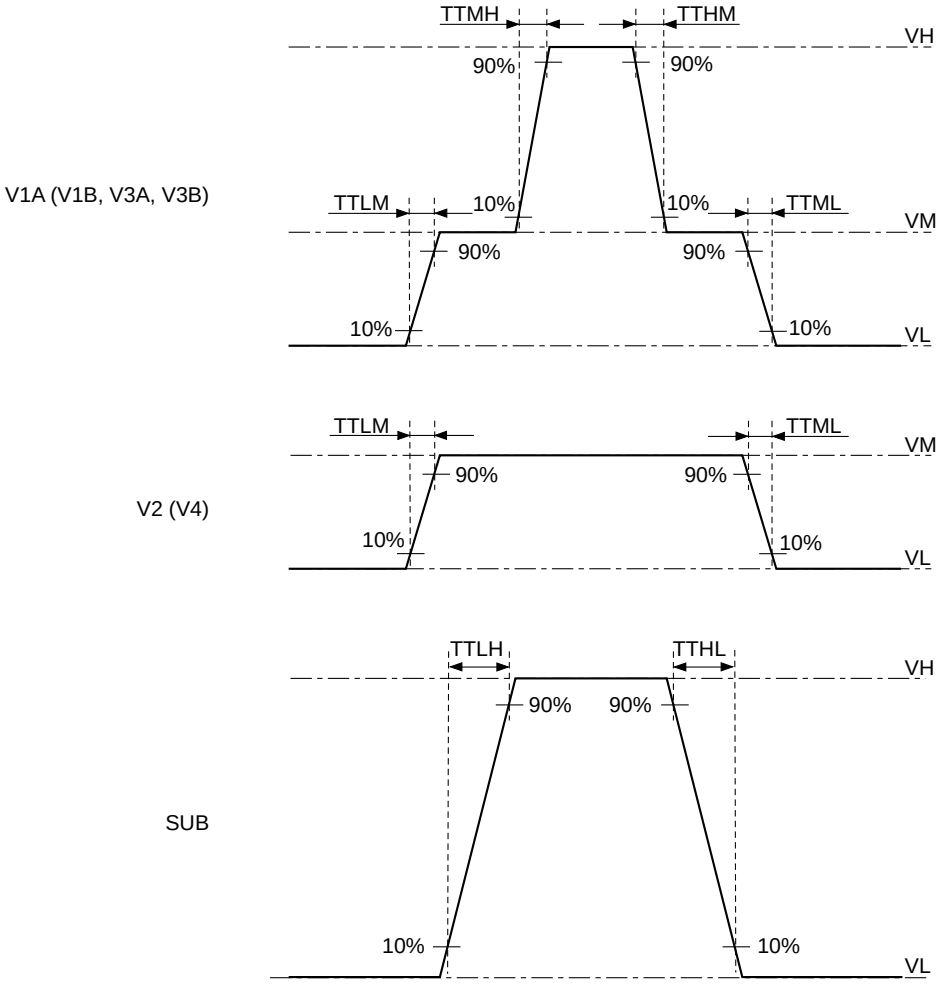
Switching Characteristics (VH = 15.0V, VM = GND, VL = –7.5V)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Rise time	TTLM	VL to VM	200	350	500	ns
	TTMH	VM to VH	200	350	500	ns
	TTLH	VL to VH	30	60	90	ns
Fall time	TTML	VM to VL	200	350	500	ns
	TTHM	VH to VM	200	350	500	ns
	TTHL	VH to VL	30	60	90	ns
Output noise voltage	VCLH				1.0	V
	VCLL				1.0	V
	VCMH				1.0	V
	VCML				1.0	V

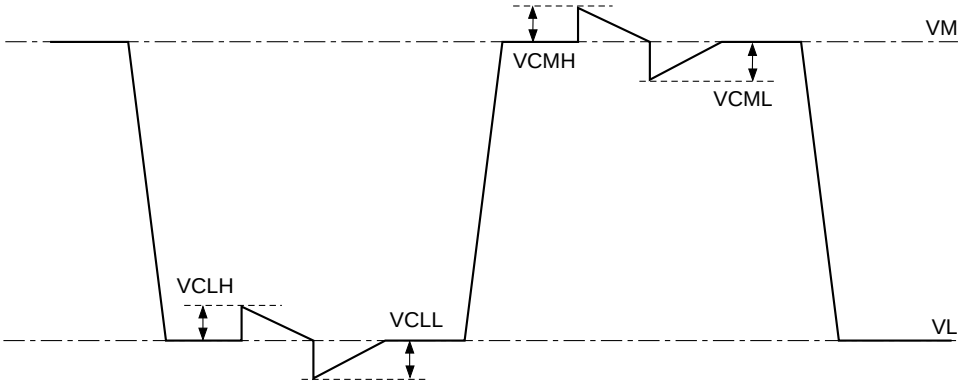
Notes)

1. The MOS structure of this IC has a low tolerance for static electricity, so full care should be given for measures to prevent electrostatic discharge.
2. For noise and latch-up countermeasures, be sure to connect a by-pass capacitor (0.1µF or more) between each power supply pin (VH, VL) and GND.
3. To protect the CCD image sensor, clamp the SUB pin output at VH before input to the CCD image sensor.

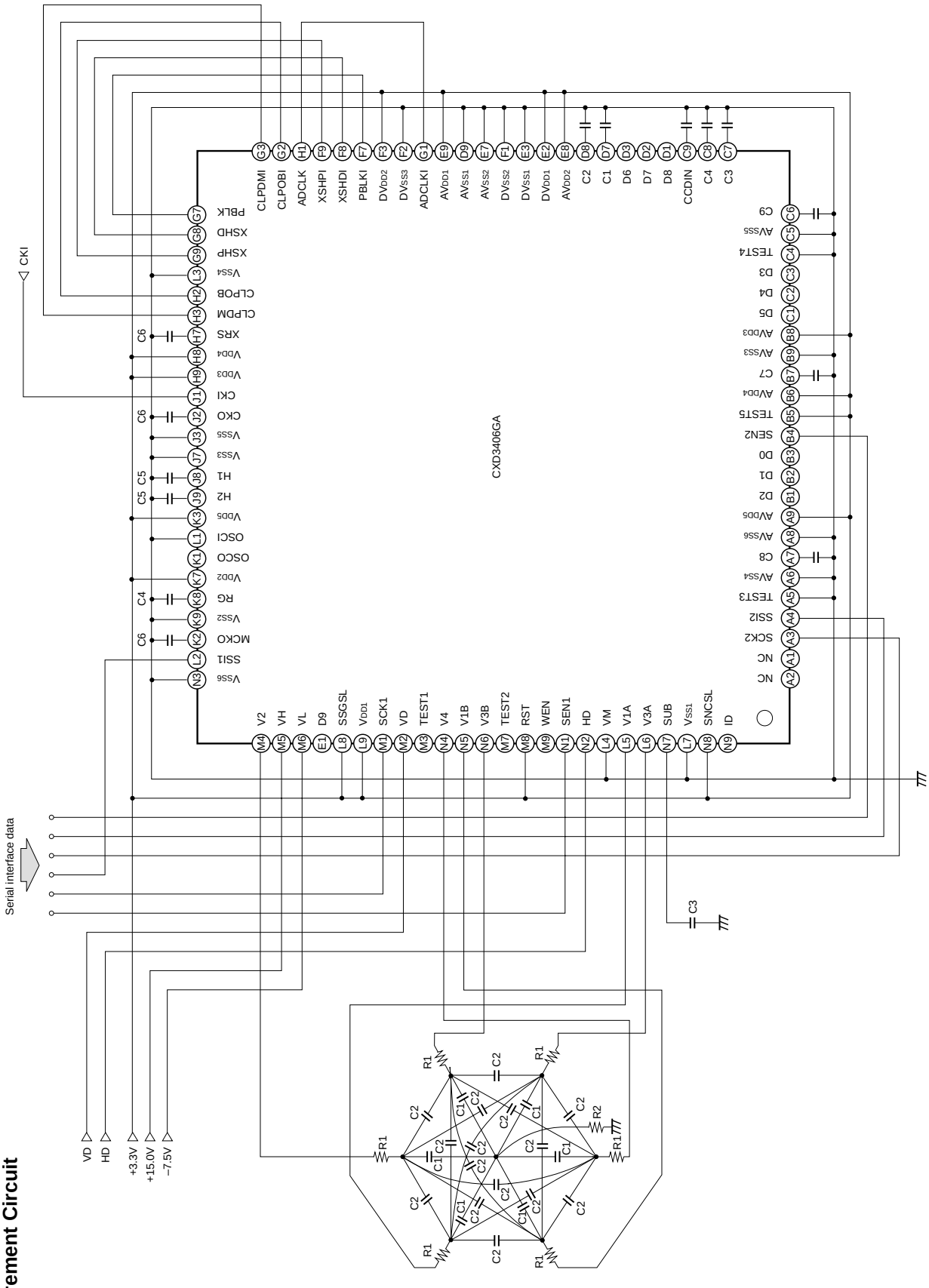
Switching Waveforms



Waveform Noise

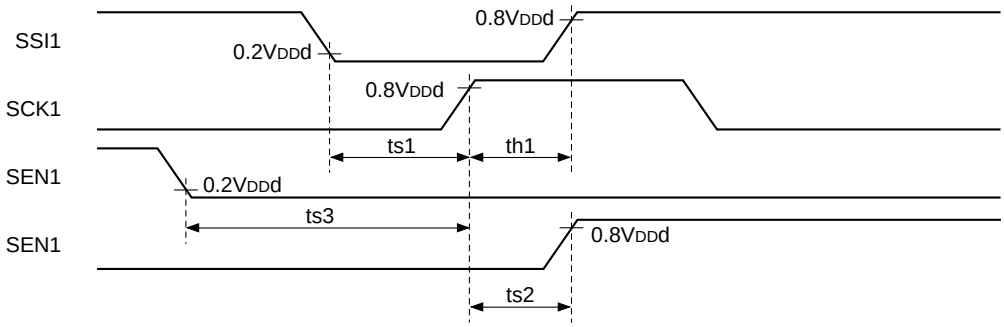


Measurement Circuit



AC Characteristics

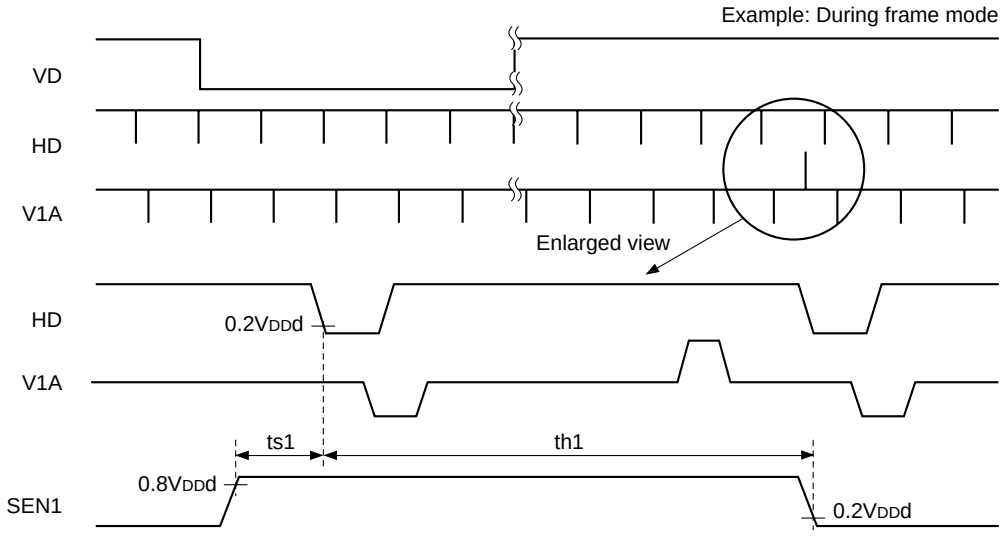
AC characteristics between the serial interface clocks



(Within the recommended operating conditions)

Symbol	Definition	Min.	Typ.	Max.	Unit
ts1	SSI1 setup time, activated by the rising edge of SCK1	20			ns
th1	SSI1 hold time, activated by the rising edge of SCK1	20			ns
ts2	SCK1 setup time, activated by the rising edge of SEN1	20			ns
ts3	SEN1 setup time, activated by the rising edge of SCK1	20			ns

Serial interface clock internal loading characteristics (1)

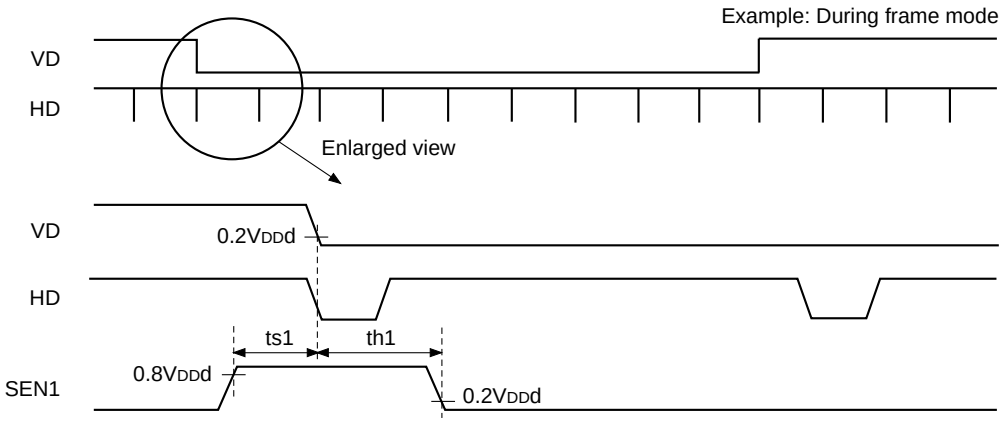


* Be sure to maintain a constantly high SEN1 logic level near the falling edge of the HD in the horizontal period during which V1A/B and V3A/B values take the ternary value and during that horizontal period.

(Within the recommended operating conditions)

Symbol	Definition	Min.	Typ.	Max.	Unit
ts1	SEN1 setup time, activated by the falling edge of HD	0			ns
th1	SEN1 hold time, activated by the falling edge of HD	102			µs

Serial interface clock internal loading characteristics (2)



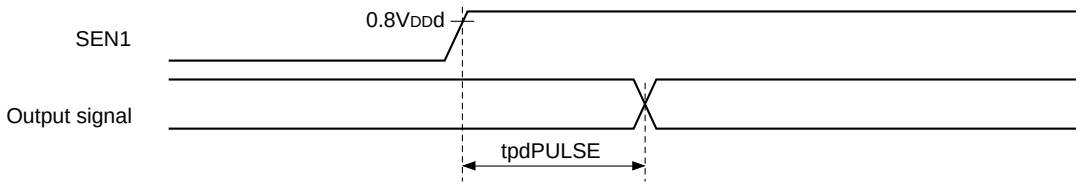
* Be sure to maintain a constantly high SEN1 logic level near the falling edge of VD.

(Within the recommended operating conditions)

Symbol	Definition	Min.	Typ.	Max.	Unit
ts1	SEN1 setup time, activated by the falling edge of VD	0			ns
th1	SEN1 hold time, activated by the falling edge of VD	200			ns

Serial interface clock output variation characteristics

Normally, the serial interface data is loaded to the CXD3406GA at the timing shown in "Serial interface clock internal loading characteristics (1)" above. However, one exception to this is when the data such as STB is loaded to the CXD3406GA and controlled at the rising edge of SEN1. See "Description of Operation".



(Within the recommended operating conditions)

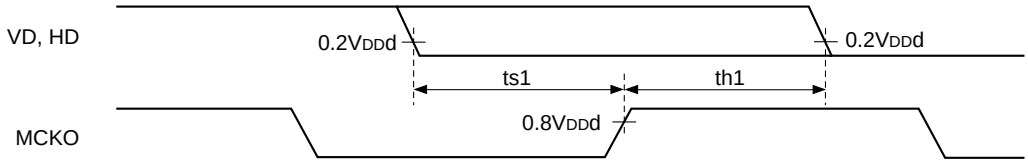
Symbol	Definition	Min.	Typ.	Max.	Unit
tpdPULSE	Output signal delay, activated by the rising edge of SEN1	5		100	ns

RST loading characteristics

(Within the recommended operating conditions)

Symbol	Definition	Min.	Typ.	Max.	Unit
tw1	RST pulse width	35			ns

VD and HD loading characteristics

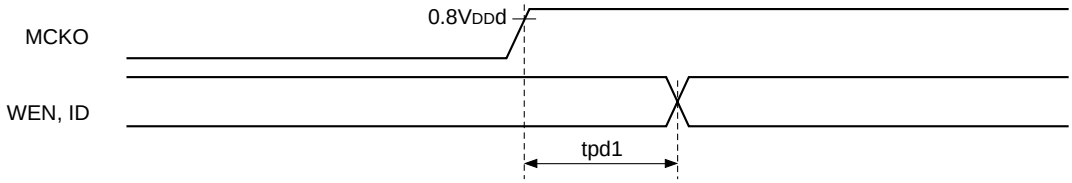


MCKO load capacitance = 10pF

(Within the recommended operating conditions)

Symbol	Definition	Min.	Typ.	Max.	Unit
ts1	VD and HD setup time, activated by the rising edge of MCKO	20			ns
th1	VD and HD hold time, activated by the rising edge of MCKO	5			ns

Output variation characteristics



WEN and ID load capacitance = 10pF

(Within the recommended operating conditions)

Symbol	Definition	Min.	Typ.	Max.	Unit
tpd1	Time until the above outputs change after the rise of MCKO	20		60	ns

CCD Signal Processor Block Electrical Characteristics

DC Characteristics

(Fc = 18MSPS, $DV_{DD1, 2}$ = $AV_{DD1, 2, 3, 4, 5}$ = 3.3V, Ta = 25°C)

Item	Pins	Symbol	Conditions	Min.	Typ.	Max.	Unit
Supply voltage 1	DV_{DD1}	$V_{DD}e$		3.0	3.3	3.6	V
Supply voltage 2	DV_{DD2}	$V_{DD}f$		3.0	3.3	3.6	V
Supply voltage 3	AV_{DD1}, AV_{DD2}, AV_{DD3}, AV_{DD4}, AV_{DD5}	$V_{DD}g$		3.0	3.3	3.6	V
Analog input capacitance	CCDIN	C_{IN}			15		pF
Input voltage	SCK2, SSI2, SEN2, TEST3, TEST4, XSHDI, XSHPI, ADCLKI, CLPOBI, CLPDMI, PBLKI	V_{I+}			1.8		V
		V_{I-}			1.1		V
A/D clock duty	ADCLKI				50		%
Output voltage	D0 to D9	V_{OH}	Feed current where I_{OH} = –2.0mA	$V_{DD}e$ – 0.9			V
		V_{OL}	Pull-in current where I_{OL} = 2.0mA			0.4	V

Analog Characteristics

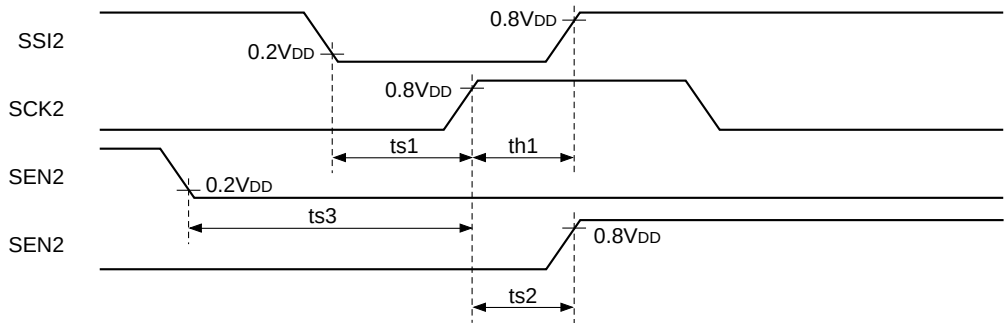
(Fc = 18MSPS, $DV_{DD1, 2}$ = $AV_{DD1, 2, 3, 4, 5}$ = 3.3V, Ta = 25°C)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
CCDIN input voltage amplitude	V_{IN}	PGA gain = 0dB, output full scale	900		1100	mV
PGA maximum gain	Gmax	PGA gain setting data = "3FFh"		42		dB
PGA minimum gain	Gmin	PGA gain setting data = "000h"		–6		dB
ADC resolution				10		bit
ADC maximum conversion rate	Fc max		18			MHz
ADC integral non-linearity error	E_L	PGA gain = 0dB		±1.0	±5.0	LSB
ADC differential non-linearity error	E_D	PGA gain = 0dB		±0.5	±1.0	LSB
Signal-to-noise ratio	SNR*1	CCDIN input connected to GND via a coupling capacitor PGA gain = 0dB		62		dB
CCDIN input voltage clamp level	CLP			1.5		V
CCD optical black signal clamp level	OB	OBLVL = "8h" PGA gain = 0dB		32		LSB

*1 SNR = 20 log (full-scale voltage/rms noise)

AC Characteristics

AC characteristics between the serial interface clocks

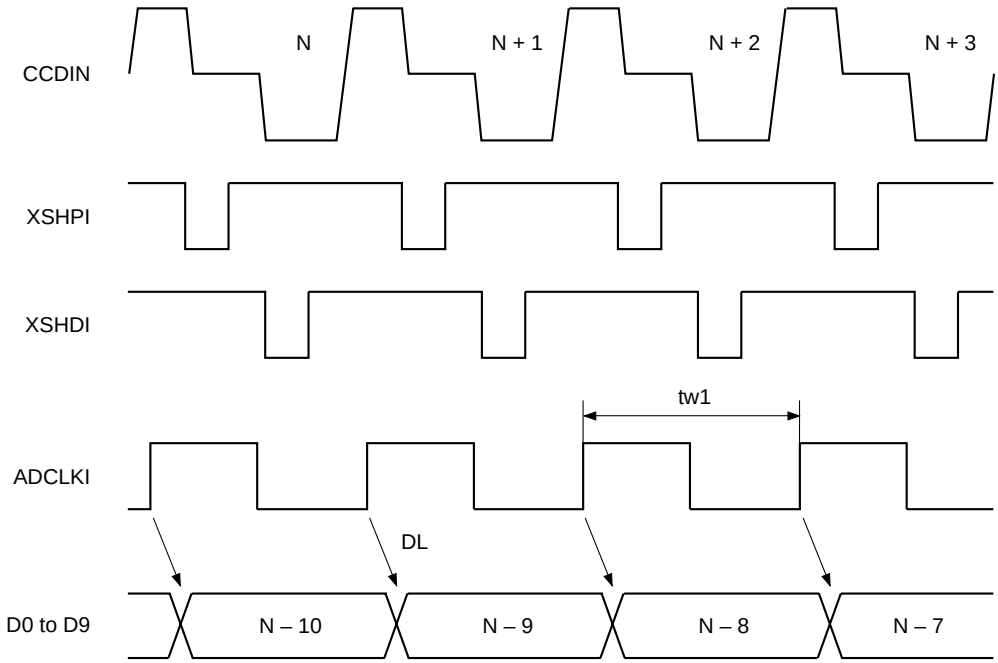


* The setting values are reflected to the operation 5 or 6 ADCLKI clocks after the serial data is loaded at the rise of SEN2.

(Fc = 18MSPS, $DV_{DD1, 2}$ = $AV_{DD1, 2, 3, 4, 5}$ = 3.3V, Ta = 25°C)

Symbol	Definition	Min.	Typ.	Max.	Unit
tp1	SCK2 clock period	100			ns
ts1	SSI2 setup time, activated by the rise of SCK2	30			ns
th1	SSI2 hold time, activated by the rise of SCK2	30			ns
ts2	SCK2 setup time, activated by the rise of SEN2	30			ns
ts3	SEN2 setup time, activated by the rise of SCK2	30			ns

CDS/ADC Timing Chart

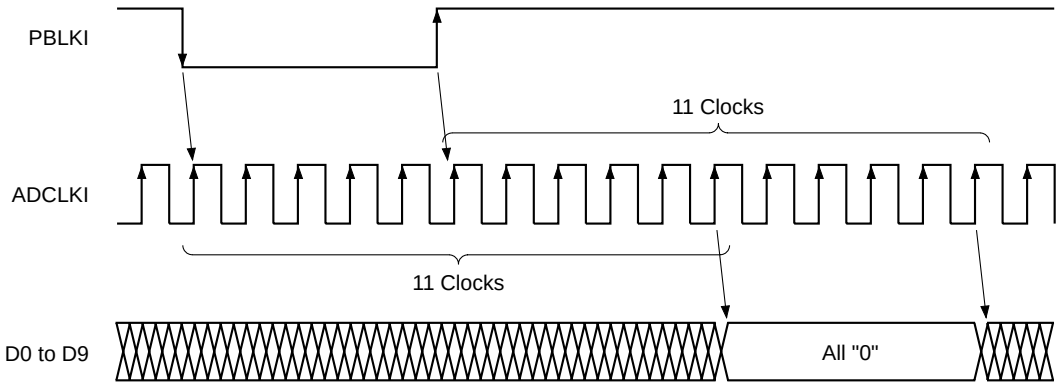


* Set the input pulse polarity setting data D13, D14 and D15 of the serial interface data to "0".

(Fc = 18MSPS, $DV_{DD1, 2}$ = $AV_{DD1, 2, 3, 4, 5}$ = 3.3V, Ta = 25°C)

Symbol	Definition	Min.	Typ.	Max.	Unit
tw1	ADCLKI clock period	54			ns
	ADCLKI clock duty		50		%
DL	Data latency		9		clocks

Preblanking Timing Chart



Description of Operation

Pulses output from the CXD3406GA's timing generator block are controlled mainly by the RST pin and by the serial interface data. The Pin Status Table is shown below, and the details of serial interface control are described on page 19 and thereafter.

Pin Status Table

Pin No.	Symbol	CAM	SLP	STB	RST	Pin No.	Symbol	CAM	SLP	STB	RST
A1	NC	—				D3	D6	—			
A2	NC	—				D7	C1	—			
A3	SCK2	—				D8	C2	—			
A4	SSI2	—				D9	AV_{SS1}	—			
A5	TEST3	—				E1	D9	—			
A6	AV_{SS4}	—				E2	DV_{DD1}	—			
A7	C8	—				E3	DV_{SS1}	—			
A8	AV_{SS6}	—				E7	AV_{SS2}	—			
A9	AV_{DD5}	—				E8	AV_{DD2}	—			
B1	D2	—				E9	AV_{DD1}	—			
B2	D1	—				F1	DV_{SS2}	—			
B3	D0	—				F2	DV_{SS3}	—			
B4	SEN2	—				F3	DV_{DD2}	—			
B5	TEST5	—				F7	PBLKI	—			
B6	AV_{DD4}	—				F8	XSHDI	—			
B7	C7	—				F9	XSHPI	—			
B8	AV_{DD3}	—				G1	ADCLKI	—			
B9	AV_{SS3}	—				G2	CLPOBI	—			
C1	D5	—				G3	CLPDMI	—			
C2	D4	—				G7	PBLK	ACT	L	L	H
C3	D3	—				G8	XSHD	ACT	L	L	ACT
C4	TEST4	—				G9	XSHP	ACT	L	L	ACT
C5	AV_{SS5}	—				H1	ADCLK	ACT	L	L	ACT
C6	C9	—				H2	CLPOB	ACT	L	L	H
C7	C3	—				H3	CLPDM	ACT	L	L	H
C8	C4	—				H7	XRS	ACT	L	L	ACT
C9	CCDIN	—				H8	V_{DD4}	—			
D1	D8	—				H9	V_{DD3}	—			
D2	D7	—				J1	CKI	ACT	ACT	ACT	ACT

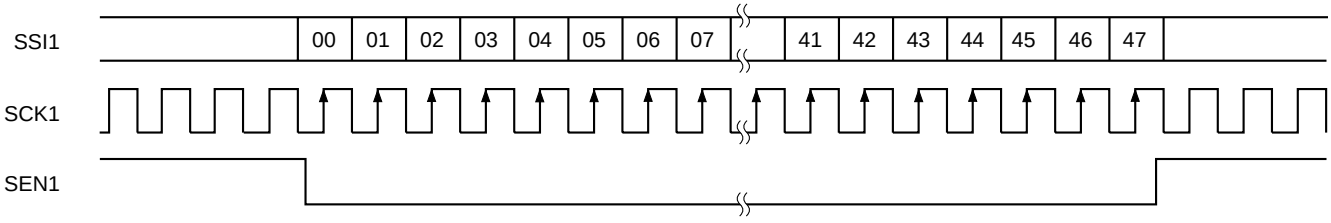
Pin No.	Symbol	CAM	SLP	STB	RST	Pin No.	Symbol	CAM	SLP	STB	RST
J2	CKO	ACT	ACT	L	ACT	L9	V_{DD1}	—			
J3	V_{SS5}	—				M1	SCK1	ACT	ACT	ACT	DIS
J7	V_{SS3}	—				M2	VD*1	ACT	L	L	H
J8	H1	ACT	L	L	ACT	M3	TEST1	—			
J9	H2	ACT	L	L	ACT	M4	V2	ACT	VM	VM	VM
K1	OSCO	ACT	ACT	ACT	ACT	M5	VH	—			
K2	MCKO	ACT	ACT	L	ACT	M6	VL	—			
K3	V_{DD5}	—				M7	TEST2	—			
K7	V_{DD2}	—				M8	RST	ACT	ACT	ACT	L
K8	RG	ACT	L	L	ACT	M9	WEN	ACT	L	L	L
K9	V_{SS2}	—				N1	SEN1	ACT	ACT	ACT	DIS
L1	OSCI	ACT	ACT	ACT	ACT	N2	HD*1	ACT	L	L	H
L2	SSI1	ACT	ACT	ACT	DIS	N3	V_{SS6}	—			
L3	V_{SS4}	—				N4	V4	ACT	VM	VM	VL
L4	VM	—				N5	V1B	ACT	VH	VH	VM
L5	V1A	ACT	VH	VH	VM	N6	V3B	ACT	VH	VH	VL
L6	V3A	ACT	VH	VH	VL	N7	SUB	ACT	VH	VH	VL
L7	V_{SS1}	—				N8	SNCSL	ACT	ACT	ACT	ACT
L8	SSGSL	ACT	ACT	ACT	ACT	N9	ID	ACT	L	L	L

*1 It is for output. For input, all items are "ACT".

Note) ACT means that the circuit is operating, and DIS means that loading is stopped.
L indicates a low output level, and H a high output level in the controlled status.
Also, VH, VM and VL indicate the voltage levels applied to VH (Pin M5), VM (Pin L4) and VL (Pin M6), respectively, in the controlled status.

Timing Generator Block Serial Interface Control

The CXD3406GA's timing generator block basically loads and reflects the timing generator block serial interface data sent in the following format in the readout portion at the falling edge of HD. Here, readout portion specifies the horizontal period during which V1A/B and V3A/B, etc. take the ternary value.
Note that some items reflect the timing generator block serial interface data at the falling edge of VD or the rising edge of SEN1.



There are two categories of timing generator block serial interface data: CXD3406GA timing generator block drive control data (hereafter "control data") and electronic shutter data (hereafter "shutter data").
The details of each data are described below.

Control Data

Data	Symbol	Function	Data = 0	Data = 1	RST
D00 to D07	CHIP	Chip enable	10000001 → Enabled Other values → Disabled		All 0
D08 to D09	CTG	Category switching	See D08 to D09 CTG.		All 0
D10 to D12	MODE	Drive mode switching	See D10 to D12 MODE.		All 0
D13 to D14	SMD	Electronic shutter mode switching	See D13 to D14 SMD.		All 0
D15	PTSG	Internal SSG output pattern switching	NTSC equivalent	PAL equivalent	0
D16 to D23	CDAT	AF drive control data	See D16 to D23 CDAT.		All 0
D24 to D33	—	—	—	—	All 0
D34	—	—	—	—	1
D35	—	—	—	—	0
D36 to D37	LDAD	ADCLK logic phase switching	See D36 to D37 LDAD.		1 0
D38 to D39	STB	Standby control	See D38 to D39 STB.		All 0
D40 to D47	—	—	—	—	All 0

Shutter Data

Data	Symbol	Function	Data = 0	Data = 1	RST
D00 to D07	CHIP	Chip enable	10000001 → Enabled Other values → Disabled		All 0
D08 to D09	CTG	Category switching	See D08 to D09 CTG.		All 0
D10 to D19	SVD	Electronic shutter vertical period specification	See D10 to D19 SVD.		All 0
D20 to D31	SHD	Electronic shutter horizontal period specification	See D20 to D31 SHD.		All 0
D32 to D41	SPL	High-speed shutter position specification	See D32 to D41 SPL.		All 0
D42 to D47	—	—	—	—	All 0

Detailed Description of Each Data

Shared data: D08 to D09 CTG [Category]

Of the data provided to the CXD3406GA by the timing generator block serial interface, the CXD3406GA loads D10 and subsequent data to each data register as shown in the table below according to the combination of D08 and D09.

D09	D08	Description of operation
0	0	Loading to control data register
0	1	Loading to shutter data register
1	X	Test mode

Note that the CXD3406GA can apply these categories consecutively within the same vertical period. However, care should be taken as the data is overwritten if the same category is applied.

Control data: D10 to D12 MODE [Drive mode]

The CXD3406GA timing generator block drive mode can be switched as follows. However, the drive mode bits are loaded to the CXD3406GA and reflected at the falling edge of VD.

D12	D11	D10	Description of operation
0	0	0	Draft mode (sextuple speed: default)
0	0	1	Frame mode (A field readout)
0	1	0	Frame mode (B Field readout)
0	1	1	Frame mode
1	0	X	AF1 mode
1	1	X	AF2 mode

Control data: D15 PTSG [Internal SSG output pattern]

The CXD3406GA internal SSG output pattern can be switched as follows. However, the drive mode bits are loaded to the CXD3406GA and reflected at the falling edge of VD.

D15	Description of operation
0	NTSC equivalent pattern
1	PAL equivalent pattern

The VD period in each pattern is defined as follows for each drive mode.

	Frame mode	Draft mode	AF1 mode	AF2 mode
NTSC equivalent pattern	918H + 1716ck	262H + 1144ck	131H + 572ck	65H + 1430ck
PAL equivalent pattern	945H*1	314H + 1568ck	157H + 784ck	78H + 1536ck

*1 Only 944H and 945H are 1208ck period.

See the Timing Charts for the actual operation.

Control data: D36 to D37 LDAD [ADCLK logic phase]

This indicates the ADCLK logic phase adjustment data. The default is 90° relative to MCKO.

D37	D36	Degree of adjustment (°)
0	0	0
0	1	90
1	0	180
1	1	270

Control data: D38 to D39 STB [Standby]

The operating mode of the timing generator block is switched as follows. However, the standby bits are loaded to the CXD3406GA and control is applied immediately at the rising edge of SEN1.

D39	D38	Symbol	Operating mode
X	0	CAM	Normal operating mode
0	1	SLP	Sleep mode
1	1	STB	Standby mode

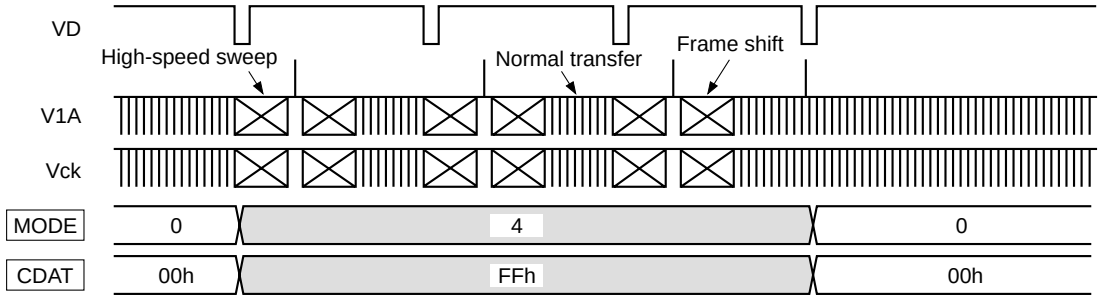
See the Pin Status Table for the pin status in each mode.

Control data: [AF drive]

The CXD3406GA controls the drive of the vertical cut-out area of the line in AF1/AF2 mode by using control data D16 to D23 CDAT. This mode has a function on purpose to raise frame rate for auto focus (AF), and cannot support operation such as electrical image stabilization.

The AF drive bits are loaded to the CXD3406GA and reflected at the falling edge of VD. As shown in the figure below, first, the fixed stage is swept at high speed, and it goes to readout period and vertical OB period. Then normal transfer is performed equivalent to draft mode from the frame shift to the stage specified by the serial interface data to the timing of the falling edge of the next VD.

Therefore, the number of frame shift stages applied to CDAT and the control by VD period are conditions for its application.



The number of high-speed sweep are different according to the selected mode. They are specified as follows.

AF1 mode: 138 stages (0 to 7H)
AF2 mode: 208 stages (0 to 11H)

The frame shift data is expressed as shown in the table below using D16 to D23 CDAT.

MSB							LSB
D23	D22	D21	D20	D19	D18	D17	D16
0	1	1	0	1	0	0	1
	↓				↓		
	6				9		

CDAT is expressed as 69h .

Its definition area is specified as follows.

AF1 mode: 00h ≤ CDAT ≤ FFh (11 to 23H)
AF2 mode: 00h ≤ CDAT ≤ FFh (14 to 27H)

Control data/shutter data: [Electronic shutter]

The CXD3406GA realizes various electronic shutter functions by using control data D13 to D14 SMD and shutter data D10 to D19 SVD, D20 to D31 SHD and D32 to D41 SPL.

These functions are described in detail below.

First, the various modes are shown below.

These modes are switched using control data D13 to D14 SMD.

D14	D13	Description of operation
0	0	Electronic shutter stopped mode
0	1	High-speed/low-speed shutter mode
1	0	
1	1	HTSG control mode

The electronic shutter data is expressed as shown in the table below using D20 to D31 SHD as an example. However, MSB (D31) is a reserve bit for the future specification, and it is handled as a dummy on this IC.

MSB											LSB
D31	D30	D29	D28	D27	D26	D25	D24	D23	D22	D21	D20
X	0	0	1	1	1	0	0	0	0	1	1
	↓				↓				↓		
	1				C				3		

SHD is expressed as 1C3h.

[Electronic shutter stopped mode]

During this mode, all shutter data items are invalid.

SUB is not output in this mode, so the shutter speed is the accumulation time for one field.

[High-speed/low-speed shutter mode]

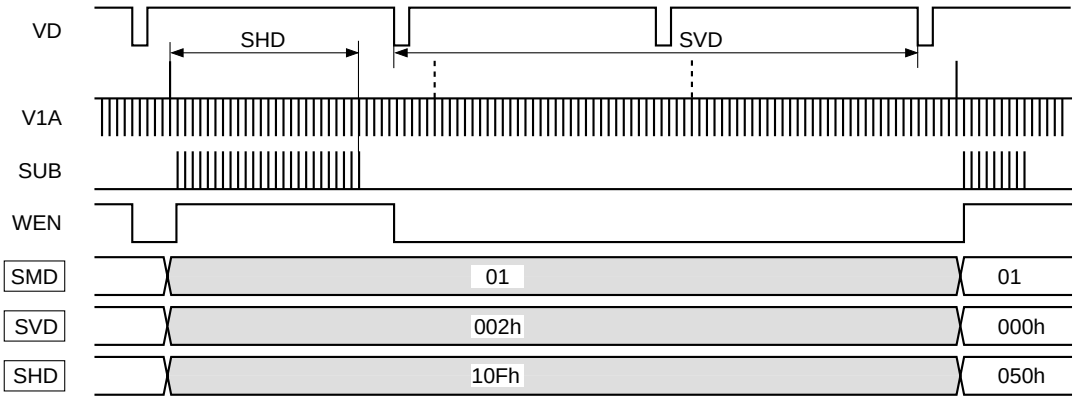
During this mode, the shutter data items have the following meanings.

Symbol	Data	Description
SVD	D10 to D19	Number of vertical periods specification (000h ≤ SVD ≤ 3FFh)
SHD	D20 to D31	Number of horizontal periods specification (000h ≤ SHD ≤ 7FFh)
SPL	D32 to D41	Vertical period specification for high-speed shutter operation (000h ≤ SPL ≤ 3FFh)

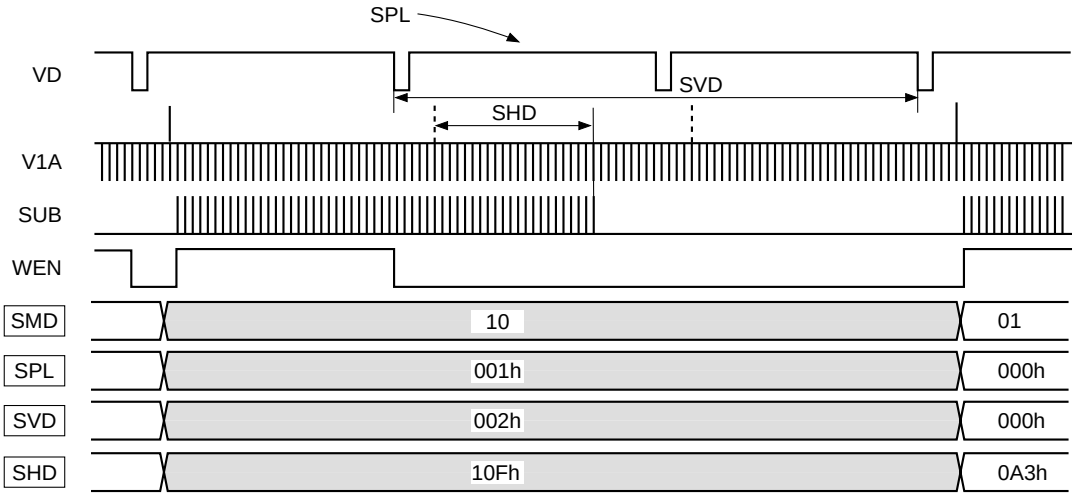
The period during which SVD and SHD are specified together is the shutter speed. Concretely, when specifying high-speed shutter, SVD is set to "000h". (See the figure.) During low-speed shutter, or in other words when SVD is set to "001h" or higher, the serial interface data is not loaded until this period is finished.

The vertical period indicated here corresponds to one field in each drive mode. In addition, the number of horizontal periods applied to SHD can be considered as (number of SUB pulses – 1). However, in the frame mode A field, it matches (number of SUB pulses + 1). This is a specification for flickerless when the same mode is repeated. But this change may not occur because of flickerless depending on the conditions during low-speed shutter.

Note) The bit data definition area is assured in terms of the CXD3406GA functions, and does not assure the CCD characteristics.



Further, SPL can be used during this mode to specify the SUB output at the desired vertical period during the low-speed shutter period.
In the case below, SUB is output based on SHD at the SPL vertical period out of (SVD + 1) vertical periods.



Incidentally, SPL is counted as "000h", "001h", "002h" and so on in conformance with SVD.
Using this function, it is possible to achieve smooth exposure time transitions when changing from low-speed shutter to high-speed shutter or vice-versa.

[HTSG control mode]

During this mode, all shutter data items are invalid.

The V1A/B and V3A/B ternary level outputs are stopped, so the shutter speed is the value obtained by adding the shutter speed specified in the preceding vertical period to the vertical period during which these readout pulses are stopped as shown in the figure.

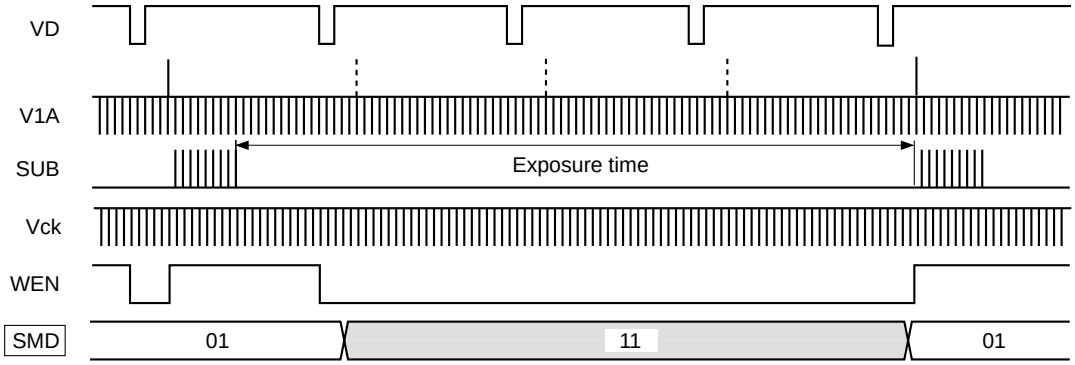
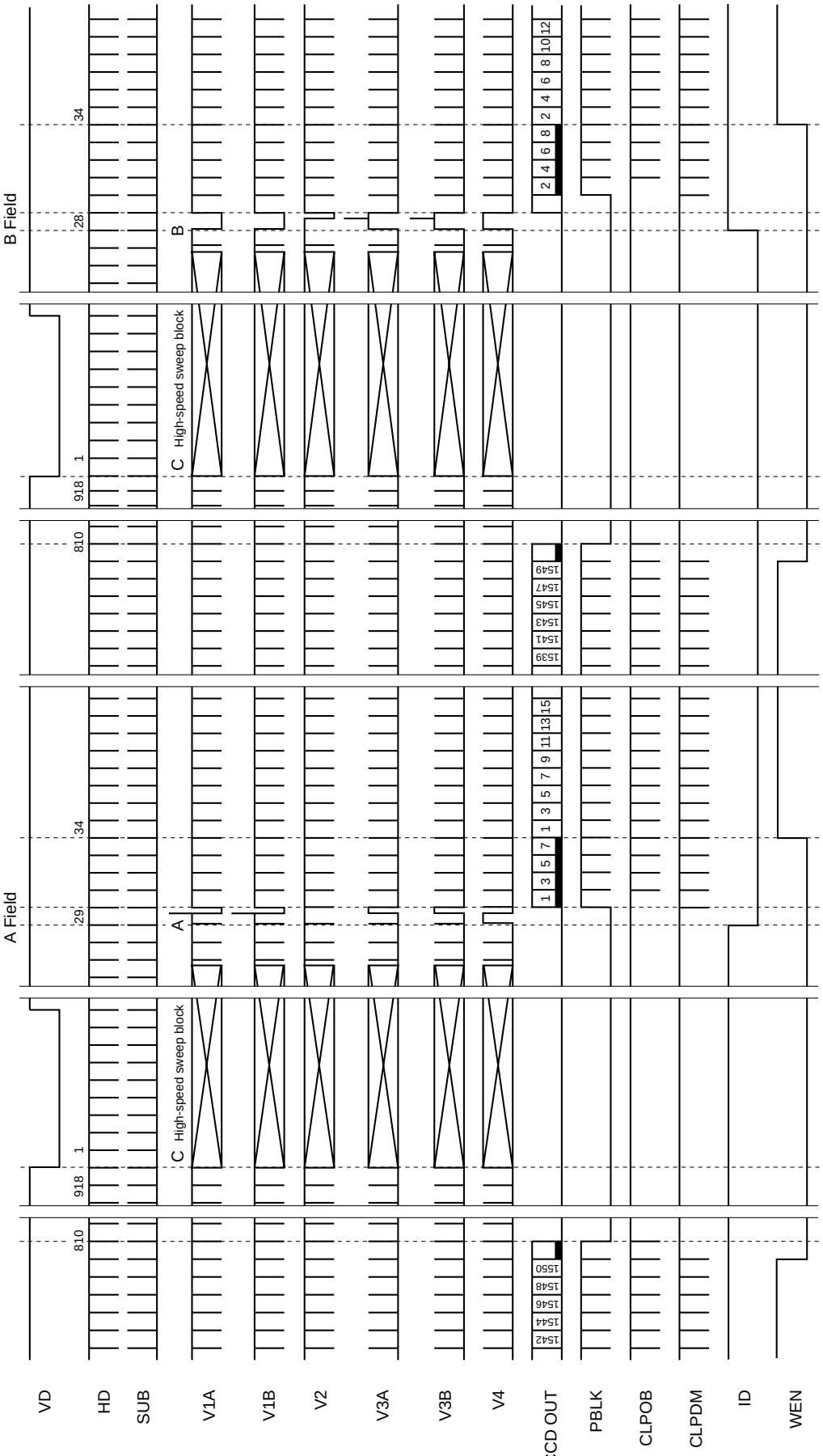


Chart-1 Vertical Direction Timing Chart

MODE
Frame mode

Applicable CCD image sensor
• ICX252/262



* The number of SUB pulses is determined by the serial interface data. This chart shows the case where SUB pulses are output in each horizontal period.
* * ID is low for lines where CCD OUT contains the R component, and high for lines where CCD OUT contains the B component.
* * * VD of this chart is NTSC equivalent pattern (918H + 1716ck units). For PAL equivalent pattern, it is 945H units, but 1208ck period only for 944H and 945H.

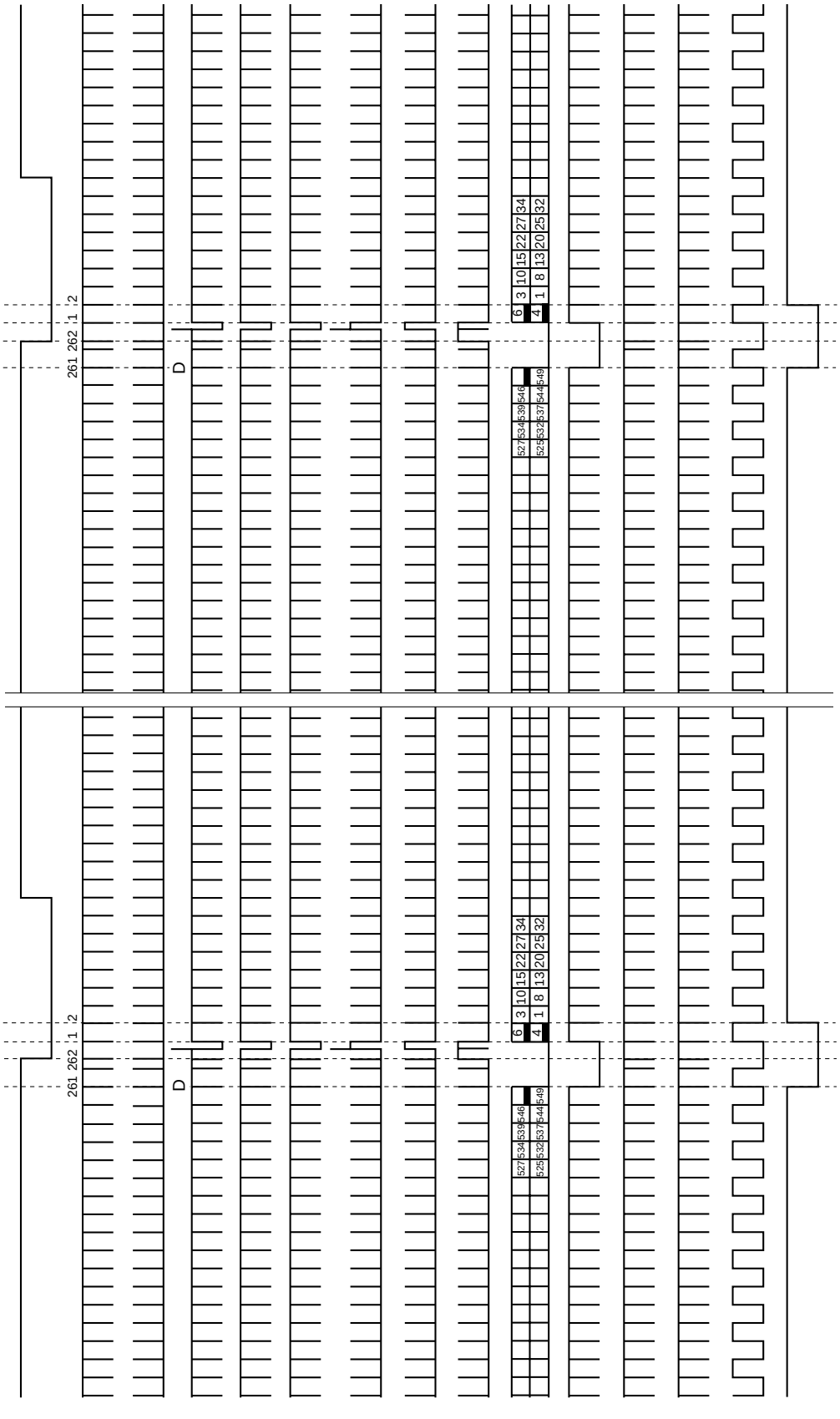
Chart-2 Vertical Direction Timing Chart

MODE

Draft mode

Applicable CCD image sensor

• ICX252/262



* The number of SUB pulses is determined by the serial interface data. This chart shows the case where SUB pulses are output in each horizontal period.
* ID is low for lines where CCD OUT contains the R component, and high for lines where CCD OUT contains the B component.
* VD of this chart is NTSC equivalent pattern (262H + 1144ck units). For PAL equivalent pattern, it is 314H + 1568ck units.

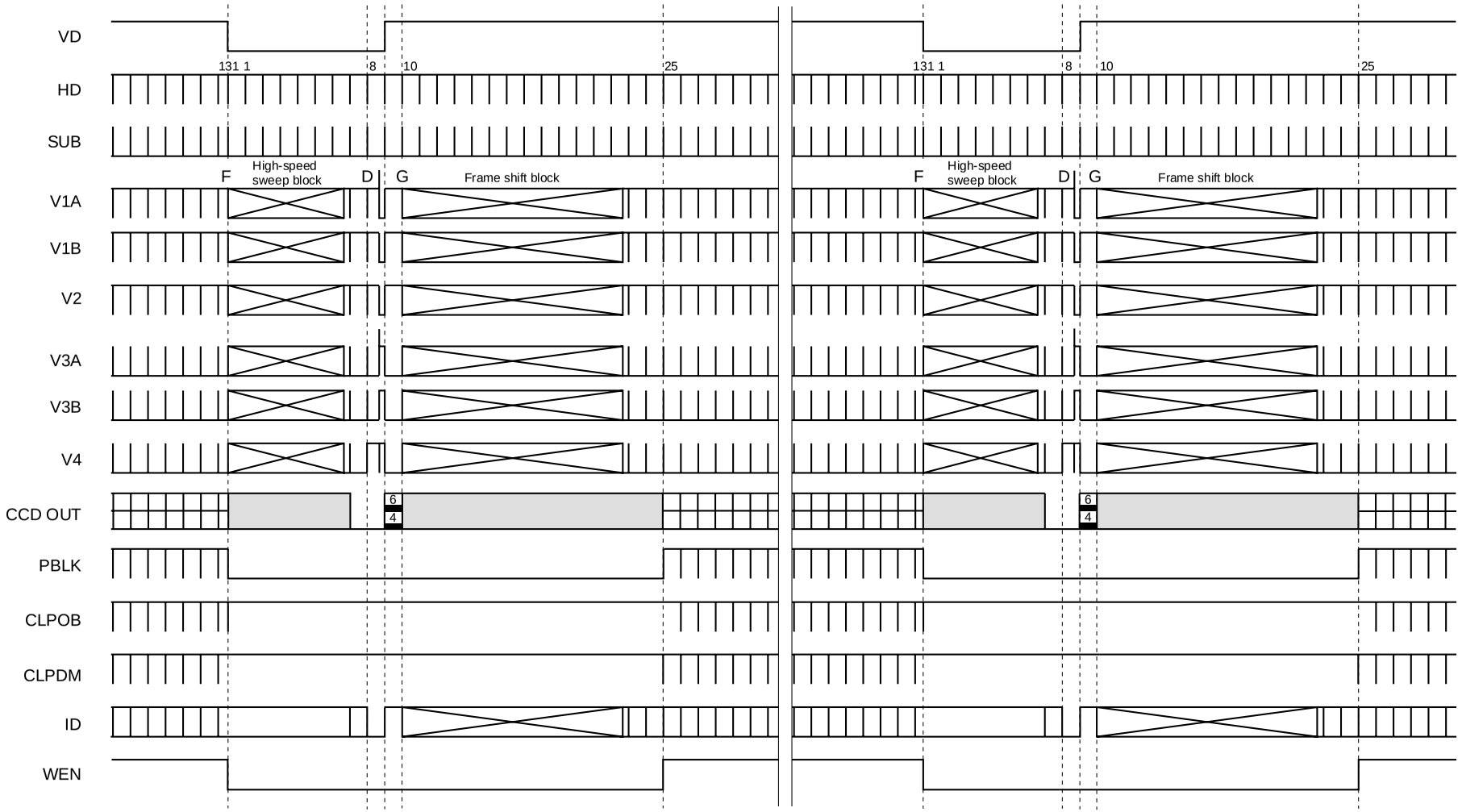
Chart-3 Vertical Direction Timing Chart

MODE

AF1 mode

Applicable CCD image sensor

• ICX252/262



* The number of SUB pulses is determined by the serial interface data. This chart shows the case where SUB pulses are output in each horizontal period.
* ID is low for lines where CCD OUT contains the R component, and high for lines where CCD OUT contains the B component.
* 138 stages are fixed for high-speed sweep block ; 0 to 255 stages can be specified by the serial interface for the frame shift block.
* VD of this chart is NTSC equivalent pattern (131H + 572ck units). For PAL equivalent pattern, it is 157H + 784ck units.

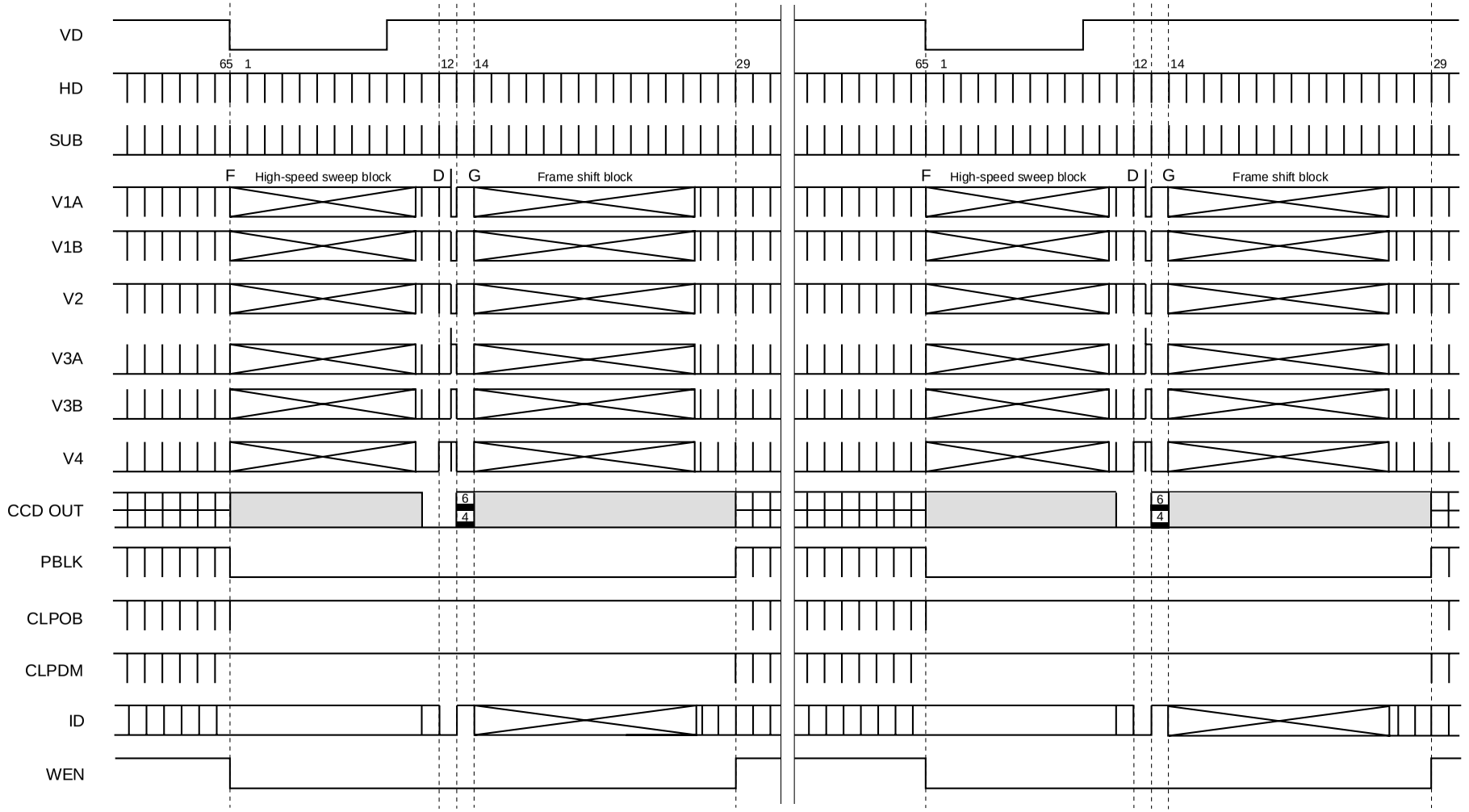
Chart-4 Vertical Direction Timing Chart

MODE

AF2 mode

Applicable CCD image sensor

• ICX252/262



* The number of SUB pulses is determined by the serial interface data. This chart shows the case where SUB pulses are output in each horizontal period.
* ID is low for lines where CCD OUT contains the R component, and high for lines where CCD OUT contains the B component.
* 208 stages are fixed for high-speed sweep block ; 0 to 255 stages can be specified by the serial interface for the frame shift block.
* VD of this chart is NTSC equivalent pattern (65H + 1430ck units). For PAL equivalent pattern, it is 78H + 1536ck units.

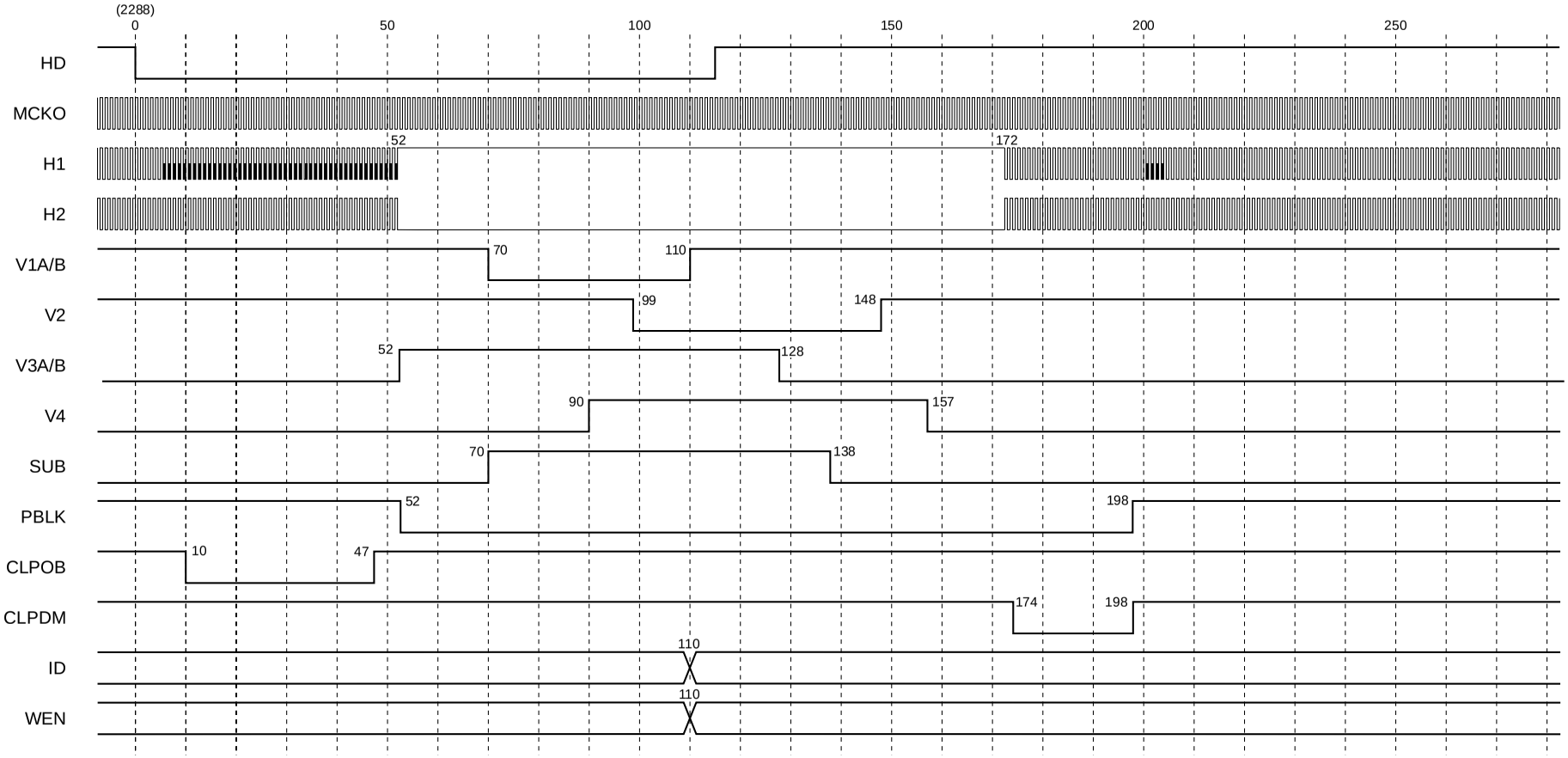
Chart-5 Horizontal Direction Timing Chart

MODE

Frame mode

Applicable CCD image sensor

• ICX252/262



* HD of this chart indicates the actual CXD3406GA load timing.
* The numbers at the output pulse transition points indicate the count at the MCKO rise from the fall of HD.
* The HD fall period should be between approximately 2.9 to 9.5µs (when the drive frequency is 18MHz). This chart shows a period of 115ck (6.4µs). Internal SSG is at this timing.
* SUB is output at this timing shown above when output is controlled by the serial interface data.
* ID and WEN are output at this timing shown above at the position shown in Chart-1.

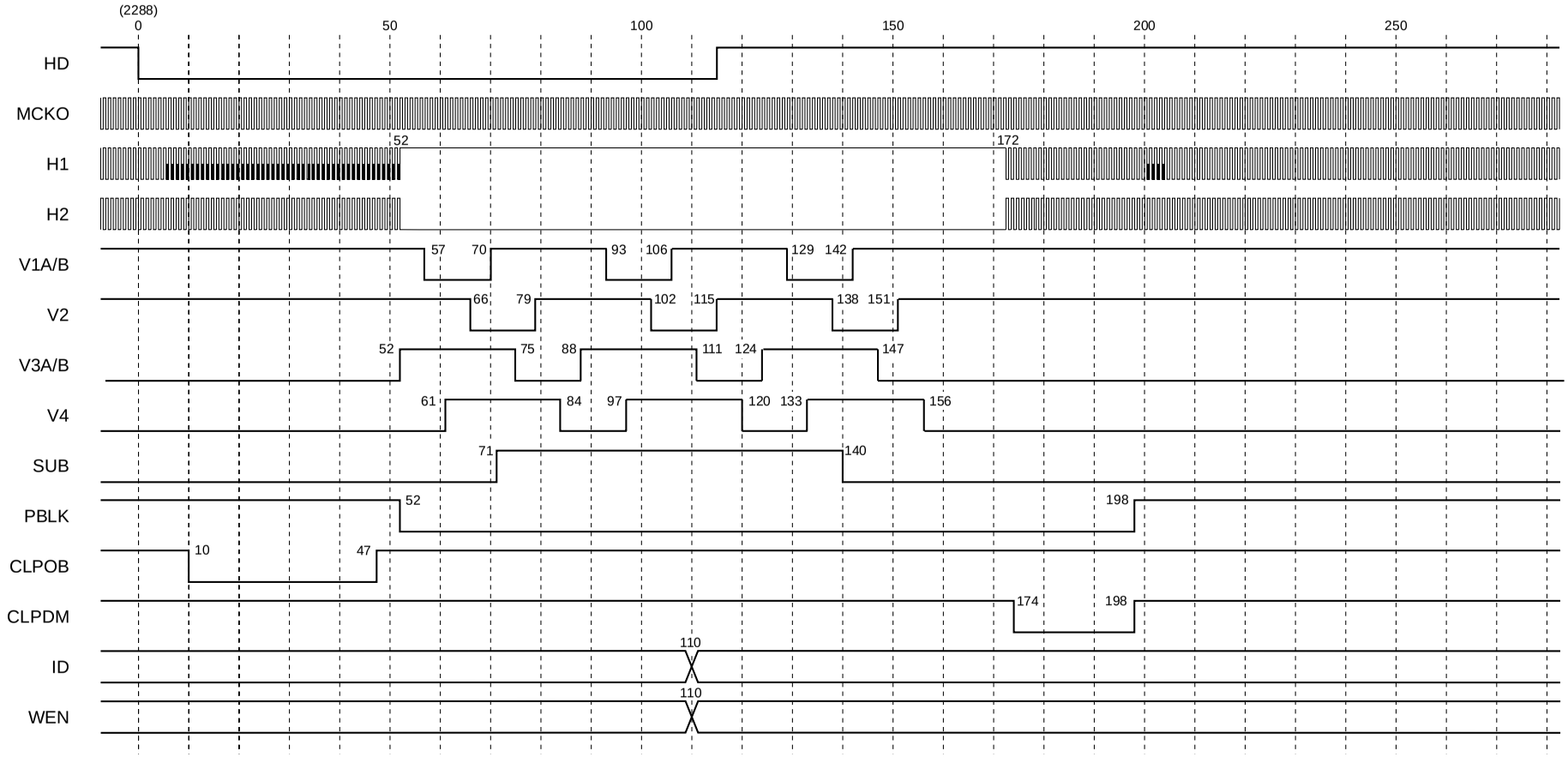
Chart-6 Horizontal Direction Timing Chart

MODE

Draft/AF1/AF2 mode

Applicable CCD image sensor

• ICX252/262



* HD of this chart indicates the actual CXD3406GA load timing.
* The numbers at the output pulse transition points indicate the count at the MCKO rise from the fall of HD.
* The HD fall period should be between approximately 2.9 to 9.5µs (when the drive frequency is 18MHz). This chart shows a period of 115ck (6.4µs). Internal SSG is at this timing.
* SUB is output at this timing shown above when output is controlled by the serial interface data.
* ID and WEN are output at this timing shown above at the position shown in Charts-2, 3 and 4.

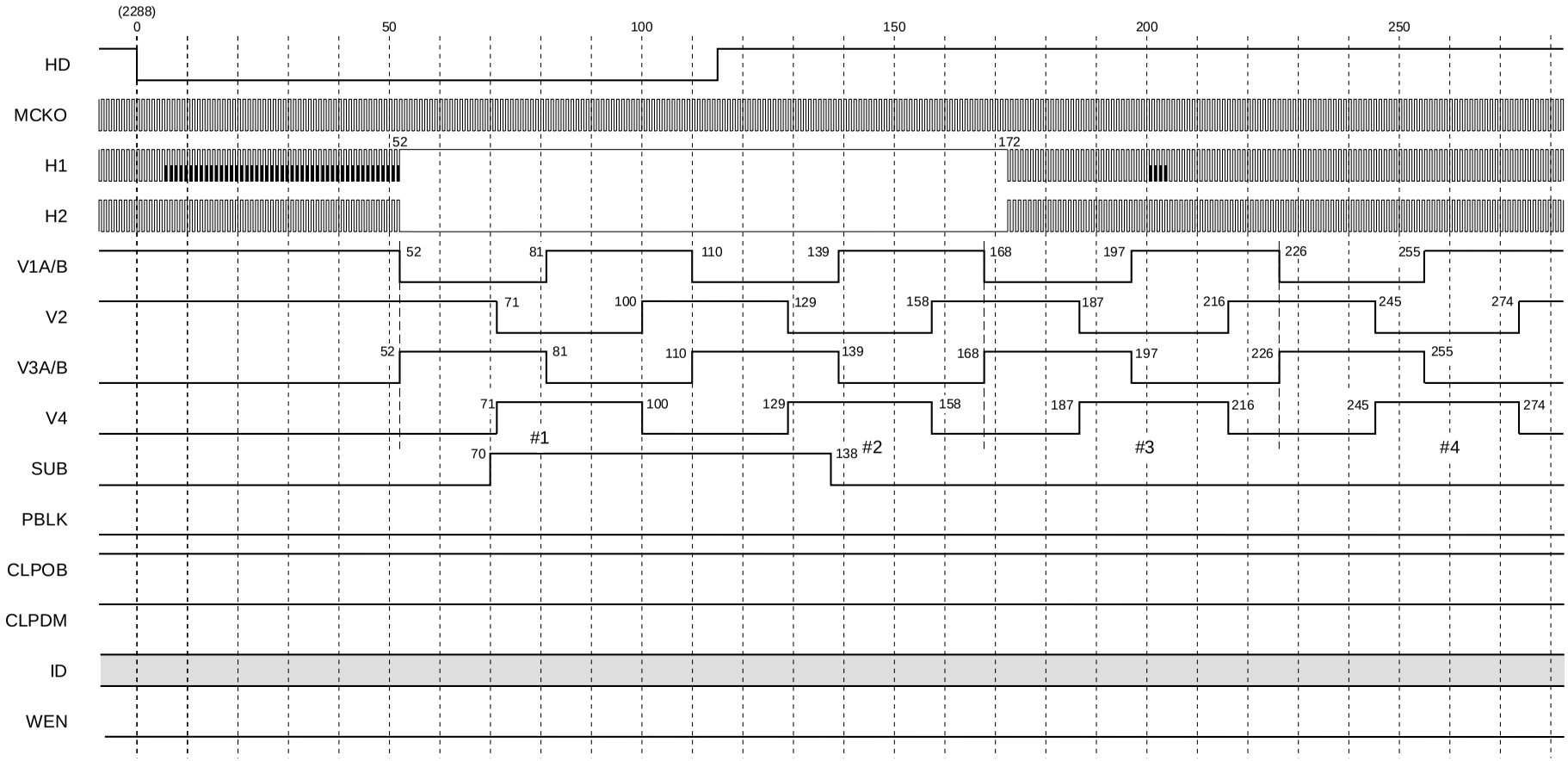
Chart-7 Horizontal Direction Timing Chart (High-speed sweep: C)

MODE

Frame mode

Applicable CCD image sensor

• ICX252/262



* HD of this chart indicates the actual CXD3406GA load timing.
* The numbers at the output pulse transition points indicate the count at the MCKO rise from the fall of HD.
* The HD fall period should be between approximately 2.9 to 9.5µs (when the drive frequency is 18MHz). This chart shows a period of 115ck (6.4µs). Internal SSG is at this timing.
* SUB is output at this timing shown above when output is controlled by the serial interface data.
* High-speed sweep of V1A/B, V2, V3A/B and V4 is performed up to 26H of 768ck(#1038).

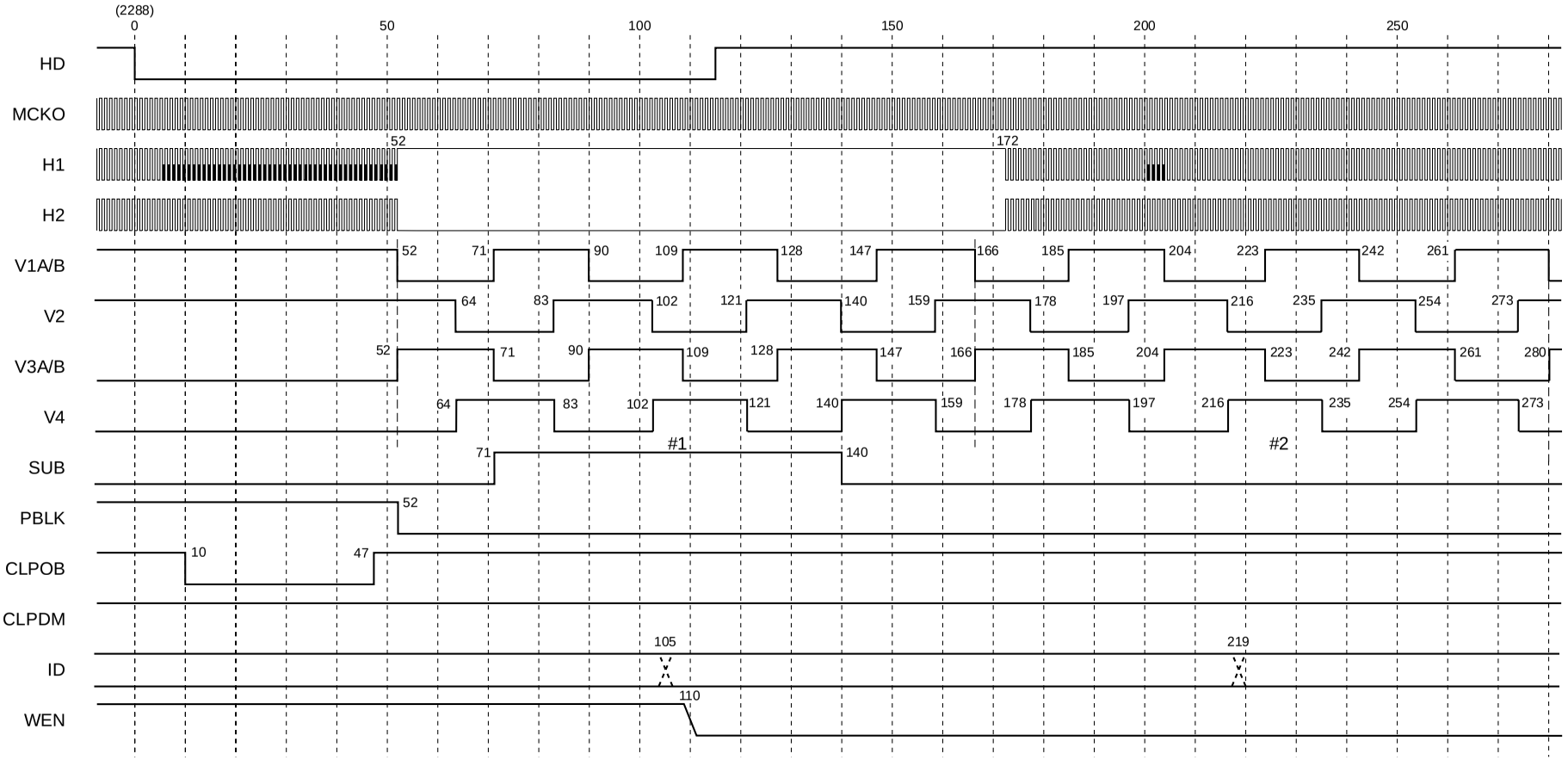
Chart-8 Horizontal Direction Timing Chart
(High-speed sweep: F)
(Frame shift: G)

MODE

AF1/AF2 mode

Applicable CCD image sensor

• ICX252/262



* HD of this chart indicates the actual CXD3406GA load timing.
* The numbers at the output pulse transition points indicate the count at the MCKO rise from the fall of HD.
* The HD fall period should be between approximately 2.9 to 9.5µs (when the drive frequency is 18MHz). This chart shows a period of 115ck (6.4µs). Internal SSG is at this timing.
* SUB is output at this timing shown above when output is controlled by the serial interface data.
* WEN is output at this timing shown above at the position shown in Chart-3 and 4.
* High-speed sweep of V1A/B, V2, V3A/B and V4 is performed up to 6H of 2056ck (#138) in AF1 mode and 10H of 884ck (#208) in AF2 mode.
* Frame shift of V1A/B, V2, V3A/B and V4 receives the output control by the serial interface data and can specify up to #255 for both of AF1/AF2 mode.
* ID is output at the timing shown with dotted line during frame shift.

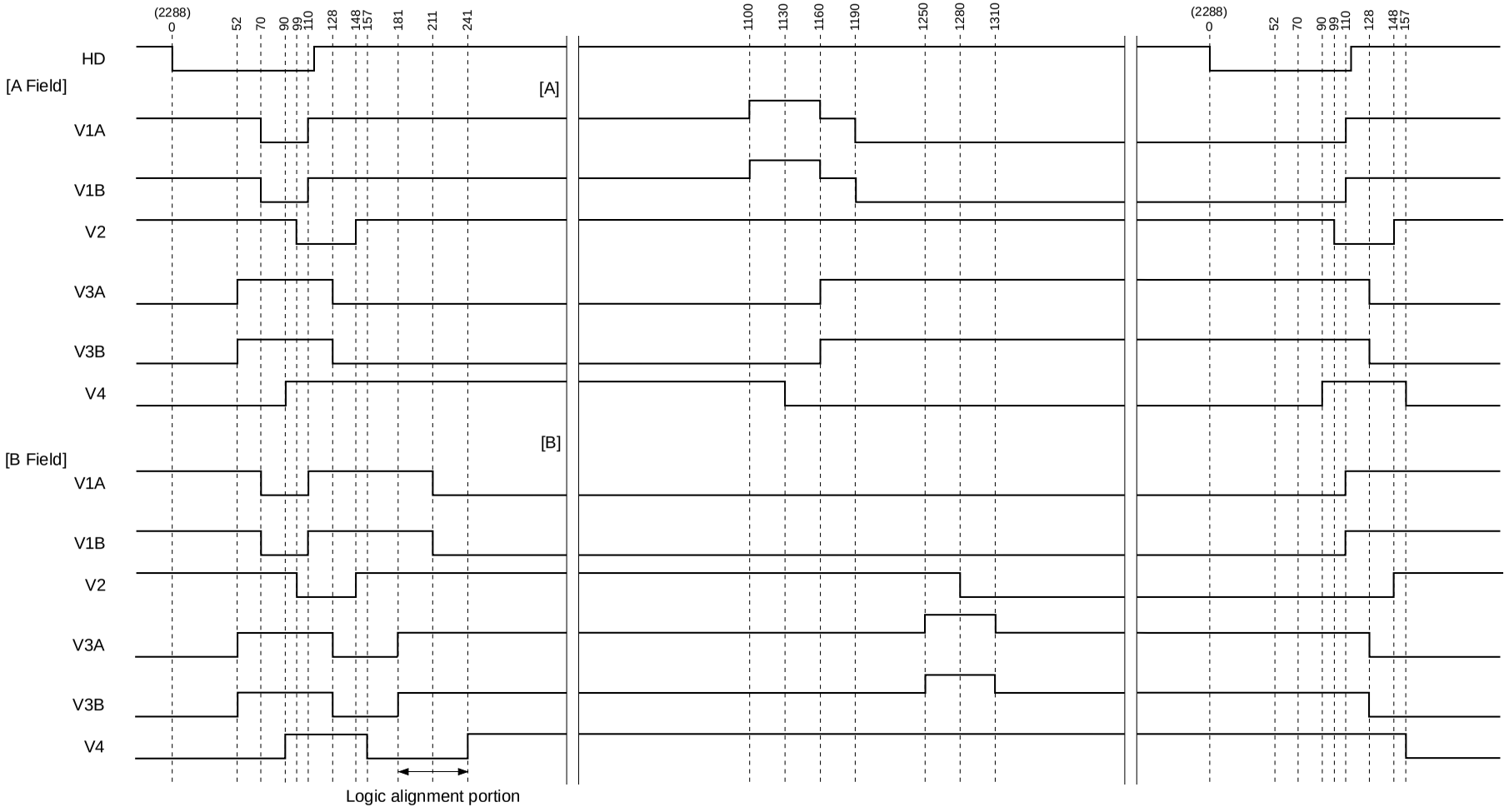
Chart-9 Horizontal Direction Timing Chart

MODE

Frame mode

Applicable CCD image sensor

• ICX252/262



* HD of this chart indicates the actual CXD3406GA load timing.

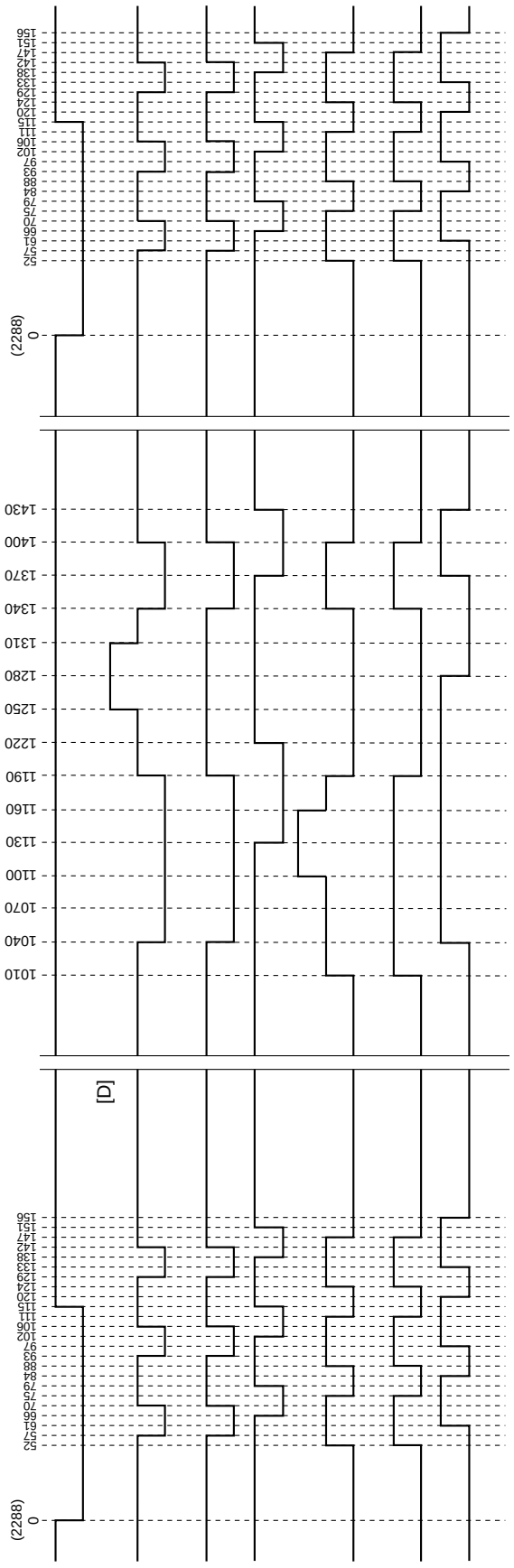
* The numbers at the output pulse transition points indicate the count at the MCKO rise from the fall of HD.

* The HD fall period should be between approximately 2.9 to 9.5µs (when the drive frequency is 18MHz). This chart shows a period of 115ck (6.4µs). Internal SSG is at this timing.

Chart-10 Horizontal Direction Timing Chart

MODE
Draft/AF1/AF2 mode

Applicable CCD image sensor
• ICX252/262



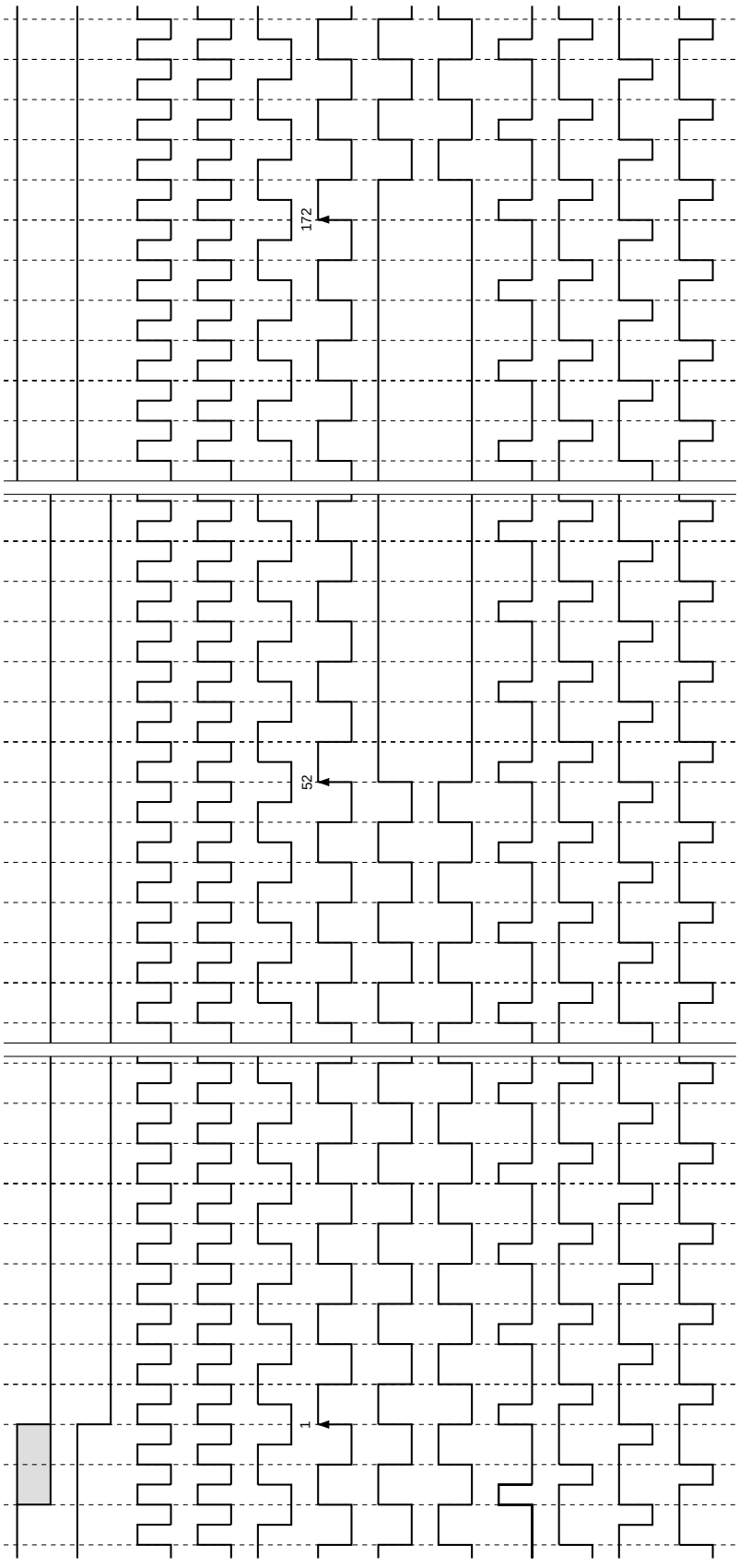
* HD of this chart indicates the actual CXD3406GA load timing.
* The numbers at the output pulse transition points indicate the count at the MCKO rise from the fall of HD.
* The HD fall period should be between approximately 2.9 to 9.5µs (when the drive frequency is 18MHz). This chart shows a period of 115ck (6.4µs). Internal SSG is at this timing.

Chart-11 High-Speed Phase Timing Chart

MODE

Applicable CCD image sensor

• ICX252/262



* HD' indicates the HD which is the actual CXD3406GA load timing.
* The phase relationship of each pulse shows the logical position relationship. For the actual output waveform, a delay is added to each pulse.
* The logical phase of ADCLK can be specified by the serial interface data.

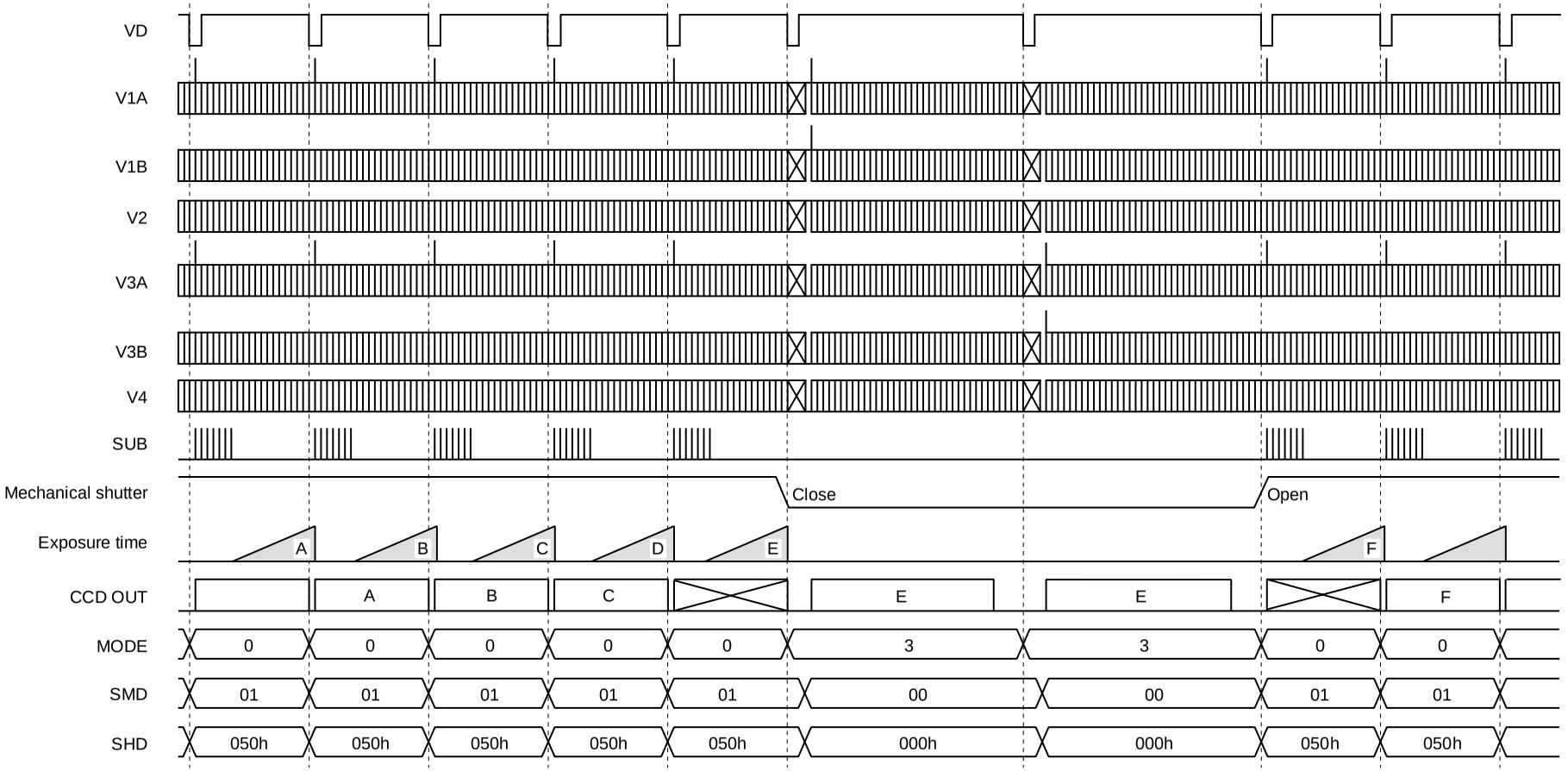
Chart-12 Vertical Direction Sequence Chart

MODE

Draft → Frame → Draft

Applicable CCD image sensor

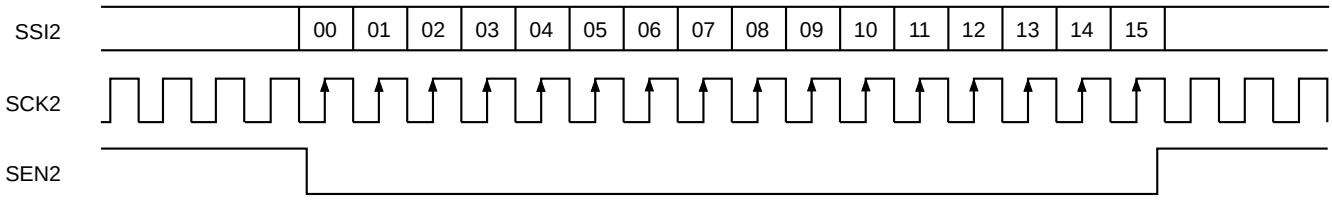
• ICX252/262



* This chart is a driving timing chart example of electronic shutter normal operation.
* Data exposed at D includes blooming component. For details, see the CCD image sensor Data Sheet.
* The CXD3406GA does not generate the pulse to control mechanical shutter operation.
* The switching timing of the drive mode and the electronic shutter data is not the same.

CCD Signal Processor Block Serial Interface Control

The CXD3406GA's CCD signal processor block basically loads the CCD signal processor block serial interface data sent in the following format at the rising edge of SEN2, and the setting values are then reflected to the operation 6 ADCLKI clocks after that.
CCD signal processor block serial interface control requires clock input to ADCLKI in order to load and reflect the serial interface data to operation, so this should normally be performed when the timing generator block is in the normal operation mode.



There are four categories of CCD signal processor block serial interface data: standby control data, PGA gain setting data, OB clamp level setting data, and input pulse polarity setting data.
Note that when data from multiple categories is loaded consecutively, the data for the category loaded last is valid and data from other categories is lost. When transferring data from multiple categories, raise SEN2 for each category and wait until the setting value 6 ADCKLI clocks after that has been reflected to operation, then transmit the next category.
The detail of each data are described below.

Standby Control Data

Data	Symbol	Function	Data = 0	Data = 1
D00	TEST	Test code	Set to 0.	
D01 to D03	CTG	Category switching	D01 to D03 CTG	
D04 to D14	FIXED	—	Set to All 0.	
D15	STB	Standby control	Normal operating mode	Standby mode

PGA Gain Setting Data

Data	Symbol	Function	Data = 0	Data = 1
D00	TEST	Test code	Set to 0.	
D01 to D03	CTG	Category switching	D01 to D03 CTG	
D04 to D05	FIXED	—	Set to All 0.	
D06 to D15	GAIN	PGA gain setting data	See D06 to D15 GAIN.	

OB Clamp Level Setting Data

Data	Symbol	Function	Data = 0	Data = 1
D00	TEST	Test code	Set to 0.	
D01 to D03	CTG	Category switching	D01 to D03 CTG	
D04 to D11	FIXED	—	Set to All 0.	
D12 to D15	OBLVL	OB clamp level setting data	See D12 to D15 OBLVL.	

Input Pulse Polarity Setting Data

Data	Symbol	Function	Data = 0	Data = 1
D00	TEST	Test code	Set to 0.	
D01 to D03	CTG	Category switching	D01 to D03 CTG	
D04 to D12	FIXED	—	Set to All 0.	
D13 to D15	POL	Input pulse polarity setting data	Set to All 0.	

Detailed Description of Each Data

Shared data: D01 to D03 CTG [Category]

Of the data provided to the CXD3406GA by the CCD signal processor block serial interface, the CXD3406GA loads D04 and subsequent data to each data register as shown in the table below according to the combination of D01 to D03 .

D01	D02	D03	Description of operation
0	0	0	Loading to standby control data register
0	0	1	Loading to PGA gain setting data register
0	1	0	Loading to OB clamp level setting data register
0	1	1	Loading to input pulse polarity setting data register
1	X	X	Access prohibited

Standby control data: D15 STB [Standby]

The operating mode of the CCD signal processor block is switched as follows. When the CCD signal processor block is in standby mode, only the serial interface is valid.

D15	Description of operation
0	Normal operating mode
1	Standby mode

PGA gain setting data: D06 to D15 GAIN [PGA gain]

The CXD3406GA can set the programmable gain amplifier (PGA) gain from –6dB to +42dB in 1024 steps by using PGA gain setting data D06 to D15 GAIN.

The PGA gain setting data is expressed as shown in the table below using D06 to D15 GAIN.

MSB									LSB
D06	D07	D08	D09	D10	D11	D12	D13	D14	D15
0	1	1	1	0	0	0	0	1	1
↓			↓				↓		
1			C				3		

GAIN is expressed as 1C3h .

For example, when GAIN is set to "000h", "080h", "220h", "348h" and "3FFh", the respective PGA gain setting values are –6dB, 0dB, +20dB, +34dB and +42dB.

OB clamp level setting data: D12 to D15 OBLVL [OB clamp level]

The CXD3406GA can set the OPB clamp output value from 0 to 60LSB in 4LSB steps by using CCD signal processor block control data D12 to D15 OBLVL.

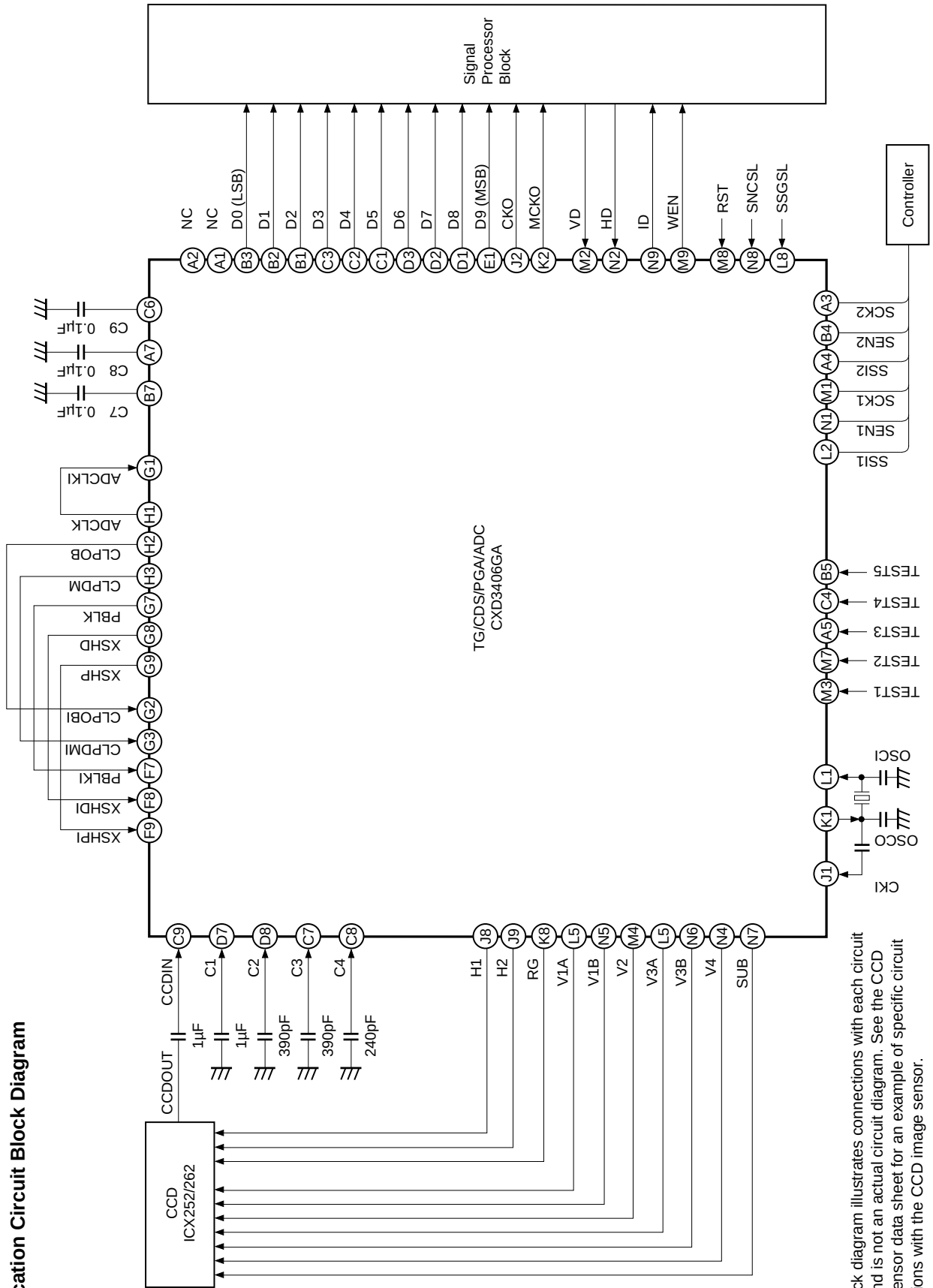
The OPB clamp output setting data is expressed as shown in the table below using D12 to D15 OBLVL.

MSB			LSB
D12	D13	D14	D15
0	1	1	0
	↓		
	6		

OBLVL is expressed as 6h .

For example, when OBLVL is set to "0h", "1h", "8h" and "Fh", the respective OPB clamp output setting values are 0LSB, 4LSB, 32LSB and 60LSB.

Application Circuit Block Diagram

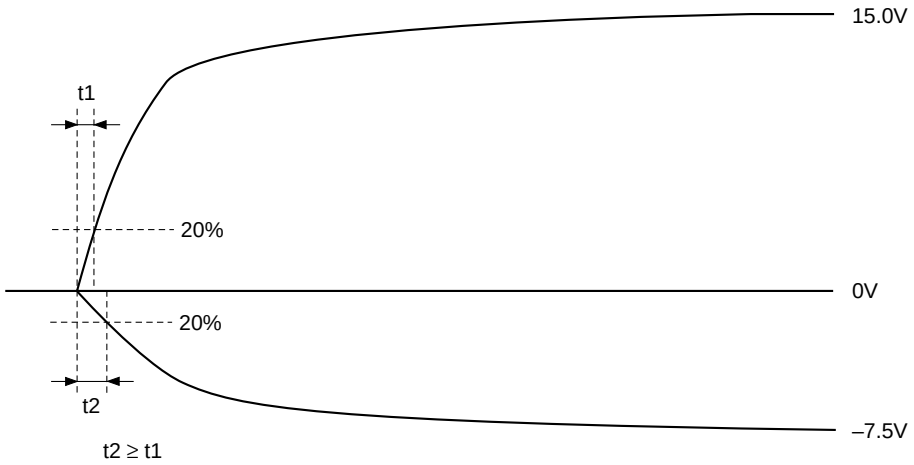


This block diagram illustrates connections with each circuit block, and is not an actual circuit diagram. See the CCD image sensor data sheet for an example of specific circuit connections with the CCD image sensor.

Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

Notes on Operation

1. Be sure to start up the timing generator block VL and VH pin power supplies at the timing shown in the figure below in order to prevent the SUB pin of the CCD image sensor from going to negative potential. In addition, start up the timing generator block V_{DD1}, V_{DD2}, V_{DD3}, V_{DD4} and V_{DD5} pin and CCD signal processor block DV_{DD1}, DV_{DD2}, AV_{DD1}, AV_{DD2}, AV_{DD3}, AV_{DD4} and AV_{DD5} pin power supplies at the same time either before or at the same time as the VH pin power supply is started up.



2. Reset the timing generator block and CCD signal processor block during power-on. The timing generator block is reset by inputting the reset signal to the RST pin. The CCD signal processor block is reset by initializing the serial data.

3. Separate the timing generator block V_{DD1}, V_{DD2}, V_{DD3}, V_{DD4} and V_{DD5} pins from the CCD signal processor block DV_{DD1}, DV_{DD2}, AV_{DD1}, AV_{DD2}, AV_{DD3}, AV_{DD4} and AV_{DD5} pins.
   Also, the ADC output driver stage is connected to the dedicated power supply pin DV_{DD1}. Separating this pin from other power supplies is recommended to avoid affecting the internal analog circuits.

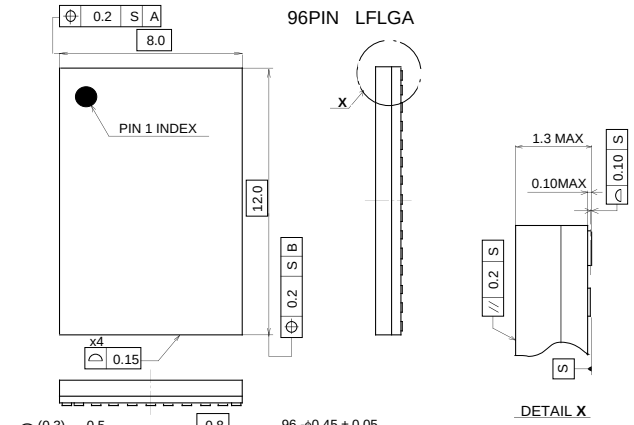
4. The difference in potential between the timing generator block V_{DD4} pin supply voltage 3 V_{DD}c and the CCD signal processor block DV_{DD1}, DV_{DD2}, AV_{DD1}, AV_{DD2}, AV_{DD3}, AV_{DD4} and AV_{DD5} pin supply voltages 1 V_{DD}e, 2 V_{DD}f and 3 V_{DD}g should be 0.1V or less.

5. The timing generator block and CCD signal processor block ground pins should use a shared ground which is connected outside the IC. When the set ground is divided into digital and analog blocks, connect the timing generator block ground pins to the digital ground and the CCD signal processor block ground pins to the analog ground. The difference in potential between the timing generator block V_{SS1}, V_{SS2}, V_{SS3}, V_{SS4}, V_{SS5}, V_{SS6} and VM and the CCD signal processor block DV_{SS1}, DV_{SS2}, DV_{SS3}, AV_{SS1}, AV_{SS2}, AV_{SS3}, AV_{SS4}, AV_{SS5} and AV_{SS6} should be 0.1V or less.

6. Do not perform serial communication with the CCD signal processor block during the effective image period, as this may cause the picture quality to deteriorate. In addition, using SCK2, SSI2 and SEN2, which are used by the CCD signal processor block, use of the dedicated ports is recommended. When using these pins as shared ports with the timing generator block or other ICs, be sure to thoroughly confirm the effects on picture quality before use.

Package Outline Unit: mm

Oita Ass'y

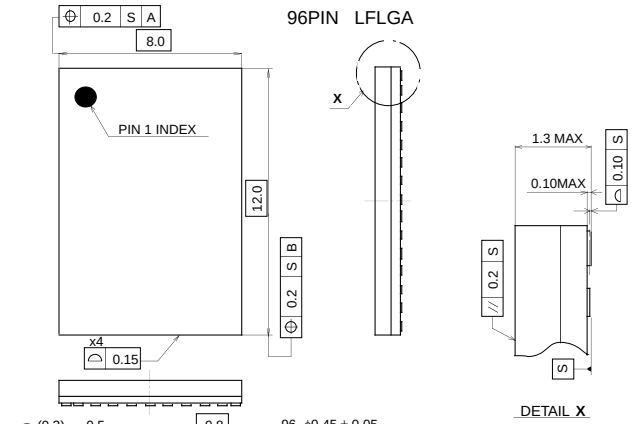


SONY CODE	LFLGA-96P-02
EIAJ CODE	P-LFLGA96-12X8-0.8
JEDEC CODE	

PACKAGE STRUCTURE

PACKAGE MATERIAL	ORGANIC SUBSTRATE
TERMINAL TREATMENT	GOLD PLATING
TERMINAL MATERIAL	NICKEL PLATING
PACKAGE MASS	0.3 g

HITACHI TOKYO Ass'y



SONY CODE	LFLGA-96P-051
EIAJ CODE	P-LFLGA96-12.0X8.0-0.8
JEDEC CODE	

PACKAGE STRUCTURE

PACKAGE MATERIAL	ORGANIC SUBSTRATE
TERMINAL TREATMENT	NICKEL & GOLD PLATING
TERMINAL MATERIAL	COPPER
PACKAGE MASS	0.3g