

SANYO

No.3238

LA5668**Multifunctional Voltage Regulator**

The LA5668 is a multifunctional voltage regulator IC especially suited for use in portable musical instrument applications.

Functions and Features

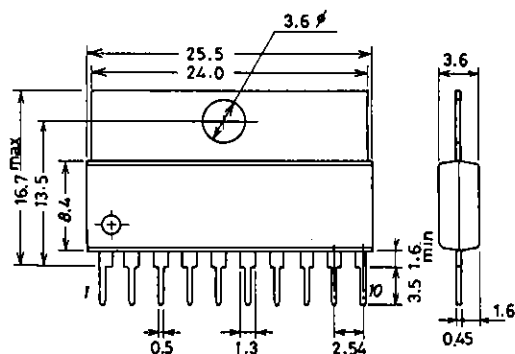
- Power output : 1.0A
- Analog output : 5.5V, 0.1A
- Digital output : 5.0V, 0.1A
- Low I_{CC} at power-OFF mode (APO = OFF) : 35 μ A typ

Maximum Ratings at $T_a = 25^\circ\text{C}$

			unit
Input Voltage	V_{IN} max	18	V
	V_{DIN} max	18	V
Output Current	I_{CO} max	1.0	A
	I_{AO} max	100	mA
	I_{DO} max	100	mA
Allowable Power Dissipation	P_d max	2.45	W
Operating Temperature	T_{opr}	-30 to +85	$^\circ\text{C}$
Storage Temperature	T_{stg}	-40 to +125	$^\circ\text{C}$

Operating Conditions at $T_a = 25^\circ\text{C}$

			unit
Input Voltage	V_{IN}	7.0 to 15	V
	V_{DIN}	7.0 to 15	V
APO Pin ON-State Voltage	$V_{APO ON}$	2 to V_{IN}	V
APO Pin OFF-State Voltage	$V_{APO OFF}$	-0.3 to +0.3	V

Package Dimensions 3046A-S10FIC
(unit: mm)

SANYO: SEP10F

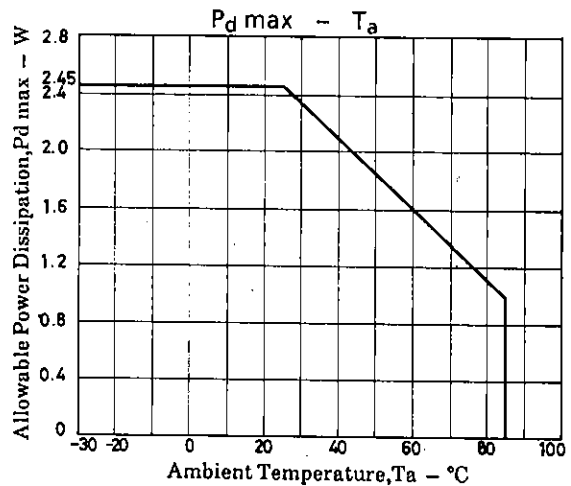
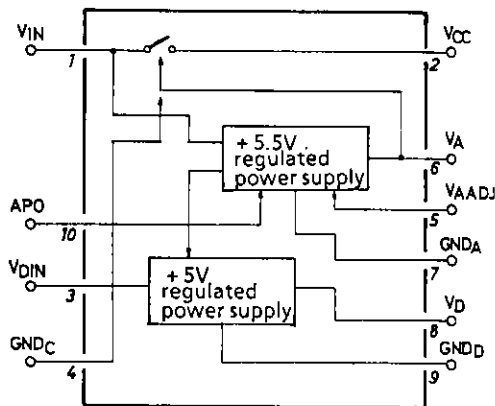
LA5668

Operating Characteristics at $T_a = 25^\circ\text{C}$

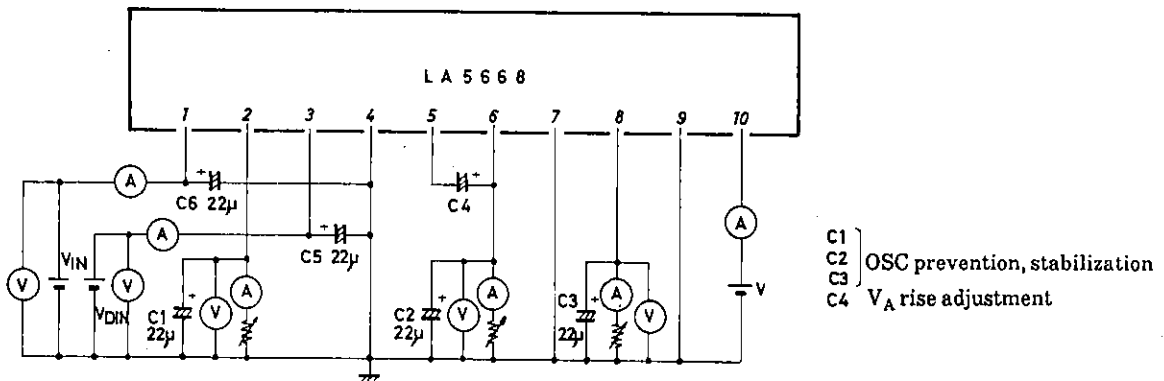
($V_{IN} = V_{DIN} = V_{APO} = 9\text{V}$, $C1 = C2 = C3 = 22\mu\text{F}$ unless otherwise specified)

			min	typ	max	unit
Quiescent Current	I_{CC1}	$V_{APO} = 0\text{V}$		35	50	μA
	I_{CC2}	$V_{APO} = V_{IN}$		8.0	11.0	mA
Output Voltage	V_{AO}	$I_{AO} = 50\text{mA}$	5.05	5.5	5.95	V
	V_{D10}	$V_{APO} = 0\text{V}, I_{DO} = 5\text{mA}$	4.55	5.0	5.45	V
	V_{D20}	$V_{APO} = V_{IN}, I_{DO} = 50\text{mA}$	4.55	5.0	5.45	V
	V_{AO} Line	$7.0 \leq V_{IN} \leq 13\text{V}, I_{AO} = 50\text{mA}$			50	mV
Line Regulation	V_{D10} Line	$7.0 \leq V_{IN} \leq 13\text{V}, V_{APO} = 0\text{V}, I_{DO} = 5\text{mA}$			50	mV
	V_{D20} Line	$7.0 \leq V_{IN} \leq 13\text{V}, V_{APO} = V_{IN}, I_{DO} = 50\text{mA}$			50	mV
	V_{A1} Load	$1 \leq I_{A10} \leq 40\text{mA}$			50	mV
Load Regulation	V_{A2} Load	$1 \leq I_{A20} \leq 80\text{mA}$			100	mV
	V_{D10} Load	$1 \leq I_{D0} \leq 10\text{mA}, V_{APO} = 0\text{V}$			50	mV
	V_{D20} Load	$1 \leq I_{D0} \leq 80\text{mA}, V_{APO} = V_{IN}$			50	mV
	Input-Output Voltage Difference	V_{dA}	$V_{IN} - V_O$ at $V_d: V_O$ 5% OFF, $I_{AO} = 50\text{mA}$	0.9	1.2	
V_{dD}		$V_{IN} - V_O$ at $V_d: V_O$ 5% OFF, $I_{DO} = 50\text{mA}$	0.9	1.2		V
V_{dOC}		$I_{CD} = 500\text{mA}, V_{IN} - V_D$ at $V_{IN} = 9\text{V}$	1.1	1.6		V
Ripple Rejection	R_{rA}	$f = 50\text{Hz}, 120\text{Hz}, I_{AO} = 100\text{mA}$		40		dB
	R_{rD}	$f = 50\text{Hz}, 120\text{Hz}, I_{DO} = 100\text{mA}$		45		dB
APO Input Current	I_{APO}	$V_{APO} = 5\text{V}$	66	86	123	μA
V_C ON-State Voltage	V_C ON	V_A voltage at $V_{APO} = 0\text{V}$	1.5			V
V_C OFF-State Voltage	V_C OFF	V_A voltage at $V_{APO} = 0\text{V}$			0.5	V
$V_A - V_D$ Voltage	$V_A - V_D$	$I_{AO} = 25\text{mA}, I_{DO} = 15\text{mA}$ at $V_{CC} = 5.5\text{V}, 9\text{V}$	-0.3			V

Block Diagram and Pin Assignment

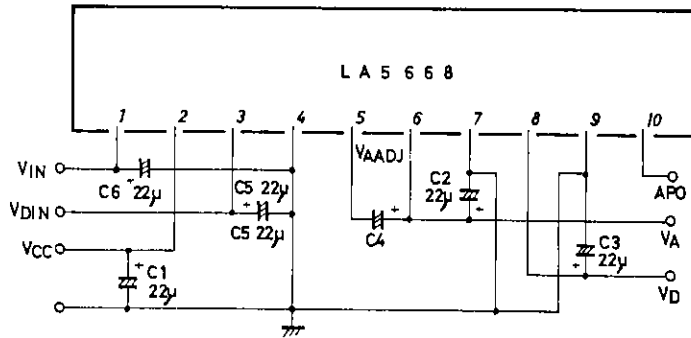


Test Circuit



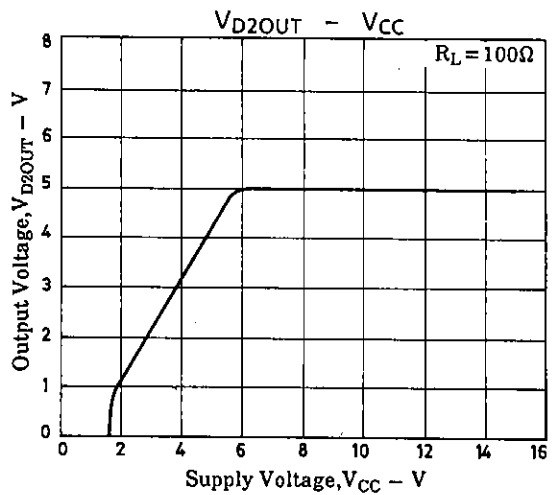
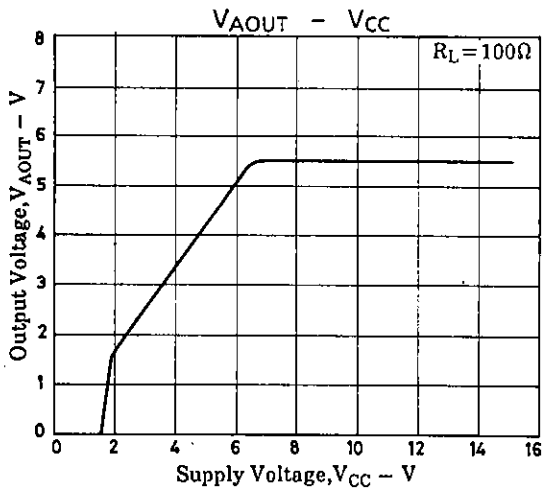
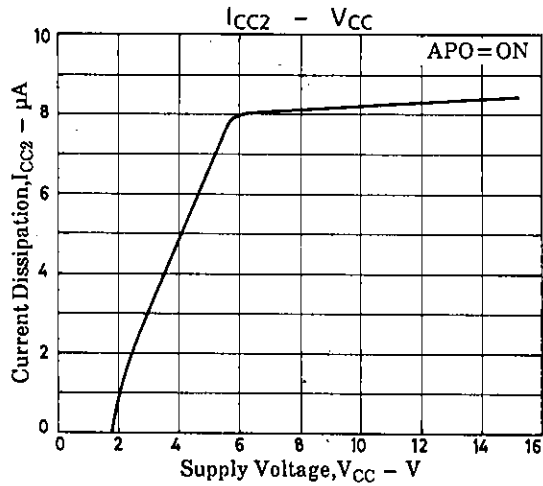
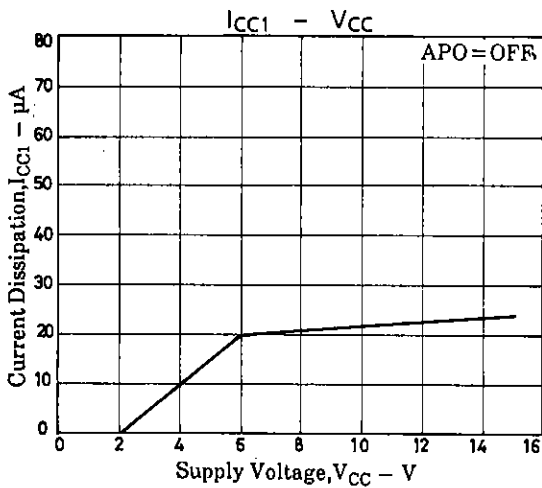
Unit (capacitance: F)

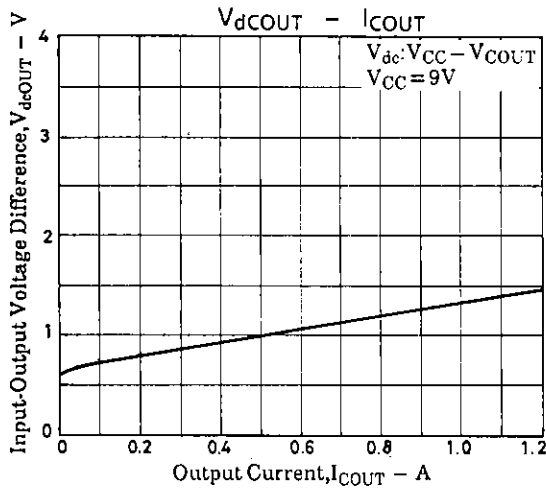
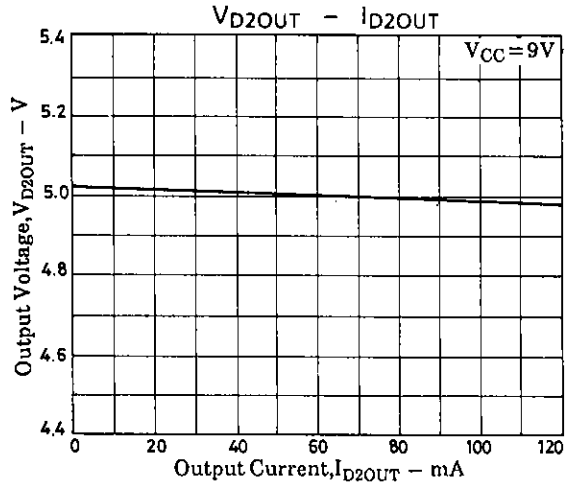
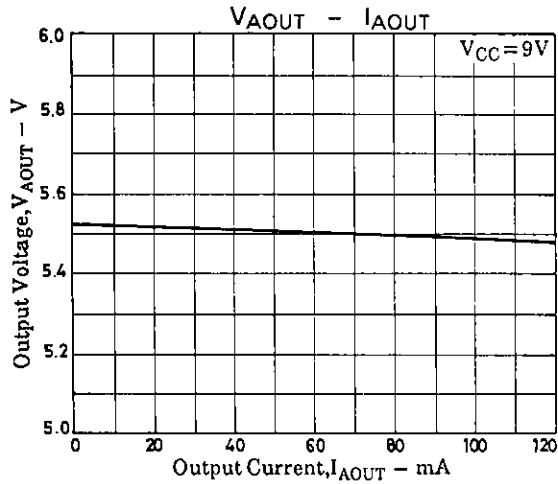
Sample Application Circuit



- C1 } OSC prevention, stabilization
- C2 } OSC prevention, stabilization
- C3 } OSC prevention, stabilization
- C4 } V_A rise adjustment

Unit (capacitance: F)





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