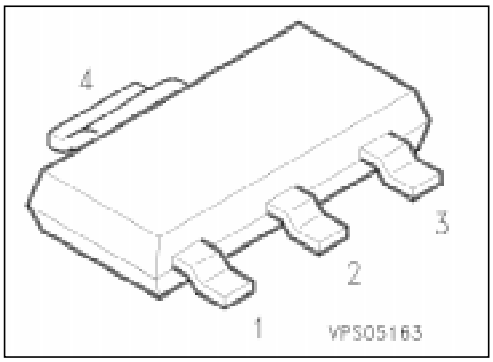
SIEMENS

NPN Silicon Darlington Transistors

BSP 50
… BSP 52

- High collector current
- Low collector-emitter saturation voltage
- Complementary types: BSP 60 … BSP 62 (PNP)



Type	Marking	Ordering Code (tape and reel)	Pin Configuration 1	2	3	4	Package[1]
BSP 50 BSP 51 BSP 52	BSP 50 BSP 51 BSP 52	Q62702-P1163 Q62702-P1164 Q62702-P1165	B	C	E	C	SOT-223

Maximum Ratings

Parameter	Symbol	Values BSP 50	BSP 51	BSP 52	Unit
Collector-emitter voltage	V_{CER}	45	60	80	V
Collector-base voltage	V_{CB0}	60	80	100	
Emitter-base voltage	V_{EB0}	5			
Collector current	I_C	1			A
Peak collector current	I_{CM}	2			
Base current	I_B	0.1			
Total power dissipation, T_S = 124 ˚C	P_{tot}	1.5			W
Junction temperature	T_j	150			˚C
Storage temperature range	T_{stg}	– 65 … + 150			

Thermal Resistance

Junction - ambient[2]	$R_{th\ JA}$	≤ 72	K/W
Junction - soldering point	$R_{th\ JS}$	≤ 17	

1) For detailed information see chapter Package Outlines.
2) Package mounted on epoxy pcb 40 mm × 40 mm × 1.5 mm/6 cm² Cu.

Electrical Characteristics

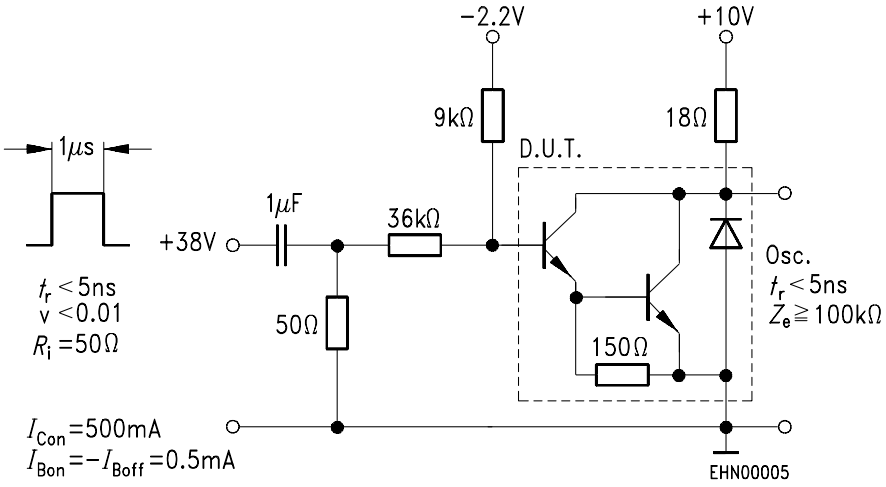
at T_A = 25 °C, unless otherwise specified.

Parameter	Symbol	Values			Unit
		min.	typ.	max.	
DC characteristics					
Collector-emitter breakdown voltage[1]	$V_{(BR)CER}$				V
I_C = 10 mA BSP 50		45	–	–	
BSP 51		60	–	–	
BSP 52		80	–	–	
Collector-base breakdown voltage	$V_{(BR)CB0}$				
I_C = 100 µA, I_B = 0 BSP 50		60	–	–	
BSP 51		80	–	–	
BSP 52		100	–	–	
Emitter-base breakdown voltage I_E = 100 µA, I_B = 0	$V_{(BR)EB0}$	5	–	–	
Collector-emitter cutoff current V_{CE} = V_{CERmax}, V_{BE} = 0	I_{CES}	–	–	10	µA
Emitter-base cutoff current V_{EB} = 4 V, I_C = 0	I_{EB0}	–	–	10	
DC current gain[2] I_C = 150 mA, V_{CE} = 10 V	h_{FE}	1000	–	–	–
I_C = 500 mA, V_{CE} = 10 V		2000	–	–	
Collector-emitter saturation voltage[2]	V_{CEsat}				V
I_C = 500 mA, I_B = 0.5 mA		–	–	1.3	
I_C = 1 A, I_B = 1 mA		–	–	1.8	
Base-emitter saturation voltage[2] I_C = 500 mA, I_B = 0.5 mA	V_{BEsat}	–	–	1.9	
I_C = 1 A, I_B = 1 mA		–	–	2.2	
AC characteristics					
Transition frequency I_C = 100 mA, V_{CE} = 5 V, f = 100 MHz	f_T	–	200	–	MHz
Switching times I_C = 500 mA, I_{B1} = I_{B2} = 0.5 mA	t_{on}	–	400	–	ns
(see diagrams)	t_{off}	–	1500	–	ns

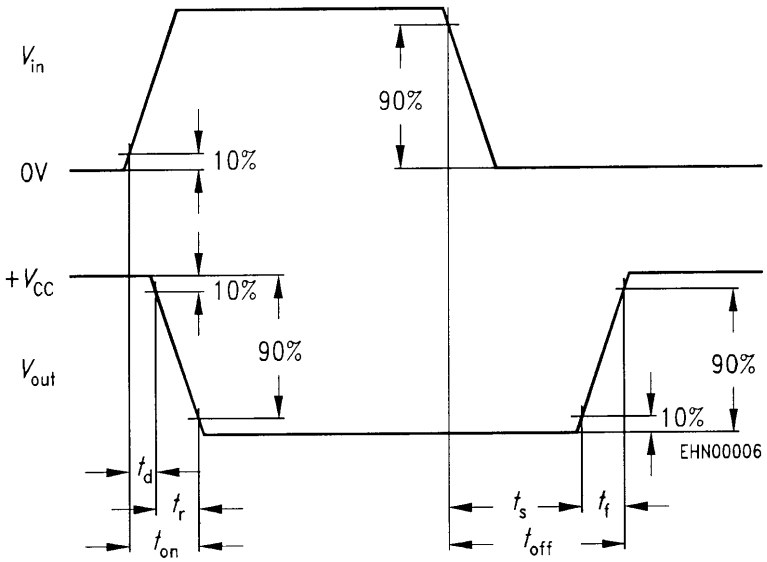
1) Compare R_{BE} for thermal stability.

2) Pulse test conditions: $t \leq 300$ µs, D = 2 %.

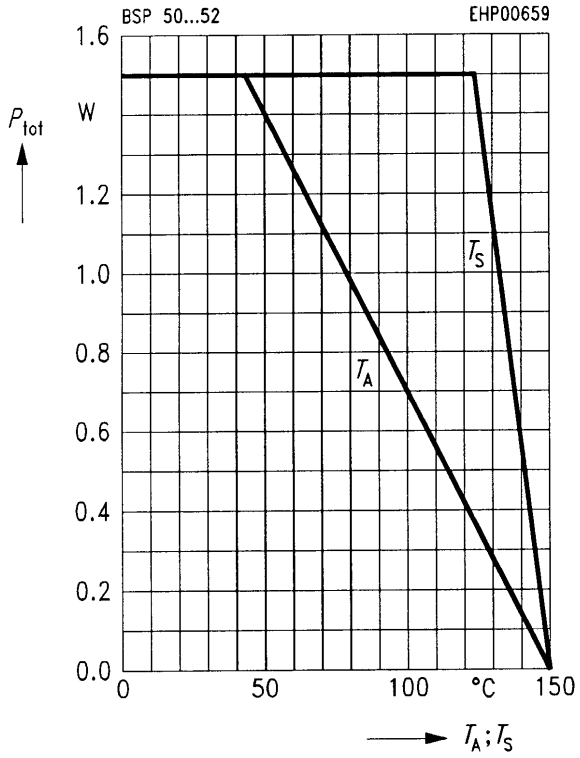
Switching time test circuit



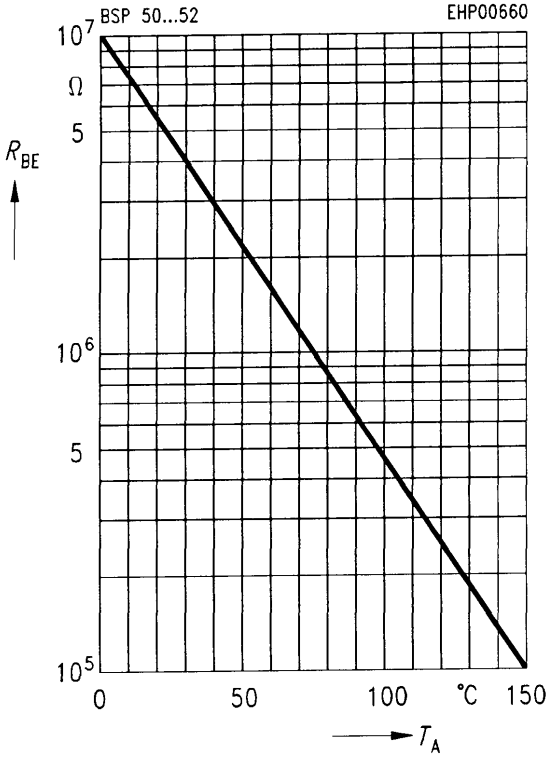
Switching time waveform



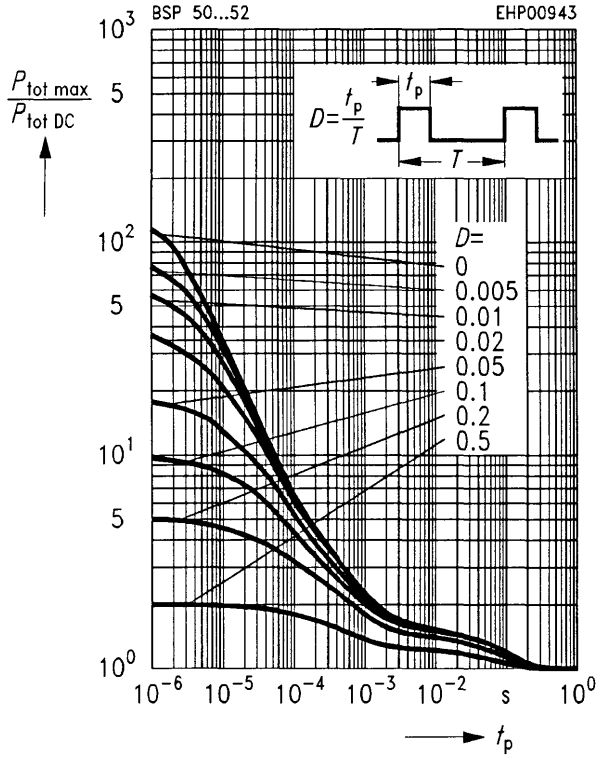
Total power dissipation $P_{tot} = f(T_A^*; T_S)$
* Package mounted on epoxy



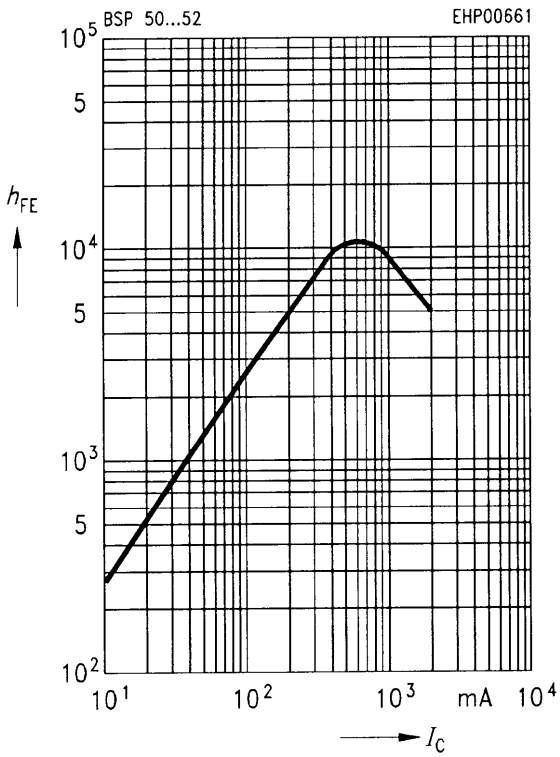
External resistance $R_{BE} = f(T_A)$**
$V_{CB} = V_{CE\ max}$
** $R_{BE\ max}$ for thermal stability



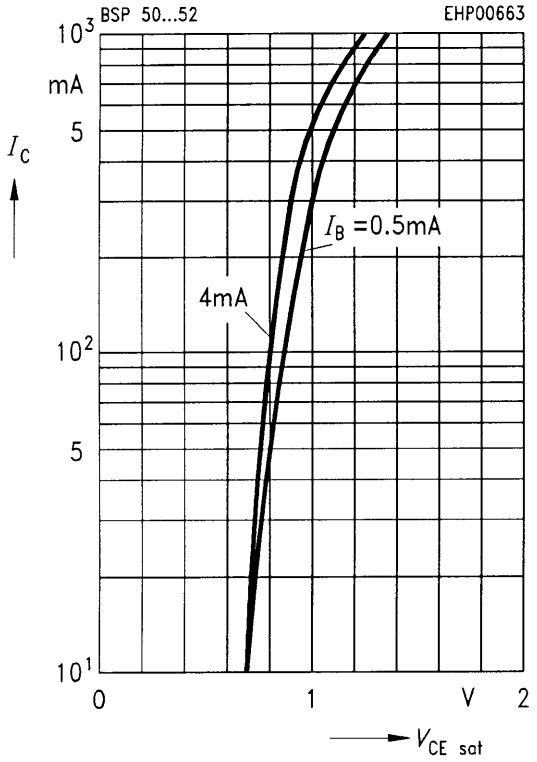
Permissible pulse load $P_{tot\ max} / P_{tot\ DC} = f(t_p)$



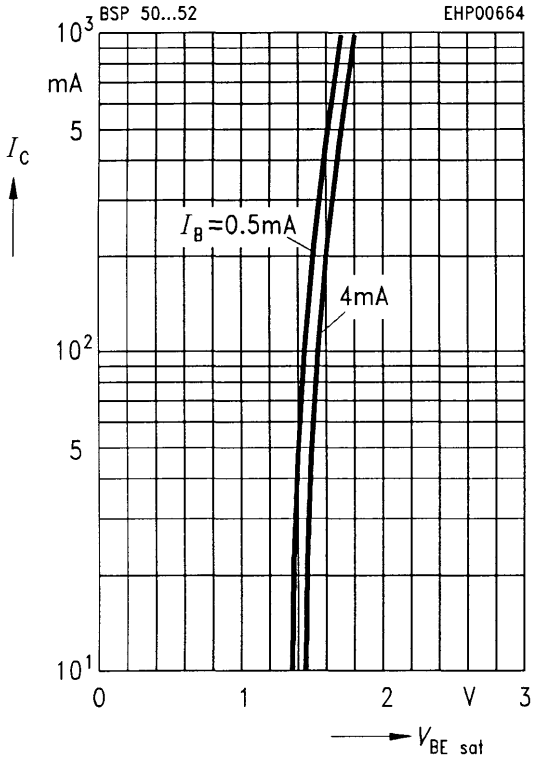
DC current gain $h_{FE} = f(I_C)$
V_{CE} = 10 V



Collector-emitter saturation voltage
$I_C = f(V_{CE\,sat})$, I_B-parameter



Base-emitter saturation voltage
$I_C = f(V_{BE\,sat})$, I_B-parameter



Transition frequency $f_T = f(I_C)$
V_{CE} = 5 V, f = 100 MHz