NEC

BIPOLAR ANALOG INTEGRATED CIRCUITS

μPC8106TB, μPC8109TB

SILICON MMIC 2.0 GHz FREQUENCY UP-CONVERTER FOR CELLULAR/CORDLESS TELEPHONES

DESCRIPTION

The μPC8106TB and μPC8109TB are silicon monolithic integrated circuit designed as frequency up-converter for cellular/cordless telephone transmitter stage. The μPC8106TB features improved intermodulation and μPC8109TB features low current consumption. From these two version, you can chose either IC corresponding to your system design. These TB suffix ICs which are smaller package than conventional T suffix ICs contribute to reduce your system size.

The μPC8106TB and μPC8109TB are manufactured using NEC's 20 GHz f_T NESAT™III silicon bipolar process. This process uses a silicon nitride passivation film and gold electrodes. These materials can protect chip surface from external pollution and prevent corrosion/migration. Thus, this IC has excellent performance, uniformity and reliability.

FEATURES

- Recommended operating frequency : f_{RFout} = 0.4 GHz to 2.0 GHz, f_{IFin} = 100 MHz to 400 MHz
- Supply voltage : V_{CC} = 2.7 to 5.5 V
- High-density surface mounting : 6-pin super minimold package
- Low current consumption : I_{CC} = 9 mA TYP. @ μPC8106TB
  I_{CC} = 5 mA TYP. @ μPC8109TB
- Minimized carrier leakage : Due to double balanced mixer
- Built-in power save function

APPLICATION

- Cellular/cordless telephone up to 2.0 GHz MAX (example: PHS, PDC, DCS1800 and so on)

ORDERING INFORMATION

Part Number	Markings	Product Type	Package	Supplying Form
μPC8106TB-E3	C2D	High IP_3	6-pin super minimold	Embossed tape 8 mm wide. Pin 1, 2, 3 face to tape perforation side. QTY 3 kp/Reel.
μPC8109TB-E3	C2G	Low current consumption		

Remark To order evaluation samples, please contact your local NEC sales office.
(Part number for sample order: μPC8106TB, μPC8109TB)

Caution Electro-static sensitive devices

The information in this document is subject to change without notice. Before using this document, please confirm that this is the latest version.
Not all devices/types available in every country. Please check with local NEC representative for availability and additional information.

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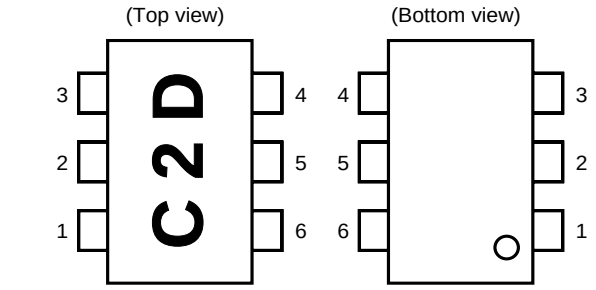
PIN CONNECTIONS



Marking is an example of μPC8106TB.

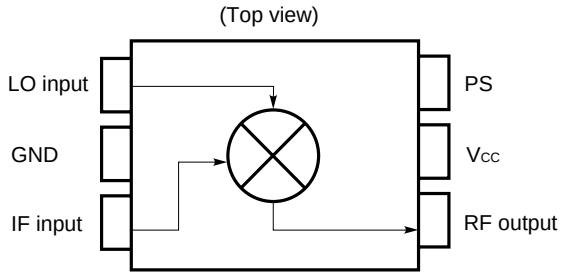
Pin No.	Pin Name
1	IFinput
2	GND
3	LOinput
4	PS
5	V_{CC}
6	RFoutput

★ SERIES PRODUCTS (T_A = +25 °C, V_{CC} = V_{PS} = V_{RFout} = 3.0 V, Z_L = Z_S = 50 Ω)

TYPE	PRODUCT NAME	V_{CC} (V)	I_{CC} (mA)	CG1 (dB)	CG2 (dB)	$P_{O(sat)}1$ (dBm)	$P_{O(sat)}2$ (dBm)	$OIP_3$1 (dBm)	$OIP_3$2 (dBm)
High IP_3	μPC8106TB	2.7 to 5.5	9	9	7	–2	–4	+5.5	+2.0
Low power consumption	μPC8109TB	2.7 to 5.5	5	6	4	–5.5	–7.5	+1.5	–1.0
Higher IP_3	μ PC8163TB	2.7 to 3.3	16.5	9	5.5	0.5	–2	+9.5	+6

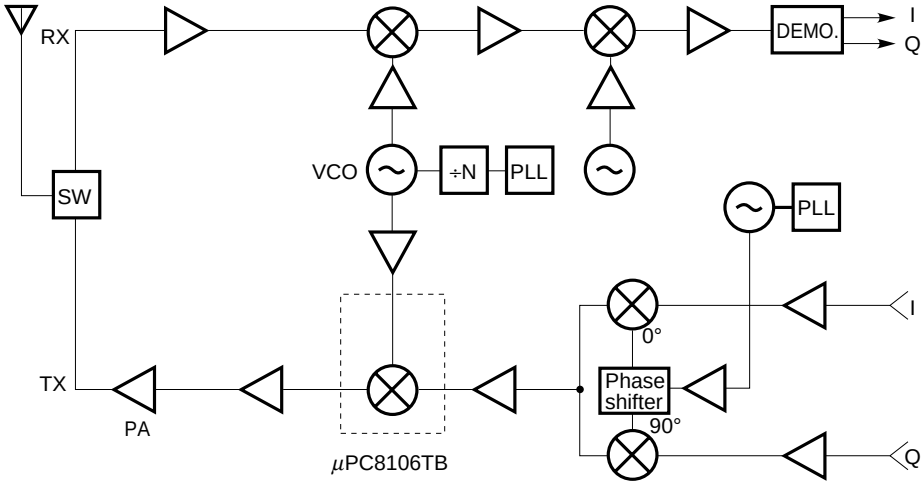
Caution The above table lists the typical performance of each model. See ELECTRICAL CHARACTERISTICS for the test conditions.

BLOCK DIAGRAM (FOR THE μPC8106TB AND μPC8109TB)

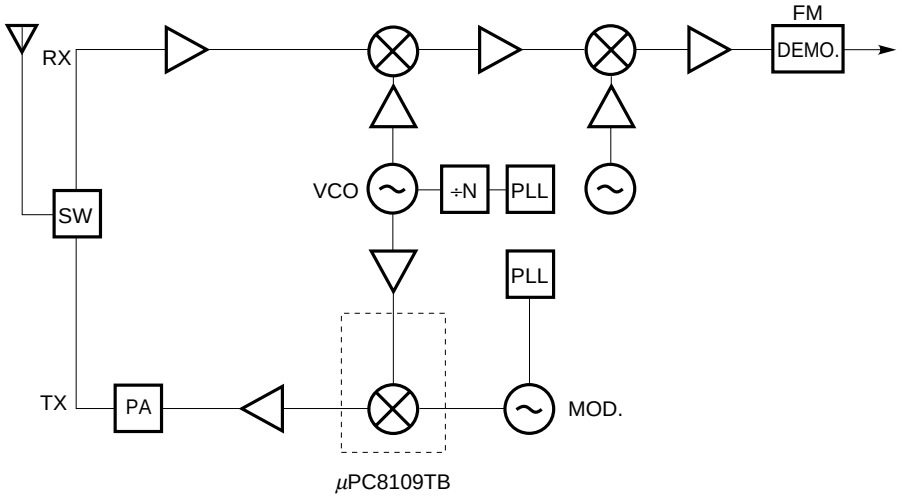


SYSTEM APPLICATION EXAMPLES (SCHEMATICS OF IC LOCATION IN THE SYSTEMS)

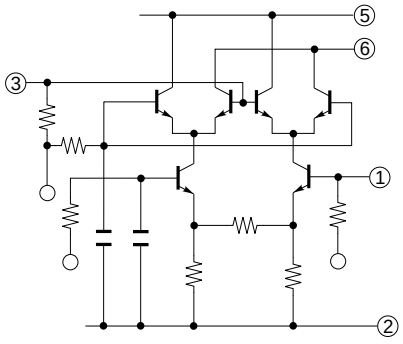
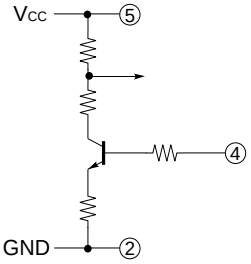
PHS, DECT



Analog cellular telephone



PIN FUNCTIONS (FOR THE μPC8106TB AND μPC8109TB)

Pin No.	Pin Name	Applied Voltage (V)	Pin Voltage (V)[Note]	Function and Explanation	Equivalent Circuit
1	IFinput	–	1.3	This pin is IF input to double balanced mixer (DBM). The input is designed as high impedance. The circuit contributes to suppress spurious signal. Also this symmetrical circuit can keep specified performance insensitive to process-condition distribution. For above reason, double balanced mixer is adopted.	
2	GND	0	–	GND pin. Ground pattern on the board should be formed as wide as possible. Track Length should be kept as short as possible to minimize ground impedance.	
3	LOinput	–	2.4	Local input pin. Recommendable input level is –10 to 0 dBm.	
5	V_{CC}	2.7 to 5.5	–	Supply voltage pin.	
6	RFoutput	Same bias as V_{CC} through external inductor	–	This pin is RF output from DBM. This pin is designed as open collector. Due to the high impedance output, this pin should be externally equipped with LC matching circuit to next stage.	
4	PS	V_{CC}/GND	–	Power save control pin. Bias controls operation as follows. Pin bias / Control V_{CC} / Operation GND / Power Save	

Note Each pin voltage is measured with $V_{CC} = V_{PS} = V_{RFout} = 3.0$ V.

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Test Conditions	Rating	Unit
Supply Votage	V_{CC}	T_A = +25 °C, Pin 5 and 6	6.0	V
PS pin Input Voltage	V_{PS}	T_A = +25 °C	6.0	V
Power Dissipation of Package	P_D	Mounted on double-sided copper-clad 50 × 50 × 1.6 mm epoxy glass PWB T_A = +85 °C	200	mW
Operating Ambient Temperature	T_A		–40 to +85	°C
Storage Temperature	T_{stg}		–55 to +150	°C
Maximum Input Power	P_{in}		+10	dBm

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	MIN.	TYP.	MAX.	Unit	Note
Supply Voltage	V_{CC}	2.7	3.0	5.5	V	The same voltage should be supplied to pin 5 and 6
Operating Ambient Temperature	T_A	–40	+25	+85	°C	
Local Input Level	P_{LOin}	–10	–5	0	dBm	Z_S = 50 Ω (without matching)
RF Output Frequency	f_{RFout}	0.4	–	2.0	GHz	With external matching circuit
IF Input Frequency	f_{IFin}	100	–	400	MHz	

ELECTRICAL CHARACTERISTICS

(T_A = +25 °C, V_{CC} = V_{RFout} = 3.0 V, f_{IFin} = 240 MHz, P_{LOin} = –5 dBm, and V_{PS} ≥ 2.7 V unless otherwise specified)

Parameter	Symbol	Conditions	μPC8106TB			μPC8109TB			Unit
			MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Circuit Current	I_{CC}	No signal	4.5	9	13.5	2.5	5	8.0	mA
Circuit Current in Power-save Mode	I_{CC}(PS)	V_{PS} = 0 V	–	–	10	–	–	10	μA
Conversion Gain 1	CG1	f_{RFout} = 0.9 GHz, P_{IFin} = –30 dBm	6	9	12	3	6	9	dB
Conversion Gain 2	CG2	f_{RFout} = 1.9 GHz, P_{IFin} = –30 dBm	4	7	10	1	4	7	dB
Maximum RF Output Power 1	$P_{O(sat)}$1	f_{RFout} = 0.9 GHz, P_{IFin} = 0 dBm	–4	–2	–	–7.5	–5.5	–	dBm
Maximum RF Output Power 2	$P_{O(sat)}$2	f_{RFout} = 1.9 GHz, P_{IFin} = 0 dBm	–6.5	–4	–	–10	–7.5	–	dBm

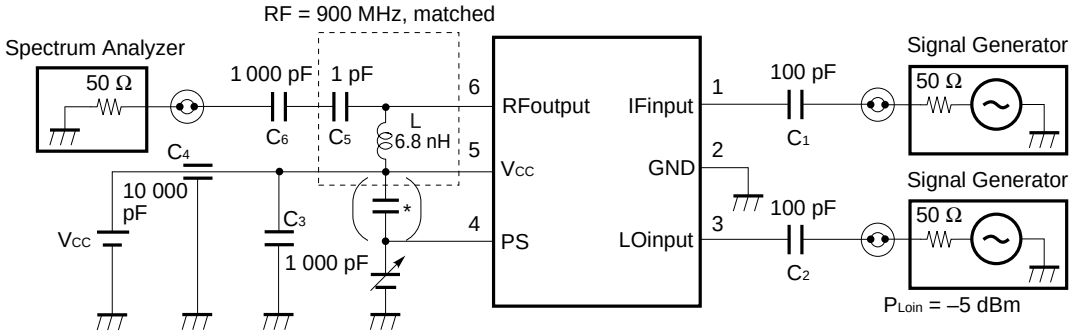
OTHER CHARACTERISTICS, FOR REFERENCE PURPOSES ONLY
(T_A = +25 °C, V_{CC} = V_{RFout} = 3.0 V, P_{LOin} = –5 dBm, and V_{PS} ≥ 2.7 V unless otherwise mentioned)

Parameter		Symbol	Conditions		Reference Value		Unit
					μPC8106TB	μPC8109TB	
Output Third-Order Distortion Intercept Point		$OIP_3$1	f_{IFin1} = 240.0 MHz	f_{RFout} = 0.9 GHz	+5.5	+1.5	dBm
		$OIP_3$2	f_{IFin2} = 240.4 MHz	f_{RFout} = 1.9 GHz	+2.0	–1.0	
Third-Order Intermodulation Distortion 1		$IM_3$1	f_{IFint} = 240.0 MHz f_{IFin2} = 240.4 MHz P_{IFin} = –20 dBm	f_{RFout} = 0.9 GHz	–31	–29	dBc
Third-Order Intermodulation Distortion 2		$IM_3$2		f_{RFout} = 1.9 GHz	–30	–28	dBc
SSB Noise Figure		SSBNF	f_{RFout} = 0.9 GHz, f_{IFin} = 240 MHz		8.5	8.5	dB
Power Save Response Time	Rise time	$T_{PS(rise)}$	V_{PS}: GND → V_{CC}		2.0	2.0	μs
	Fall time	$T_{PS(fall)}$	V_{PS}: V_{CC} → GND		2.0	2.0	μs

APPLICATION CIRCUIT EXAMPLE CHARACTERSISTICS FOR REFERENCE PURPOSE ONLY
(T_A = +25 °C, V_{CC} = V_{PS} = V_{RFout} = 3.0 V, f_{IFin} = 130 MHz, f_{LOin} = 1630 MHz, P_{LOin} = –5 dBm)

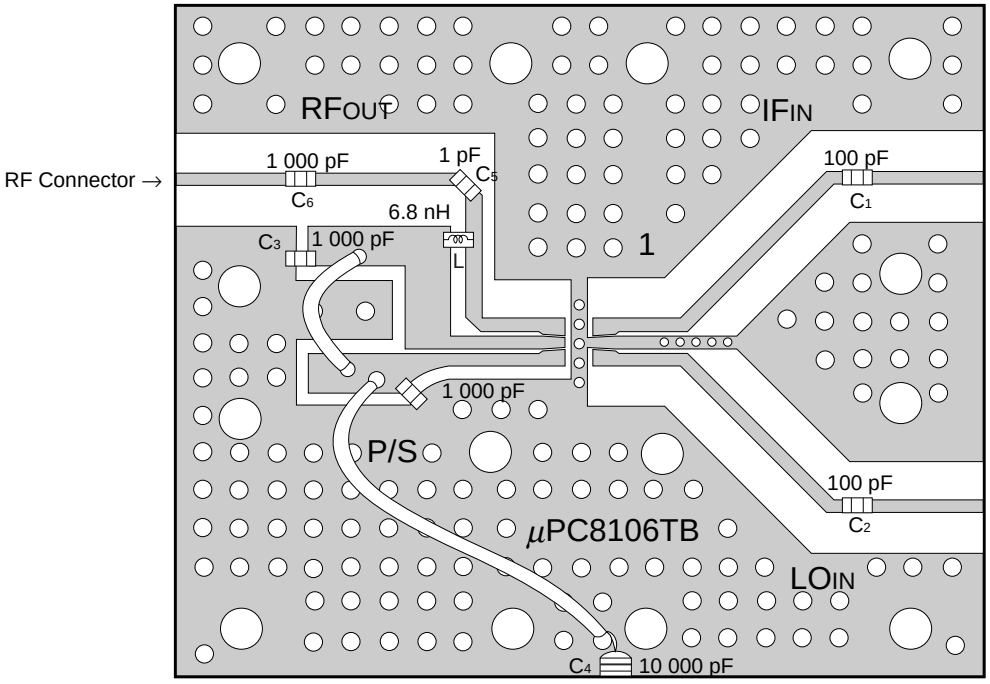
Parameter	Symbol	Conditions	Reference Value	Unit
			μPC8106TB	
Conversion Gain	CG	f_{RFout} = 1.5 GHz, with application circuit example	7	dB
Maximum RF Output Power	$P_{O(sat)}$	f_{RFout} = 1.5 GHz, with application circuit example	–3.5	dBm

★ **TEST CIRCUIT 1 (RF = 900 MHz, for the μPC8106TB and μPC8109TB)**



* In case of unstable operation, please connect capacitor 100 pF between 4 pin and 5 pin and adjust the matching circuit.

EXAMPLE OF TEST CIRCUIT 1 ASSEMBLED ON EVALUATION BOARD



COMPONENT LIST

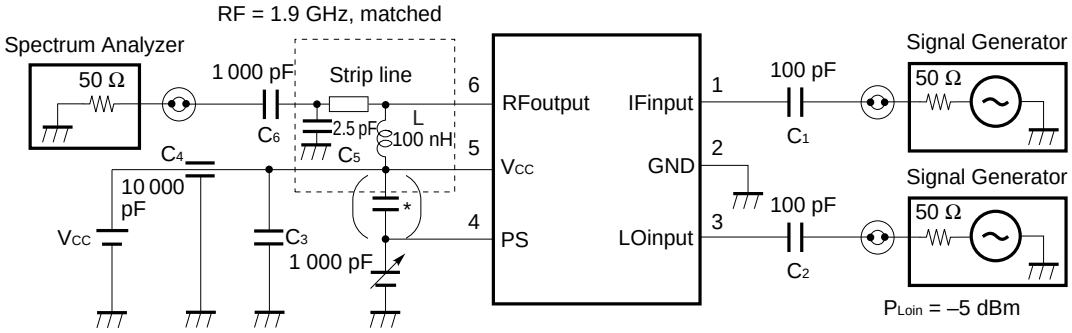
Form	Symbol	Value
Chip capacitor	C_1, C_2	100 pF
	C_3, C_6	1 000 pF
	C_5	1 pF
Through capacitor	C_4	10 000 pF
Chip inductor	L	6.8 nH[Note]

Note 6.8 nH: Murata Mfg. Co., Ltd. LQP31A6N8J04

Notes on the board

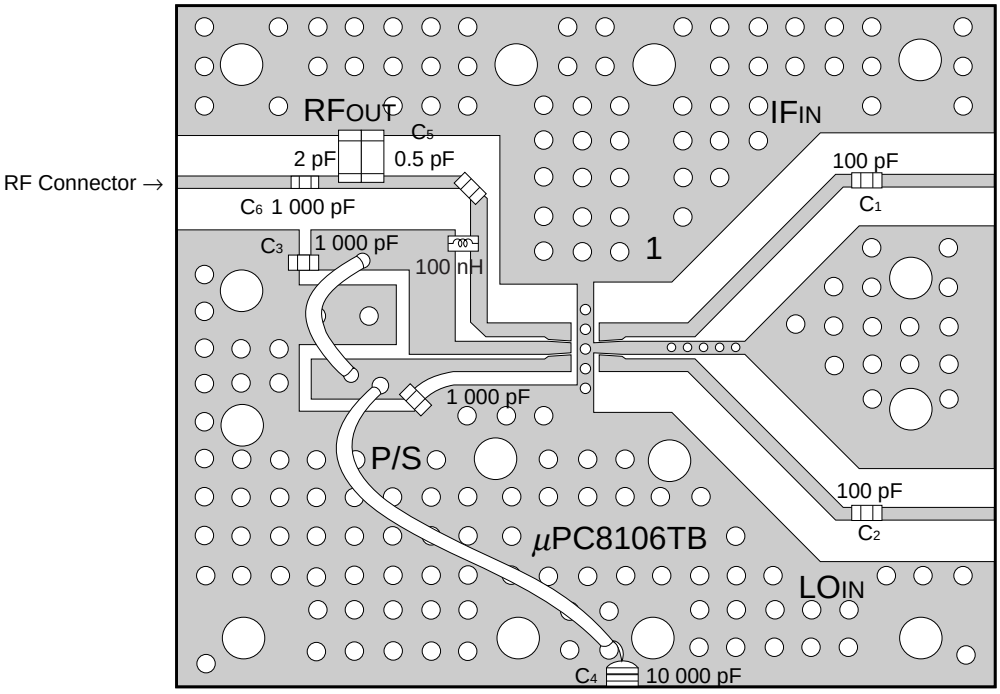
1. 35 × 42 × 0.4 mm polyimide board, 35 μm double-sided copper clad
2. Ground pattern on rear of the board
3. Solder plated patterns
4. ○◯◯: Through holes
5. C_6 is for RF short on the board pattern

★ **TEST CIRCUIT 2 (RF = 1.9 GHz, for the μPC8106TB and μPC8109TB)**



* In case of unstable operation, please connect capacitor 100 pF between 4 pin and 5 pin and adjust the matching circuit.

EXAMPLE OF TEST CIRCUIT 2 ASSEMBLED ON EVALUATION BOARD



COMPONENT LIST

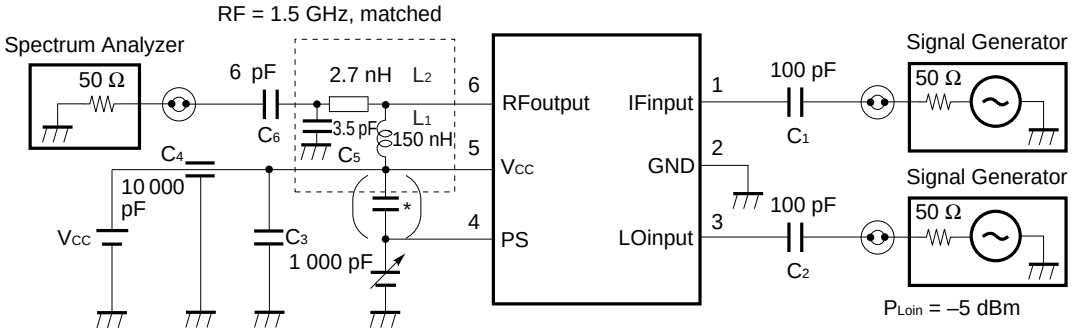
Form	Symbol	Value
Chip capacitor	C_1, C_2	100 pF
	C_3, C_6	1 000 pF
	C_5	2.5 pF (2.0 pF, 0.5 pF parallel)
Through capacitor	C_4	10 000 pF
Chip inductor	L	100 nH[Note]

Note 100 nH: Murata Mfg. Co., Ltd. LQN1AR10J(K)04

Notes on the board

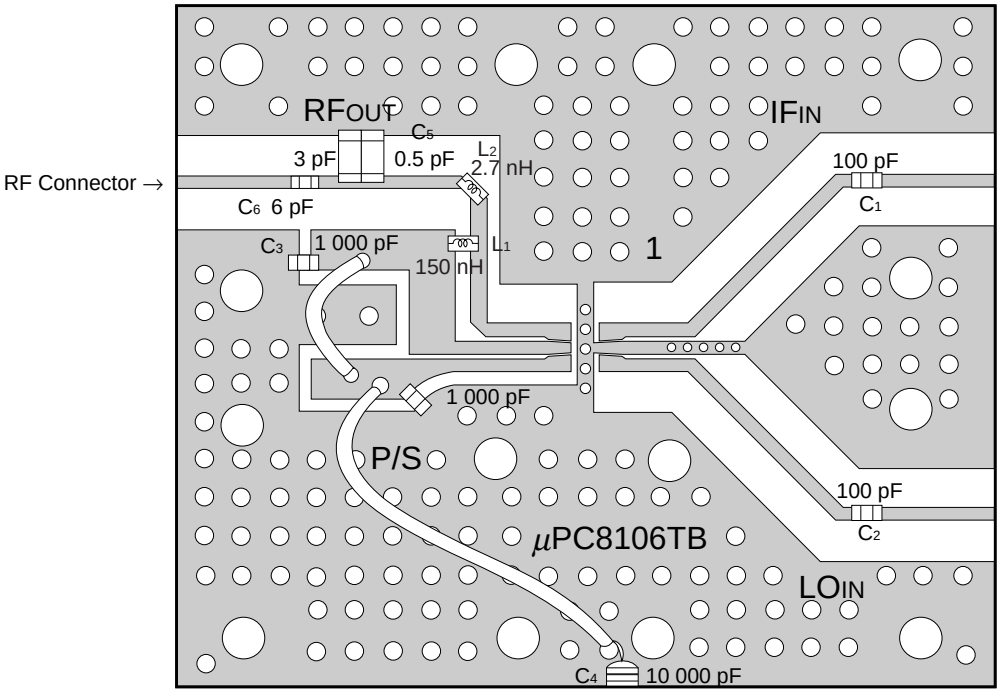
1. 35 × 42 × 0.4 mm polyimide board, 35 μm double-sided copper clad
2. Ground pattern on rear of the board
3. Solder plated patterns
4. ○◯◯: Through holes

★ **APPLICATION CIRCUIT EXAMPLE (RF = 1.5 GHz, for the μPC8106TB and μPC8109TB)**



* In case of unstable operation, please connect capacitor 100 pF between 4 pin and 5 pin and adjust the matching circuit.

EXAMPLE OF APPLICATION CIRCUIT ASSEMBLED ON EVALUATION BOARD



COMPONENT LIST

Form	Symbol	Value
Chip capacitor	C_1, C_2	100 pF
	C_3	1 000 pF
	C_5	3.5 pF (3.0 pF, 0.5 pF parallel)
	C_6	6 pF
Through capacitor	C_4	10 000 pF
Chip inductor	L_1	150 nH[Note 1]
	L_2	2.7 nH[Note 2]

Notes 1. 150 nH: TOKO Co., Ltd. LL2012-FR15

2. 2.7 nH : TOKO Co., Ltd. LL2012-F2N7S

Notes on the board

1. 35 × 42 × 0.4 mm polyimide board, 35 μm double-sided copper clad

2. Ground pattern on rear of the board

3. Solder plated patterns

4. ○○◯: Through holes

NOTICE

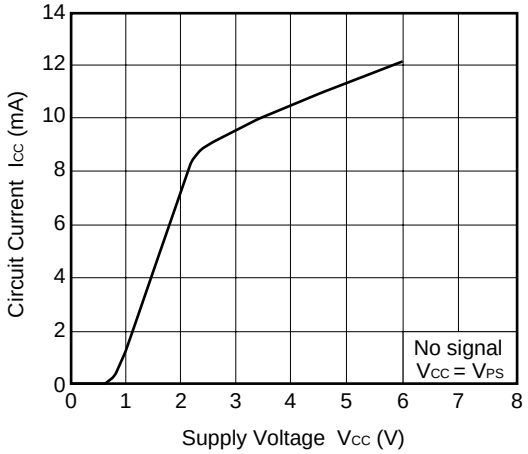
The test circuits and board pattern on data sheet are for performance evaluation use only. (They are not recommended circuits.) In the case of actual design-in, matching circuit should be determined using S parameter of desired frequency in accordance to actual mounting pattern.

For external circuits of the ICs, following Application Note is also available.

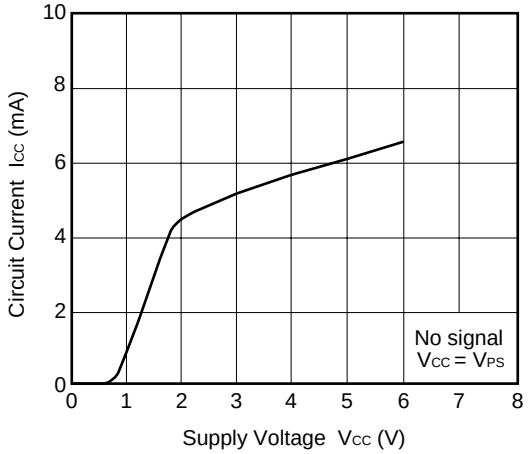
- μPC8106, μPC8109 Application Note (Document No. P13683E)

★ **TYPICAL CHARACTERISTICS (T_A = +25°C, V_{CC} = V_{RFout}) with TEST CIRCUIT 1 or 2, according to the operating frequency, unless otherwise specified**

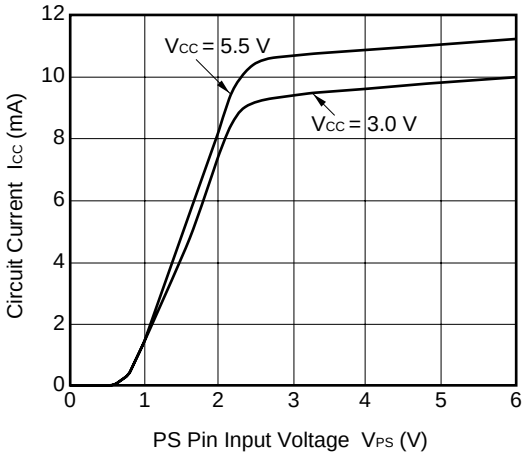
CIRCUIT CURRENT vs. SUPPLY VOLTAGE (μPC8106TB)



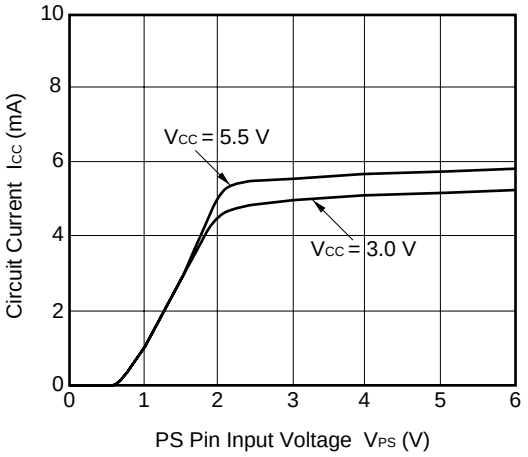
CIRCUIT CURRENT vs. SUPPLY VOLTAGE (μPC8109TB)



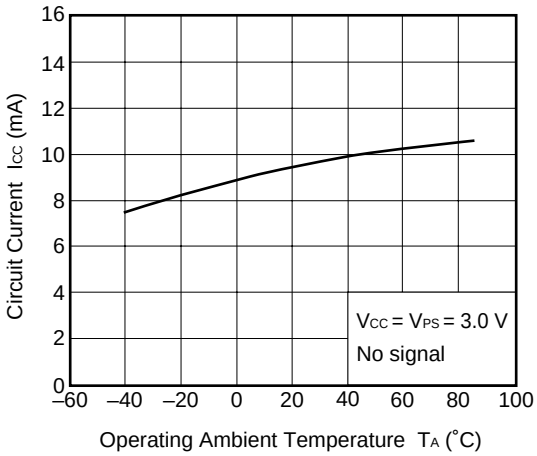
CIRCUIT CURRENT vs. PS PIN INPUT VOLTAGE (μPC8106TB)



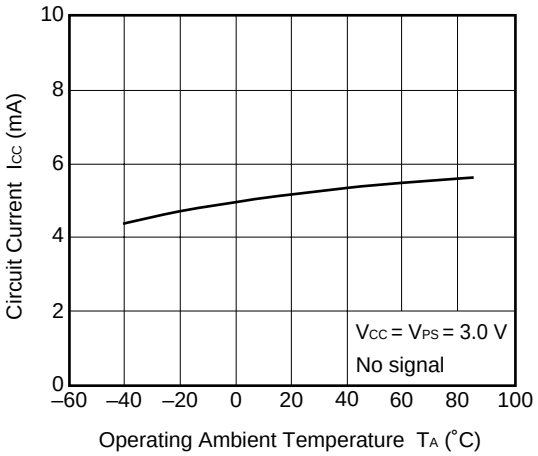
CIRCUIT CURRENT vs. PS PIN INPUT VOLTAGE (μPC8109TB)



CIRCUIT CURRENT vs. OPERATING AMBIENT TEMPERATURE (μPC8106TB)

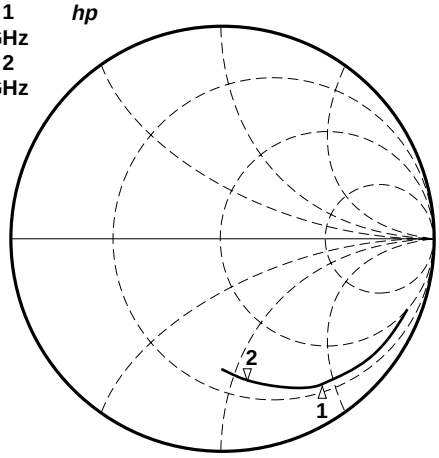


CIRCUIT CURRENT vs. OPERATING AMBIENT TEMPERATURE (μPC8109TB)



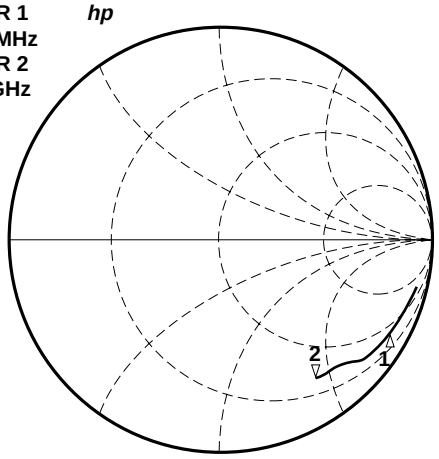
S-PARAMETERS FOR EACH PORT (V_{CC} = V_{PS} = V_{RFout} = 3.0 V) – μPC8106TB, μPC8109TB in common – (THE parameters are monitored at DUT pins.)

LO port S_{11} Z
REF 1.0 Units
2 200.0 mUnits/
▽ 21.201 Ω –53.748 Ω
MARKER 1 *hp*
1.15 GHz
MARKER 2
1.65 GHz



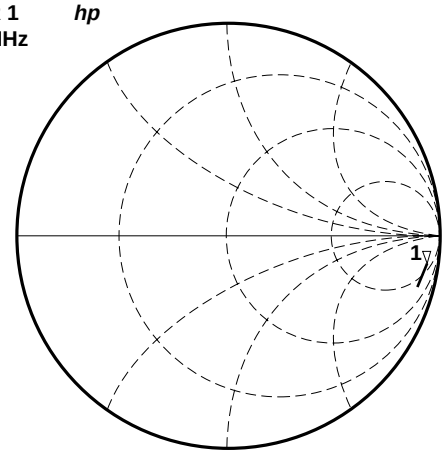
START 0.4 GHz STOP 1.9 GHz

RF port S_{22} Z
REF 1.0 Units
2 200.0 mUnits/
▽ 26.961 Ω –87.312 Ω
MARKER 1 *hp*
900 MHz
MARKER 2
1.9 GHz



START 0.4 GHz STOP 1.9 GHz

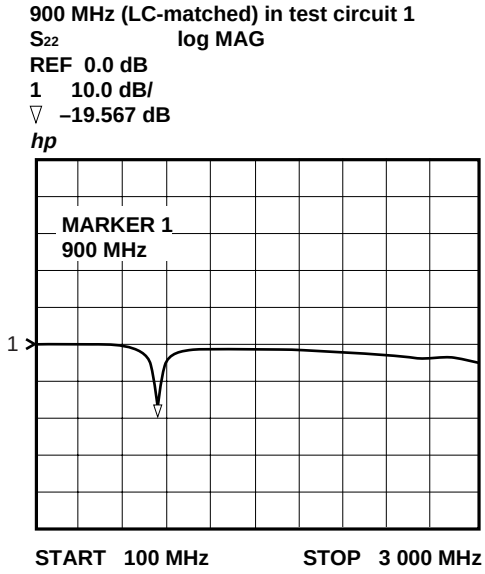
IF port S_{11} Z
REF 1.0 Units
1 200.0 mUnits/
▽ 194.16 Ω –579.53 Ω
MARKER 1 *hp*
240 MHz



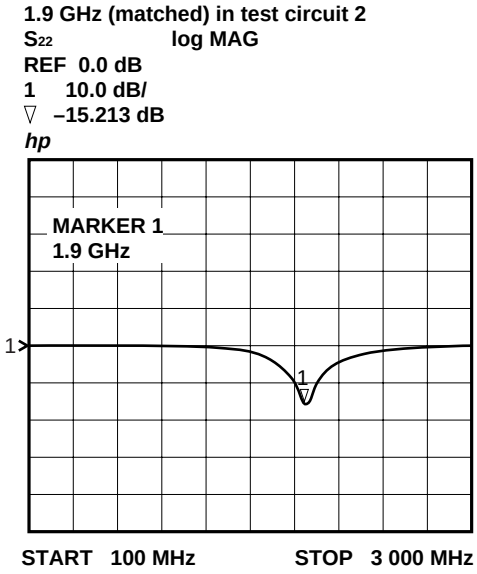
START 0.1 GHz STOP 0.4 GHz

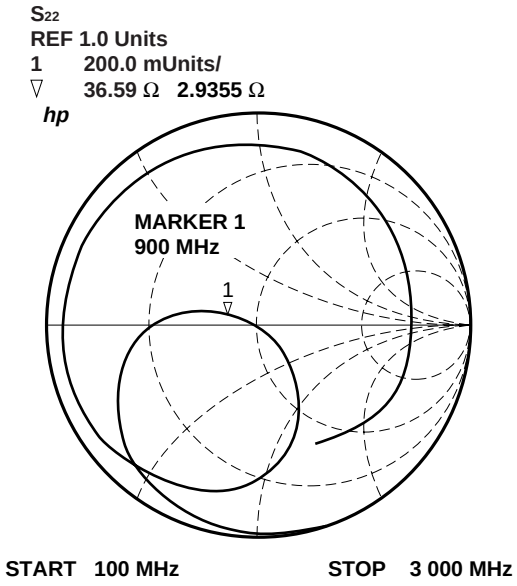
S-PARAMETERS FOR MATCHED RF OUTPUT (V_{CC} = V_{PS} = V_{RFout} = 3.0 V) – with TEST CIRCUITS 1 and 2 (μPC8106TB, μPC8109TB in common) – (S_{22} data are monitored at RF connector on board.)

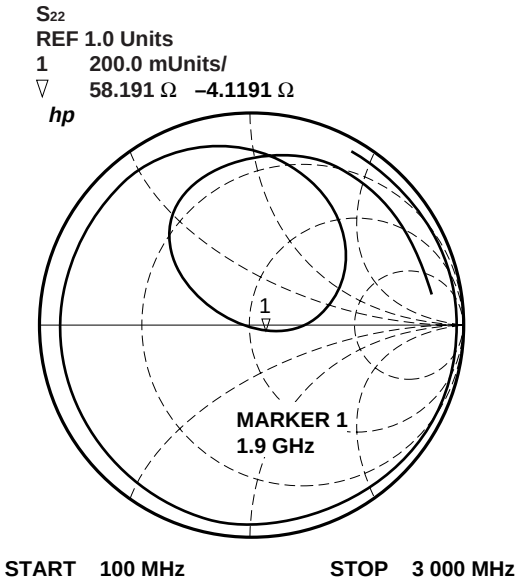
900 MHz (LC-matched) in test circuit 1



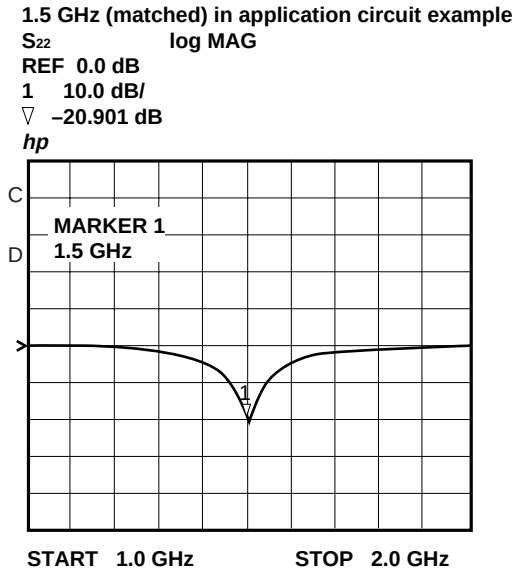
1.9 GHz (matched) in test circuit 2

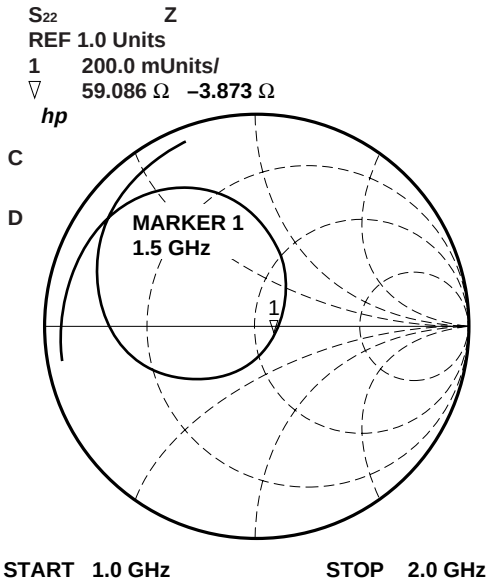




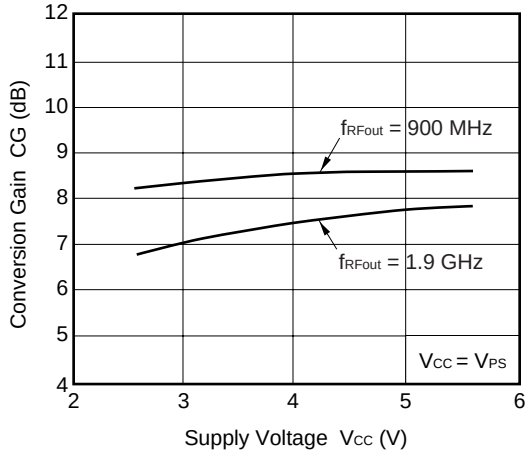


S-PARAMETERS FOR MATCHED RF OUTPUT (V_{CC} = V_{PS} = V_{RFout} = 3.0 V) – with application circuit example – (S_{22} data are monitored at RF connector on board.)

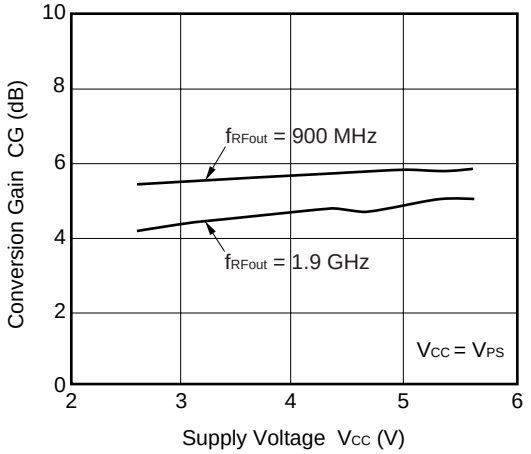




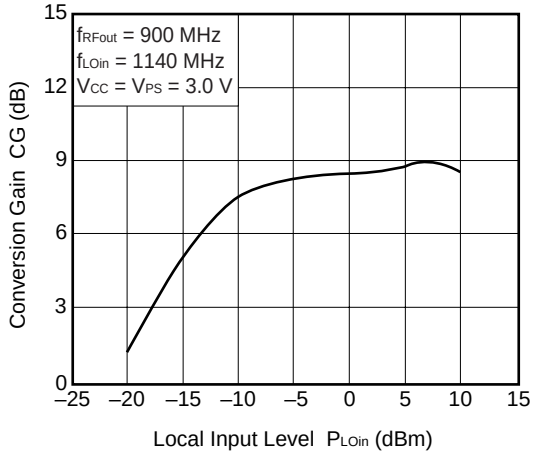
CONVERSION GAIN vs. SUPPLY VOLTAGE (μPC8106TB)



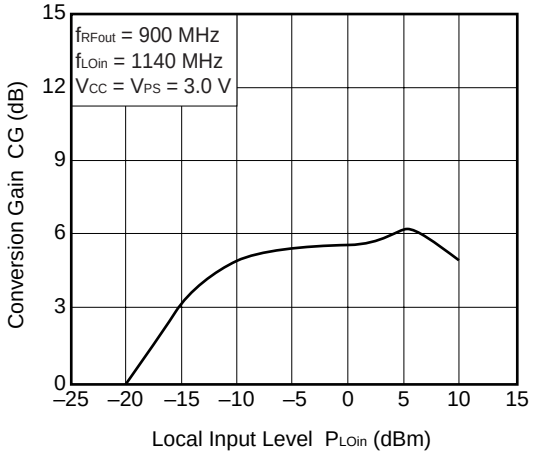
CONVERSION GAIN vs. SUPPLY VOLTAGE (μPC8109TB)



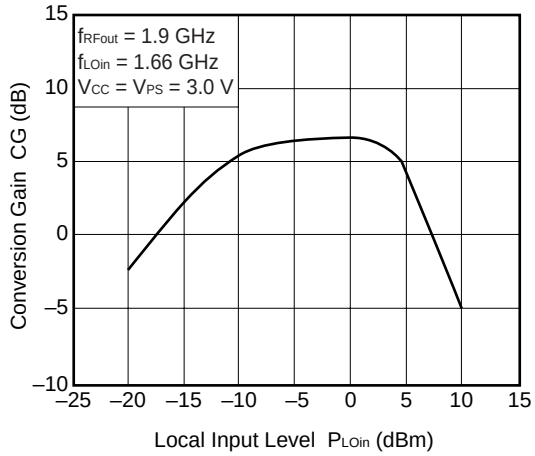
CONVERSION GAIN vs. LOCAL INPUT LEVEL (μPC8106TB)



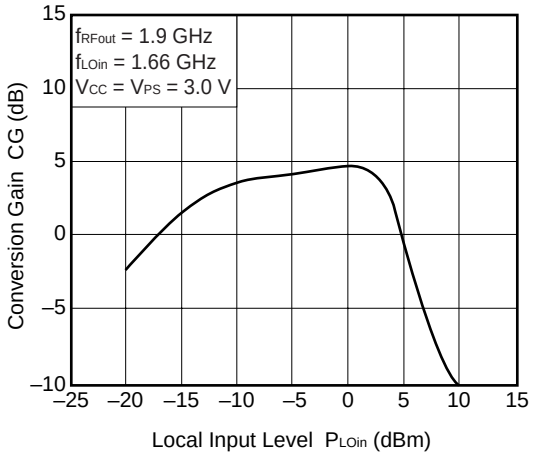
CONVERSION GAIN vs. LOCAL INPUT LEVEL (μPC8109TB)



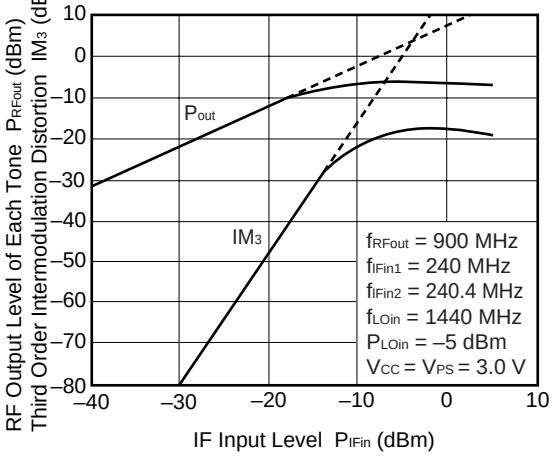
CONVERSION GAIN vs. LOCAL INPUT LEVEL (μPC8106TB)



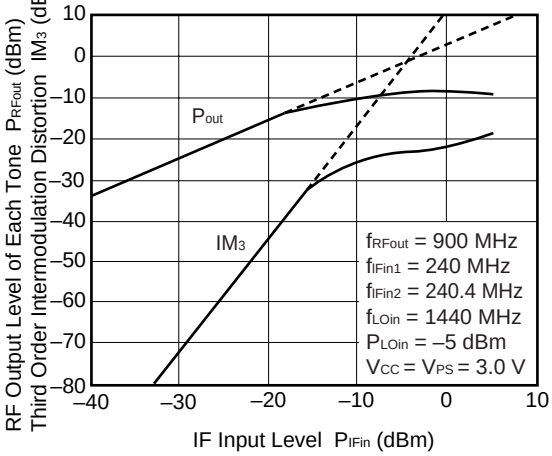
CONVERSION GAIN vs. LOCAL INPUT LEVEL (μPC8109TB)



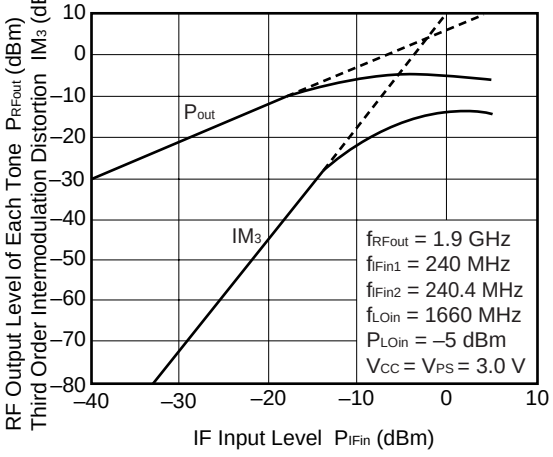
RF OUTPUT LEVEL AND IM_3 vs. IF INPUT LEVEL (μPC8106TB)



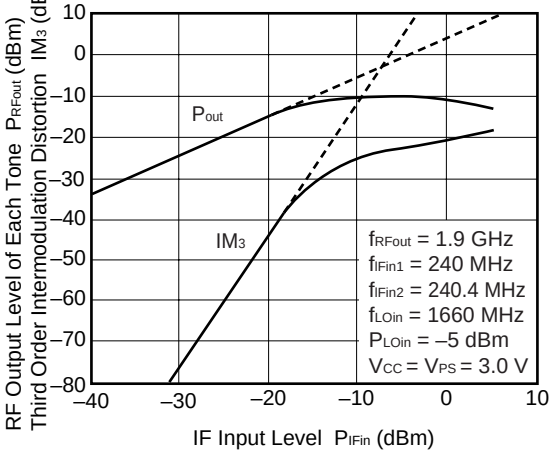
RF OUTPUT LEVEL AND IM_3 vs. IF INPUT LEVEL (μPC8109TB)



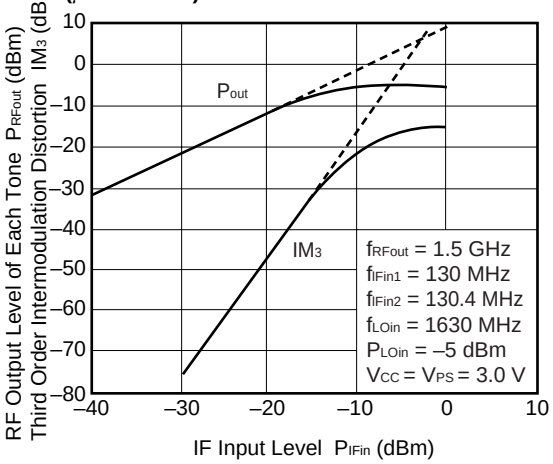
RF OUTPUT LEVEL AND IM_3 vs. IF INPUT LEVEL (μPC8106TB)



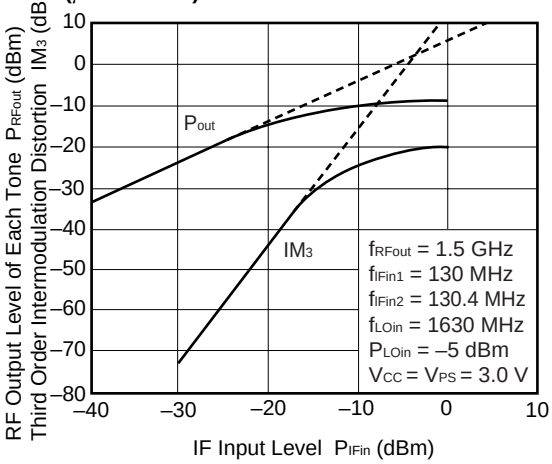
RF OUTPUT LEVEL AND IM_3 vs. IF INPUT LEVEL (μPC8109TB)



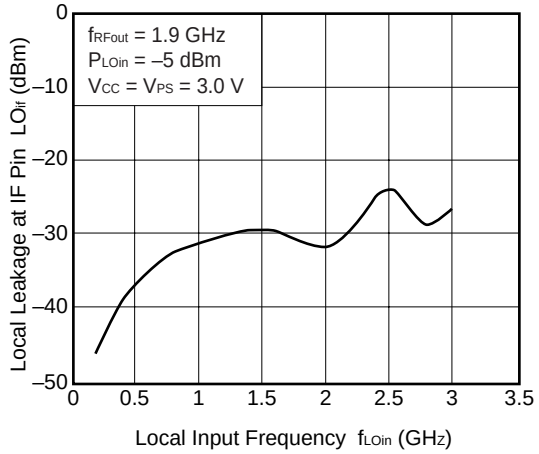
RF OUTPUT LEVEL AND IM_3 vs. IF INPUT LEVEL (μPC8106TB)



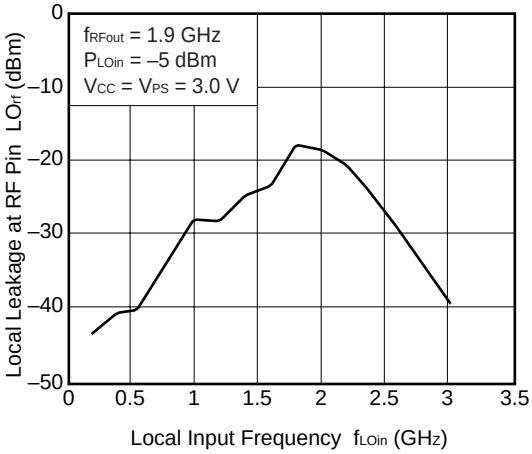
RF OUTPUT LEVEL AND IM_3 vs. IF INPUT LEVEL (μPC8109TB)



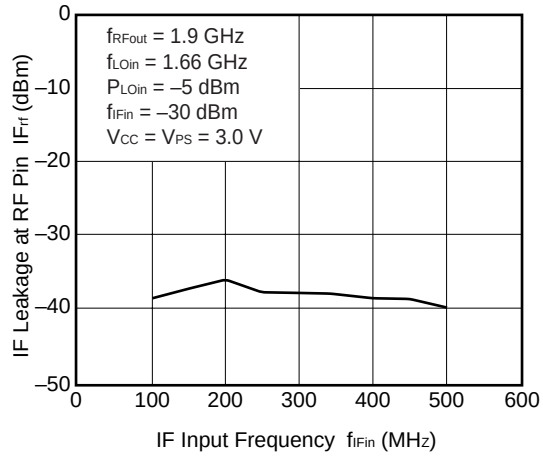
LOCAL LEAKAGE AT IF PIN vs. LOCAL INPUT FREQUENCY (μPC8106TB)



LOCAL LEAKAGE AT RF PIN vs. LOCAL INPUT FREQUENCY (μPC8106TB)

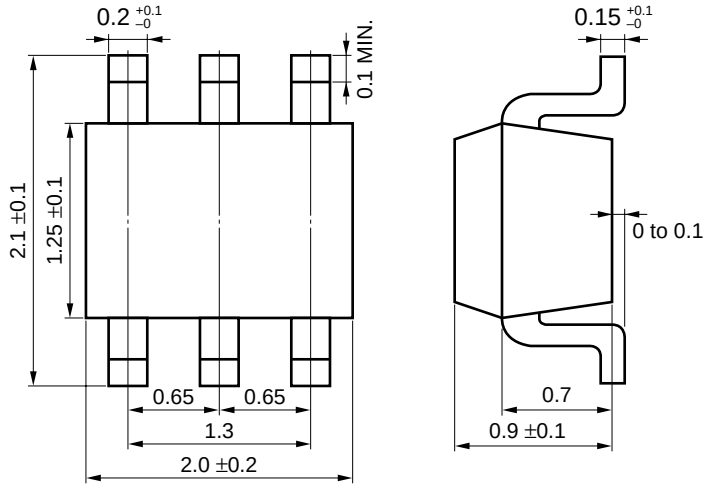


IF LEAKAGE AT RF PIN vs. IF INPUT FREQUENCY (μPC8106TB)



PACKAGE DIMENSIONS

6 pin super minimold (Unit: mm)



NOTES ON CORRECT USE

(1) Observe precutions for handling because of electrostatic sensitive devices.
(2) Form a ground pattern wide as possible to minimize ground impedance (to prevent undesired oscillation).
(3) Keep the wiring length of the ground pins as short as possible.
(4) Connect a bypass capacitor to the V_{CC} pin.
(5) Connect a matching circuit to the RF output pin.

RECOMMENDED SOLDERING CONDITIONS

This product should be soldered under the following recommended conditions. For soldering methods and conditions other than those recommended below, contact your NEC sales representative.

Soldering Method	Soldering Conditions	Recommended Condition Symbol
Infrared Reflow	Package peak temperature: 235°C or below Time: 30 seconds or less (at 210°C) Count: 3, Exposure limit: None[Note]	IR35-00-3
VPS	Package peak temperature: 215°C or below Time: 40 seconds or less (at 200°C) Count: 3, Exposure limit: None[Note]	VP15-00-3
Wave Soldering	Soldering bath temperature: 260°C or below Time: 10 seconds or less Count: 1, Exposure limit: None[Note]	WS60-00-1
Partial Heating	Pin temperature: 300°C Time: 3 seconds or less (per side of device) Exposure limit: None[Note]	–

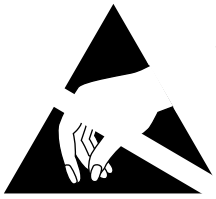
Note After opening the dry pack, keep it in a place below 25°C and 65% RH for the allowable storage period.

Caution Do not use different soldering methods together (except for partial heating).

For details of recommended soldering conditions for surface mounting, refer to information document SEMICONDUCTOR DEVICE MOUNTING TECHNOLOGY MANUAL (C10535E).

[MEMO]

[MEMO]



ATTENTION

OBSERVE PRECAUTIONS
FOR HANDLING
ELECTROSTATIC
SENSITIVE
DEVICES

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- NEC devices are classified into the following three quality grades:
  "Standard", "Special", and "Specific". The Specific quality grade applies only to devices developed based on a customer designated "quality assurance program" for a specific application. The recommended applications of a device depend on its quality grade, as indicated below. Customers must check the quality grade of each device before using it in a particular application.
  - Standard: Computers, office equipment, communications equipment, test and measurement equipment, audio and visual equipment, home electronic appliances, machine tools, personal electronic equipment and industrial robots
  - Special: Transportation equipment (automobiles, trains, ships, etc.), traffic control systems, anti-disaster systems, anti-crime systems, safety equipment and medical equipment (not specifically designed for life support)
  - Specific: Aircraft, aerospace equipment, submersible repeaters, nuclear reactor control systems, life support systems or medical equipment for life support, etc.

  The quality grade of NEC devices is "Standard" unless otherwise specified in NEC's Data Sheets or Data Books. If customers intend to use NEC devices for applications other than those specified for Standard quality grade, they should contact an NEC sales representative in advance.

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