NEC

BIPOLAR ANALOG INTEGRATED CIRCUIT

μPC8102T

RF AMPLIFIER IC FOR 150 MHz TO 330 MHz PAGER SYSTEM

DESCRIPTION

μPC8102T is a silicon monolisic integrated circuit designed as RF amplifier for 150 MHz to 330 MHz pager system. Due to 1 V supply voltage, this IC is suitable for low voltage pager system. The package is a 6 pin mini mold suitable for high-density surface mounting.

This IC is manufactured using NEC's 20 GHz f_T NESAT^{TM} III silicon bipolar process. This process uses silicon nitride passivation film and gold electrodes. These materials contribute excellent DC, AC performance. Thus, this process is utilized for 1 V voltage IC.

FEATURES

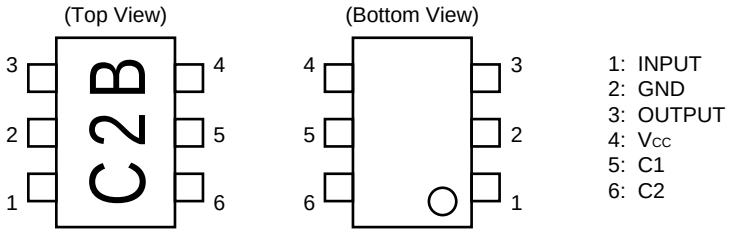
- 1 V supply voltage: V_{CC} = 0.9 V to 2.0 V
- Low noise figure: 2.3 $dB_{TYP.}$ @ f_{in} = 150 MHz (with external matching circuit to optimize NF)
- Low current consumption: I_{CC} = 0.5 $mA_{TYP.}$ @ V_{CC} = 1.0 V
- Gain available frequency: f_{RF} = 150 MHz to 330 MHz (with external matching circuit)
- High-density surface mounting: 6 pin mini mold

ORDERING INFORMATION

PART NUMBER	PACKAGE	MARKING	SUPPLYING FORM
μPC8102T-E3	6 pin mini mold	C2B	Embossed tape 8 mm wide. Pin 1, 2, 3 face to perforation side of tape. QTY 3 kp/Reel

***** For evaluation sample order, please contact your local NEC sales office.
(Order number: μPC8102T).

PIN CONNECTIONS



1: INPUT
2: GND
3: OUTPUT
4: V_{CC}
5: C1
6: C2

Caution Electro-static sensitive devices

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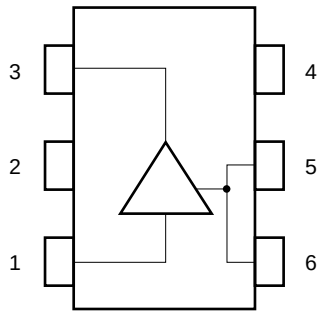
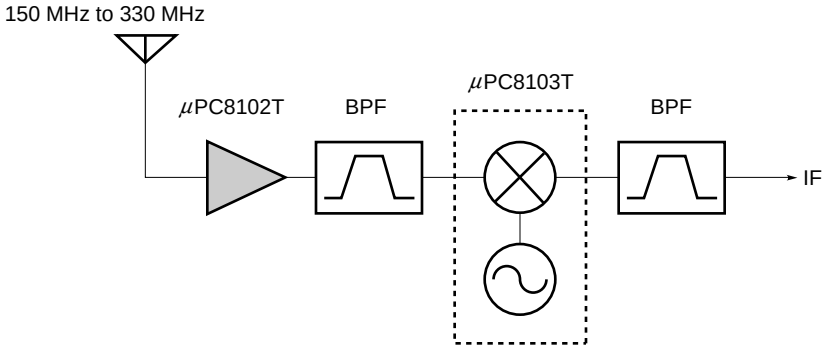
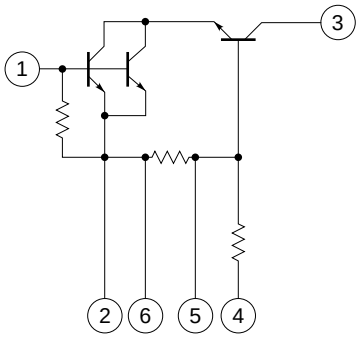
INTERNAL BLOCK DIAGRAM



SYSTEM APPLICATION EXAMPLE AS PAGER



PIN EXPLANATION

PIN NO.	NAME	SUPPLY VOLTAGE (V)	PIN VOLTAGE (V)	FUNCTION AND APPLICATION	EQUIVALENT CIRCUIT
1	INPUT	—	0.75	RF signal input pin. This pin should be externally equipped with matching circuit in accordance with desired frequency.	
2	GND	0	—	This ground pin must be connected to the system ground with minimum inductance. Ground pattern on the board should be formed as wide as possible. Track length should be kept as short as possible.	
3	OUTPUT	C2 pin voltage must be applied through external matching inductor	—	Amplified signal output pin. This pin should be externally equipped with matching circuit in accordance with desired frequency.	
4	V_{CC}	0.9 to 2.0	—	Supply voltage pin. Connect bypass capacitor (eg 1000 pF) to minimize ground impedance.	
5	C1	—	0.88	Ground with capacitance pin (eg 1000 pF).	
6	C2	—	0.85	AC ground pin for output	

Note Pin voltage values are described at V_{CC} = 1 V.

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	CONDITION	RATINGS	UNIT
Supply Voltage	V_{CC}	T_A = +25 °C	2.2	V
Power Dissipation	P_D	Mounted on 50 × 50 × 1.6 mm double copper clad epoxy glass PWB at T_A = +85 °C	280	mW
Operating Temperature	T_{opt}		–40 to +85	°C
Storage Temperature	T_{stg}		–55 to +150	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply Voltage	V_{CC}	0.9	1.0	2.0	V
Operating Temperature	T_{opt}	–40	+25	+85	°C
Operating Frequency	f_{opt}	150		330	MHz

Electric characteristic (T_A = +25 °C, V_{CC} = 1.0 V, Z_S = Z_L = 50 Ω)

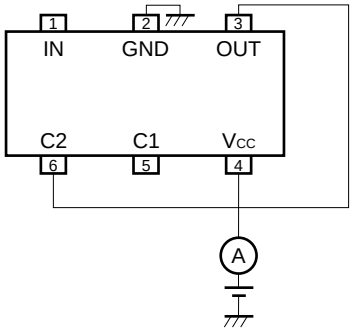
PARAMETER	SYMBOL	TEST CONDITIONS	μPC8102T			UNIT
			MIN.	TYP.	MAX.	
Circuit Current	I_{CC}	No input signal, TEST CIRCUIT 1	0.30	0.5	0.65	mA
Power Gain	G_P	f = 280 MHz, TEST CIRCUIT 3	10.0	13.5	16.5	dB
Output 3rd order intercept point	OIP_3	f_1 = 150.000 MHz, f_2 = 150.025 MHz TEST CIRCUIT 2	—	–5	—	dBm

Note External matching circuits should be attached to input and output pins.

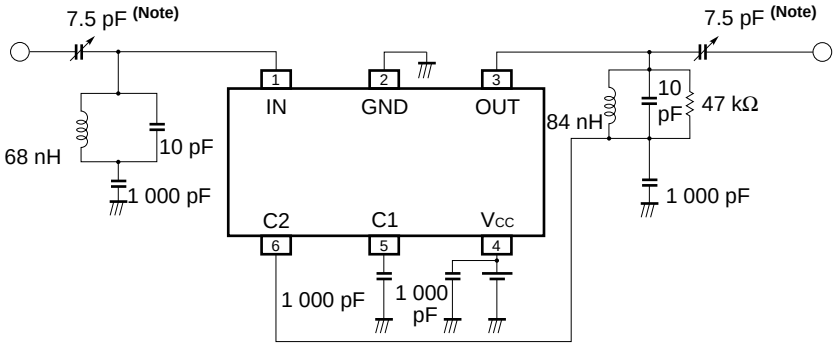
Standared characteristics for reference (Sample: I_{CC} = 0.55 mA, Condition: T_A = +25 °C, V_{CC} = 1.0 V)

PARAMETER	SYMBOL	CONDITIONS	Reference value	UNIT
matched with 50 Ω				
Power Gain 1	G_P1	f = 150 MHz, TEST CIRCUIT 2	20.6	dB
Noise Figure 1	NF1		3.6	dB
Power Gain 2	G_P2	f = 280 MHz, TEST CIRCUIT 3	14.7	dB
Noise Figure 2	NF2		4.0	dB
Power Gain 3	G_P3	f = 330 MHz, TEST CIRCUIT 5	14.5	dB
Noise Figure 3	NF3		4.1	dB
matched to optimize NF				
Power Gain 4	G_P4	f = 150 MHz, TEST CIRCUIT 2	19.4	dB
Noise Figure 4	NF4		2.3	dB
Power Gain 5	G_P5	f = 280 MHz, TEST CIRCUIT 4	14.0	dB
Noise Figure 5	NF5		2.9	dB
Power Gain 6	G_P6	f = 330 MHz, TEST CIRCUIT 6	11.6	dB
Noise Figure 6	NF6		3.1	dB

TEST CIRCUIT 1

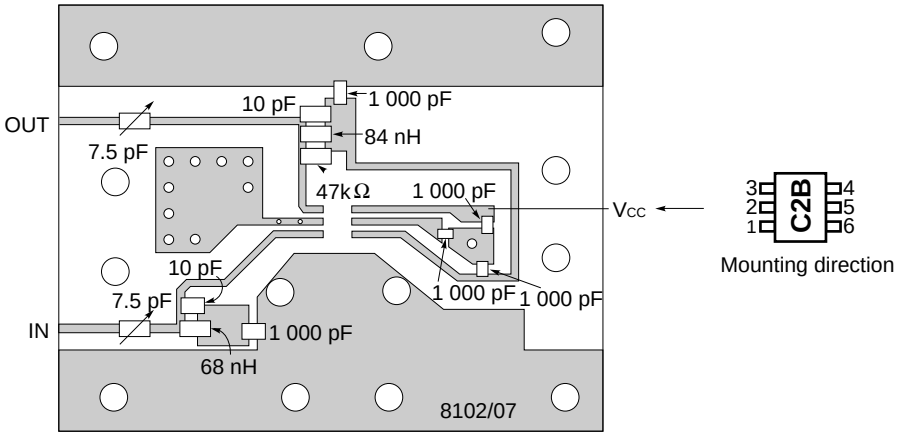


TEST CIRCUIT 2 (150 MHz) <Matched with 50 Ω or matched to optimize NF>



Note Matching can be adjusted with trimmer condenser.

ILLUSTRATION OF THE TEST CIRCUIT 2 ASSEMBLED ON EVALUATION BOARD



Note

(*1) 35 × 42 × 0.4 mm double copper clad polyimide board

(*2) Back side: GND pattern

(*3) Solder plated on pattern

(*4) ○◯ : Through holes

TEST CIRCUIT 3 (280 MHz) <Matched with 50 Ω>

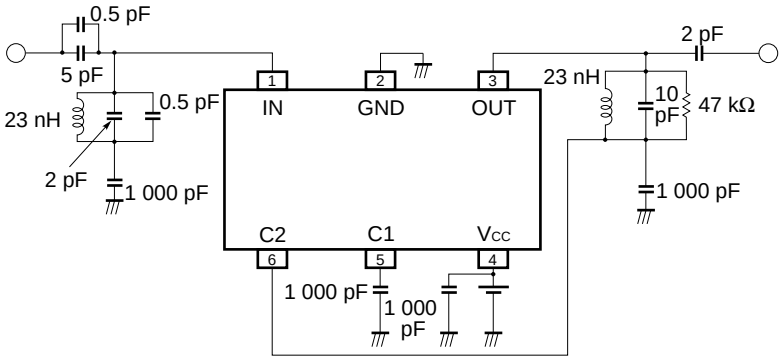
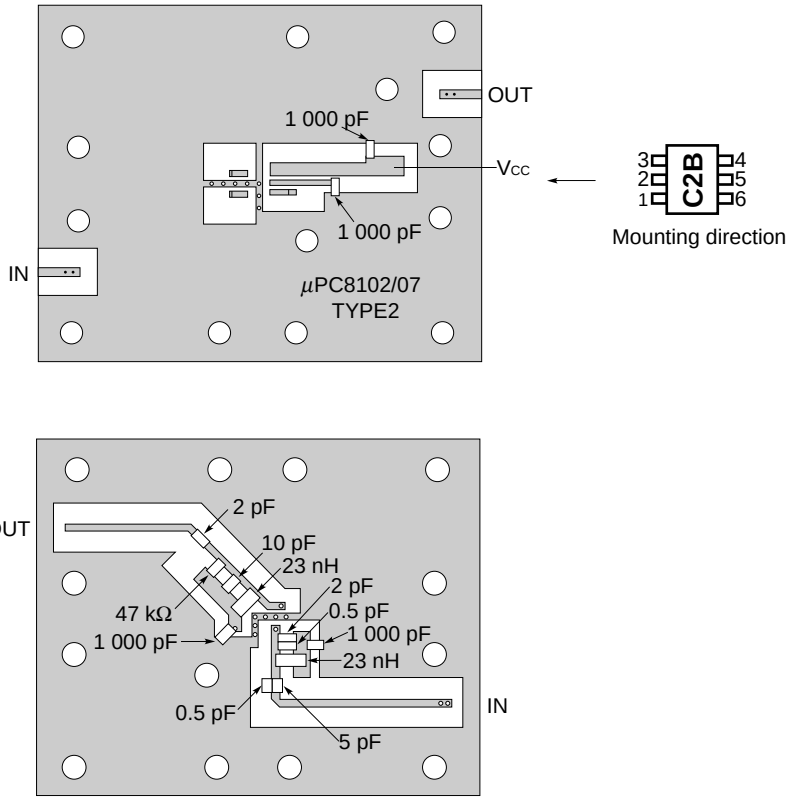


ILLUSTRATION OF THE TEST CIRCUIT 3 ASSEMBLED ON EVALUATION BOARD



Note

(*1) 35 × 42 × 0.4 mm double copper clad polyimide board

(*2) Solder plated on pattern

(*3) ○◯ : Through holes

TEST CIRCUIT 4 (280 MHz) <Matched to optimize NF>

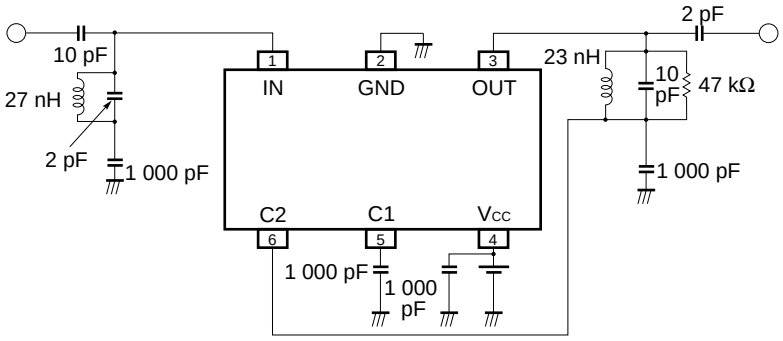
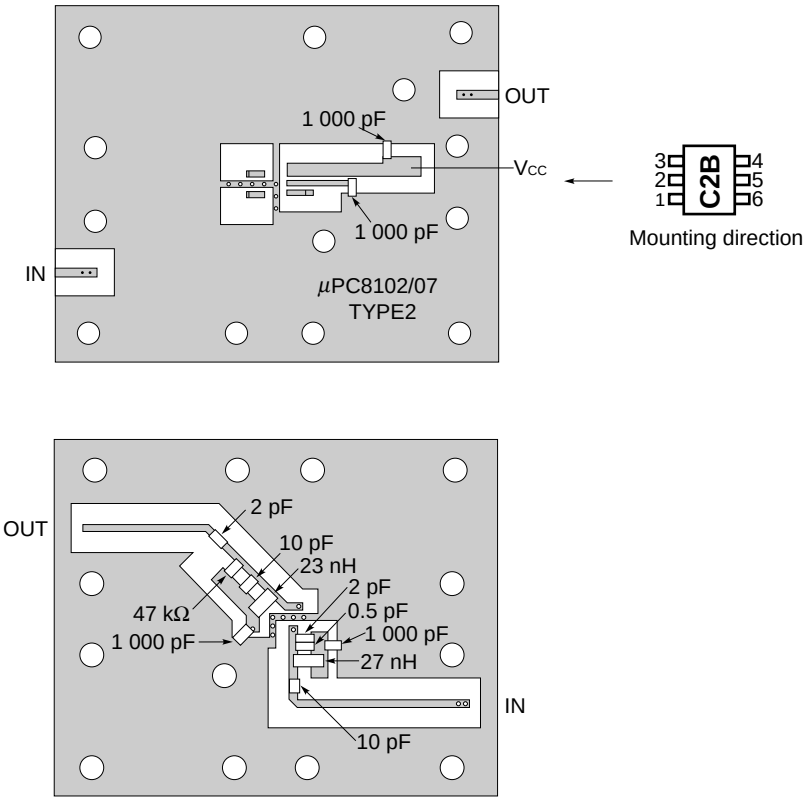


ILLUSTRATION OF THE TEST CIRCUIT 4 ASSEMBLED ON EVALUATION BOARD



Note

(*1) 35 × 42 × 0.4 mm double copper clad polyimide board

(*2) Solder plated on pattern

(*3) ○◯ : Through holes

TEST CIRCUIT 5 (330 MHz) <Matched with 50 Ω>

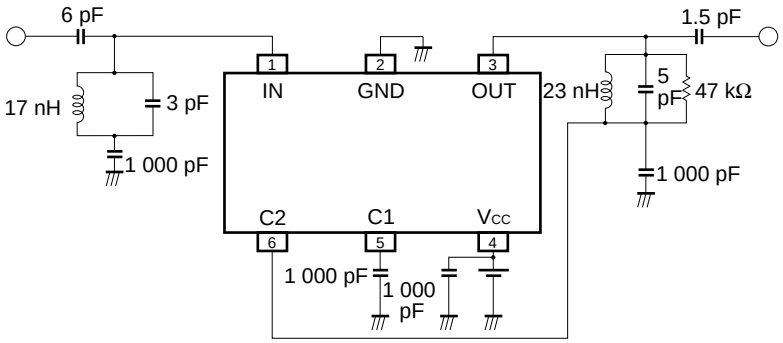
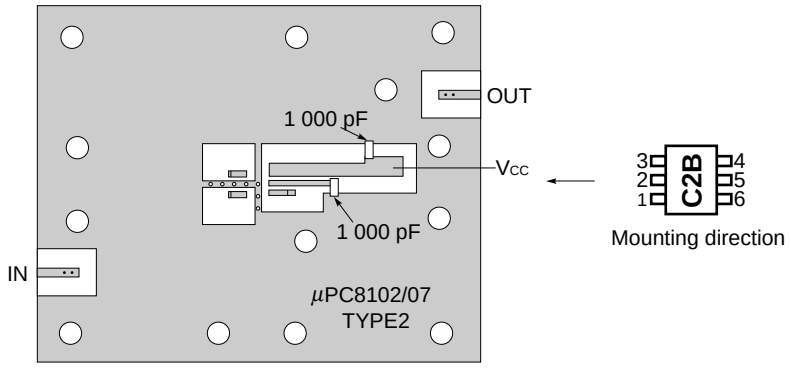
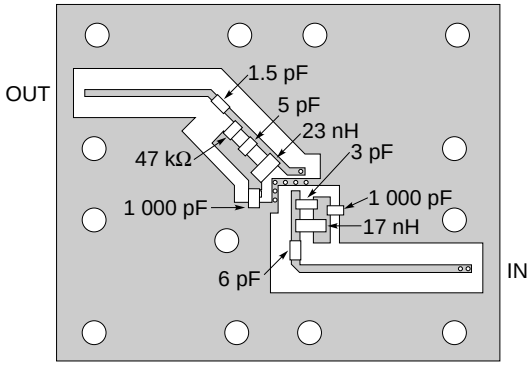


ILLUSTRATION ON THE TEST CIRCUIT 5 ASSEMBLED ON EVALUATION BOARD





Note

(*1) 35 × 42 × 0.4 mm double copper clad polyimide board

(*2) Solder plated on pattern

(*3) ○◯ : Through holes

TEST CIRCUIT 6 (330 MHz) <Matched to optimize NF>

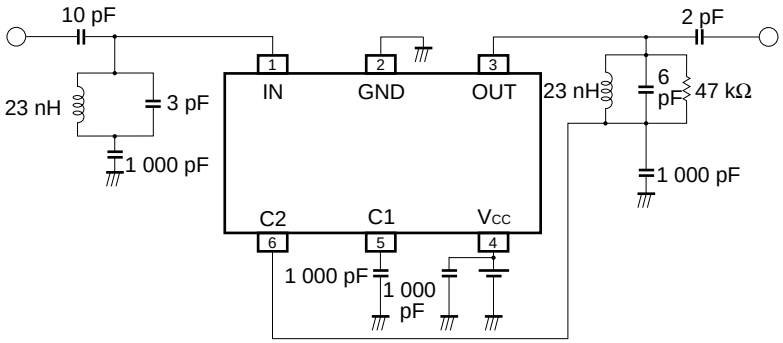
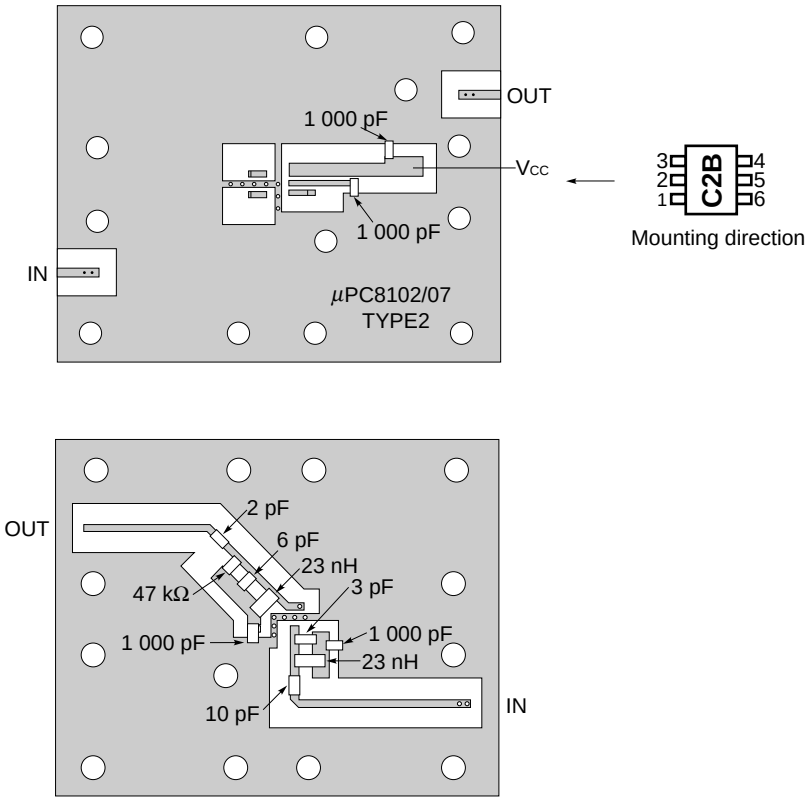


ILLUSTRATION ON THE TEST CIRCUIT 6 ASSEMBLED ON EVALUATION BOARD



Note

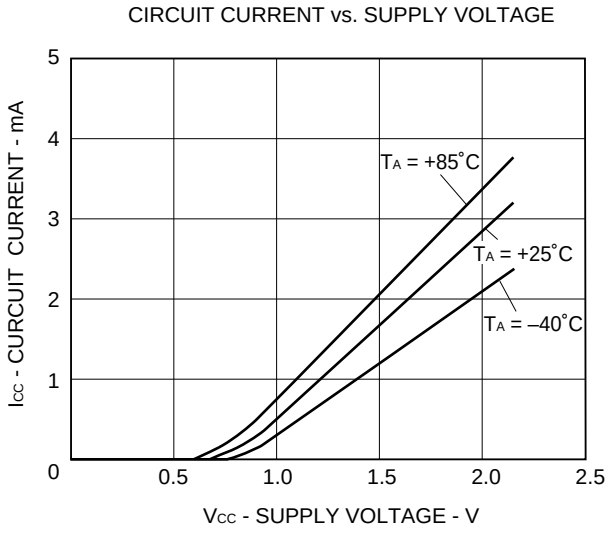
(*1) 35 × 42 × 0.4 mm double copper clad polyimide board

(*2) Solder plated on pattern

(*3) ○◯ : Through holes

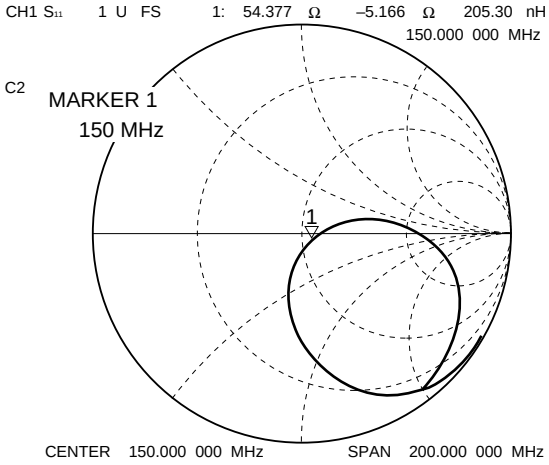
CHARACTERISTICS (T_A = +25 °C unless otherwise specified)

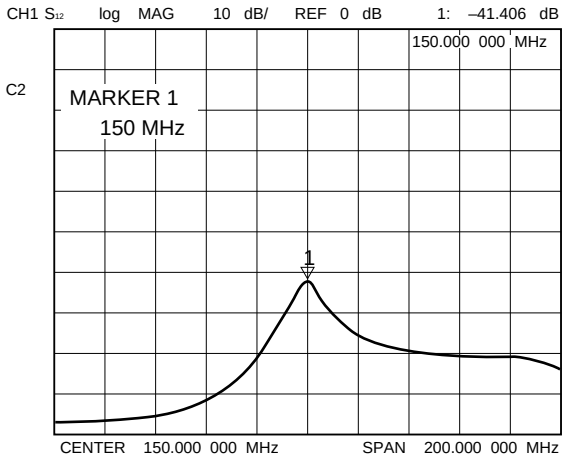
– TEST CIRCUIT 1 –

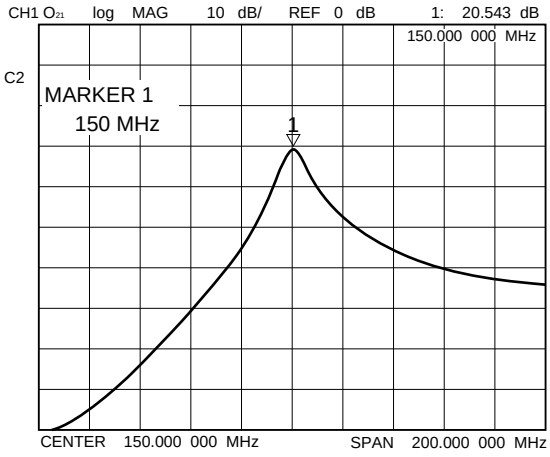


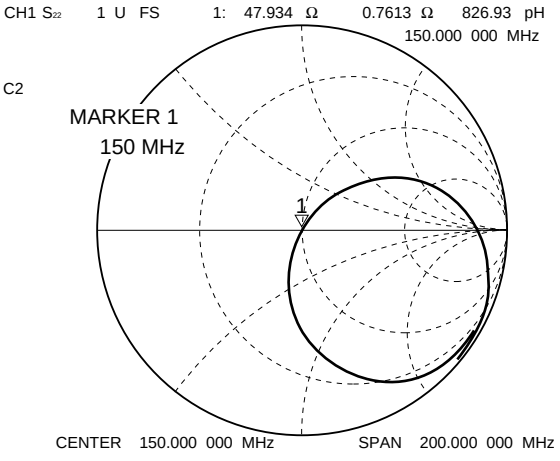
– TEST CIRCUIT 2 (matched with 50 Ω) –

150 MHz V_{CC} = 1.0 V , I_{CC} = 0.55 mA NF = 3.55 dB



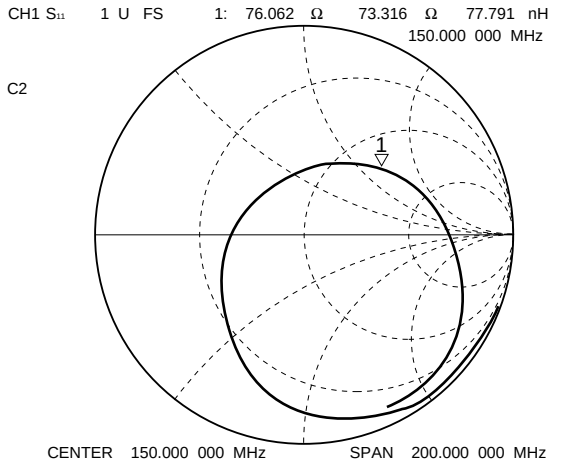


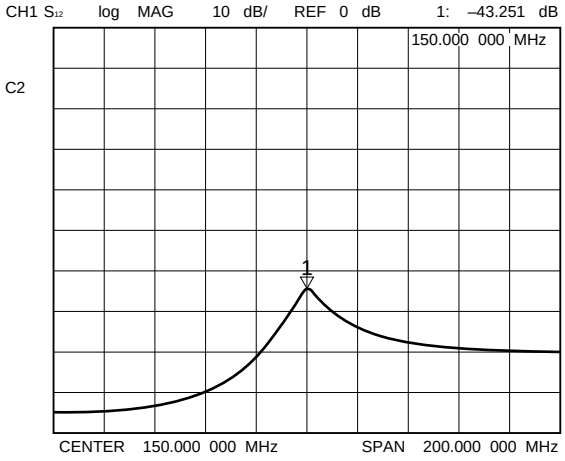


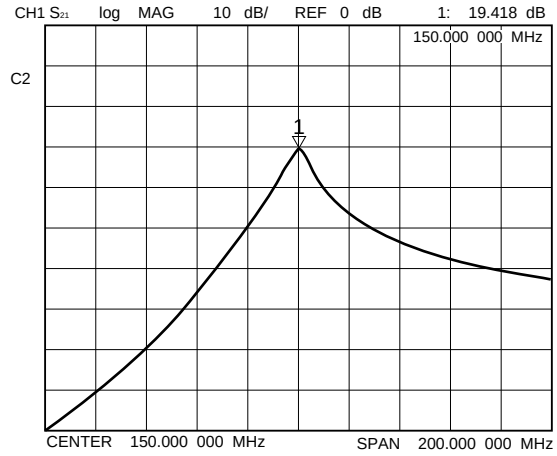


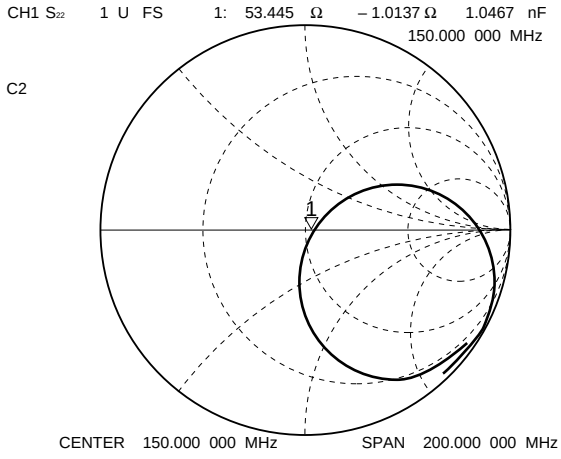
– TEST CIRCUIT 2 (matched to optimize NF) –

150 MHz V_{CC} = 1.0 V , I_{CC} = 0.55 mA NF = 2.25 dB



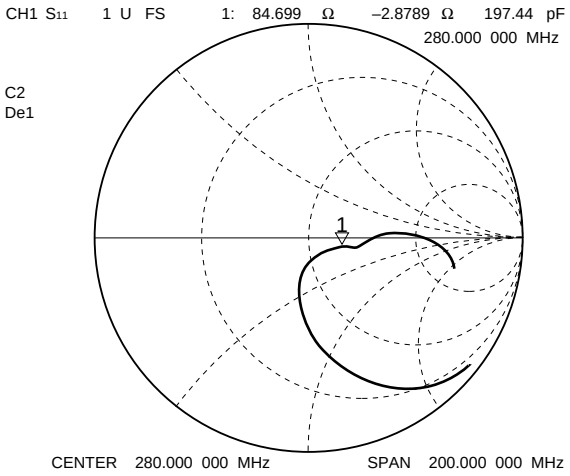


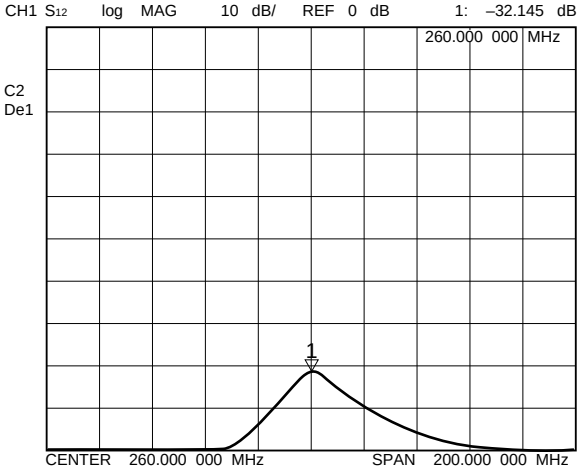


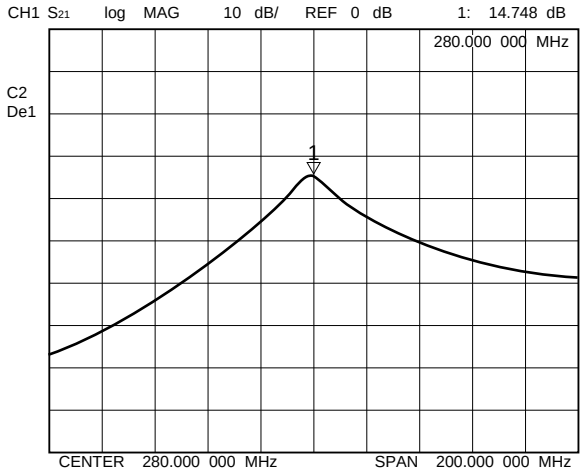


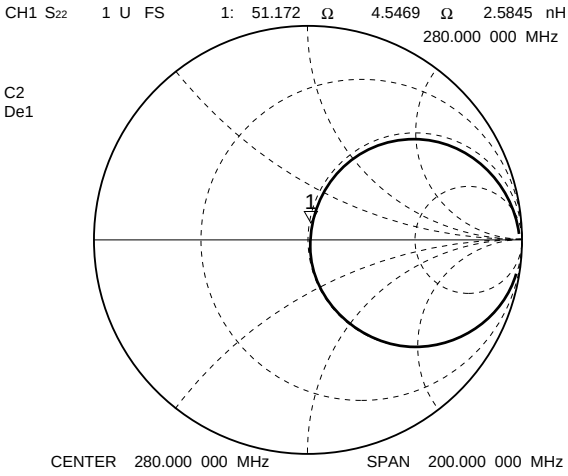
– TEST CIRCUIT 3 (matched with 50 Ω) –

280 MHz V_{CC} = 1.0 V , I_{CC} = 0.55 mA NF = 4.0 dB



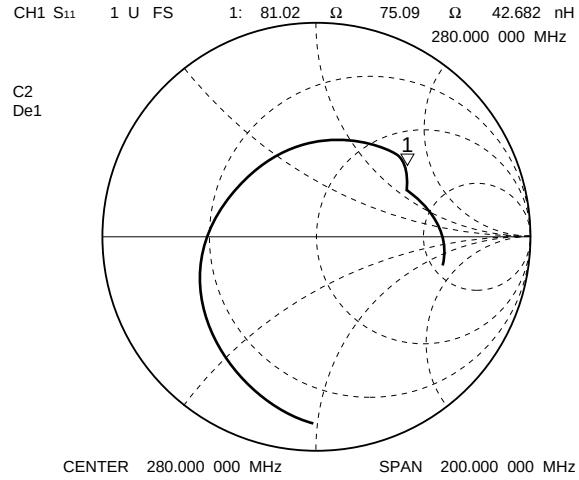


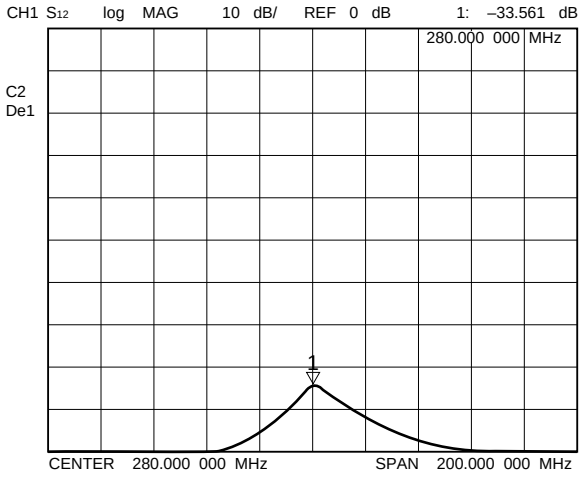


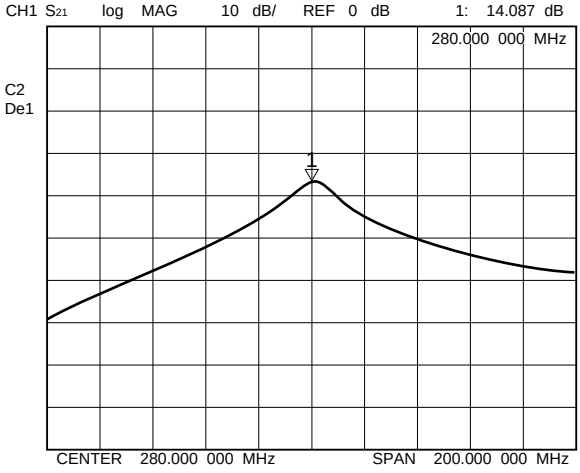


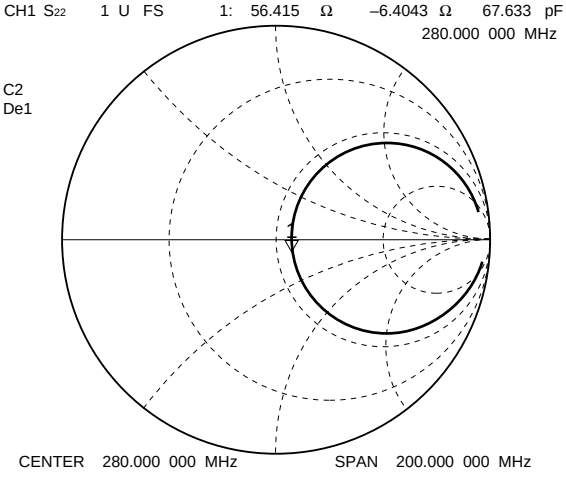
– TEST CIRCUIT 4 (matched to optimize NF) –

280 MHz V_{CC} = 1.0 V , I_{CC} = 0.55 mA T_A = 25 ˚C NF = 2.93 dB



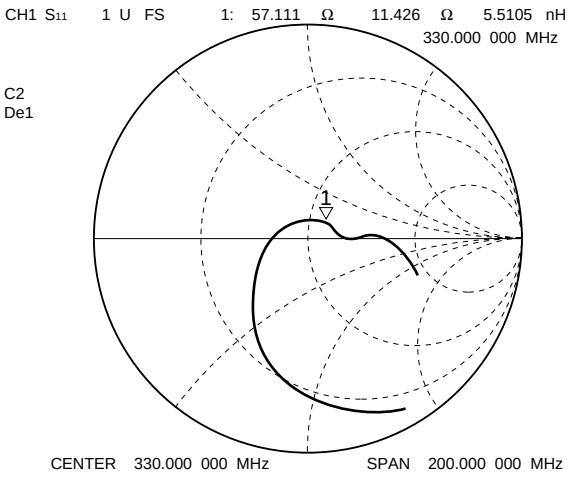


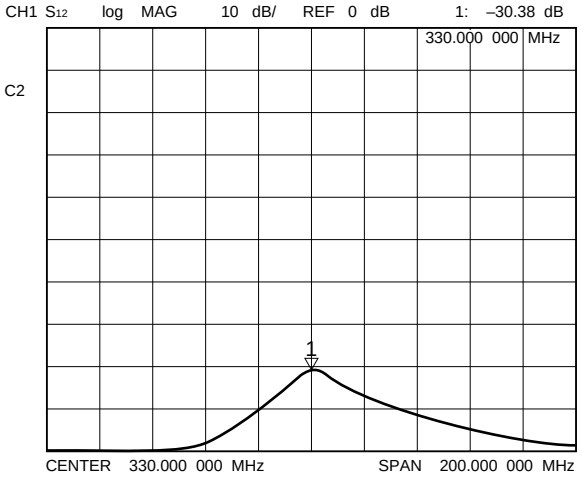


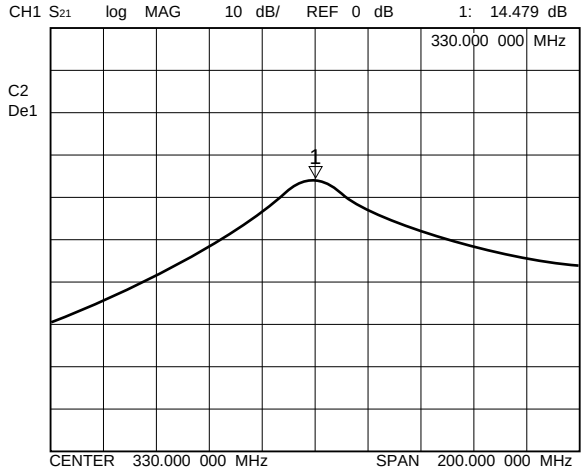


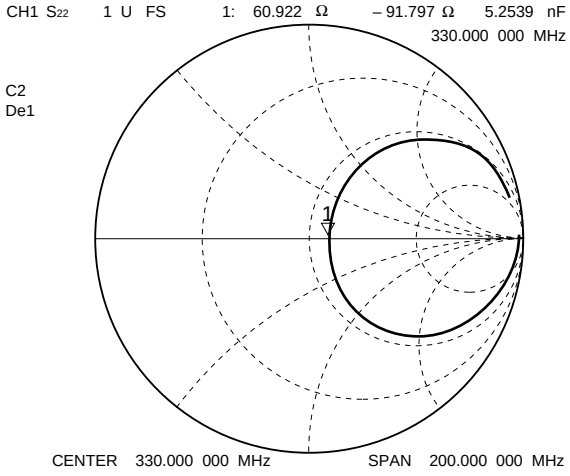
– TEST CIRCUIT 5 (matched with 50 Ω) –

330 MHz V_{CC} = 1.0 V , I_{CC} = 0.55 mA NF = 4.1 dB



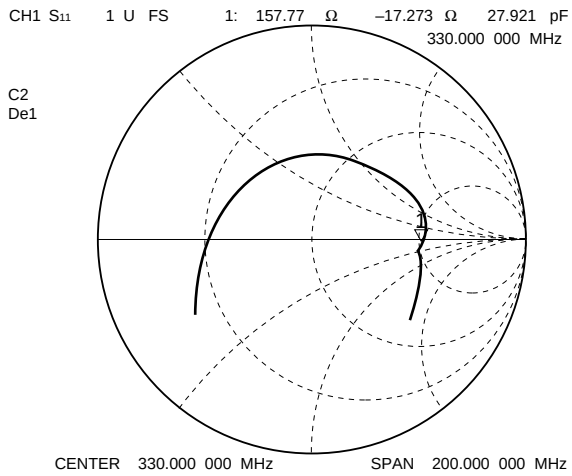


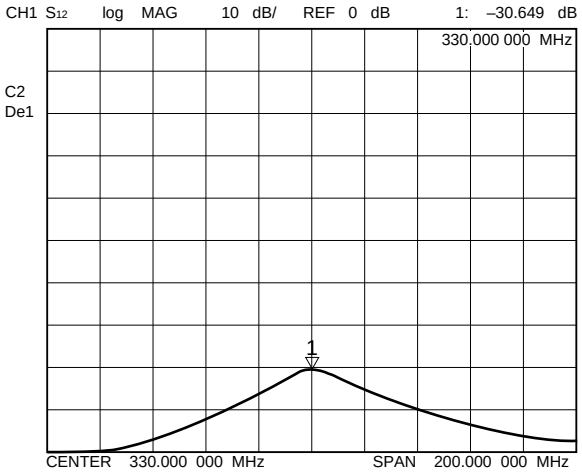


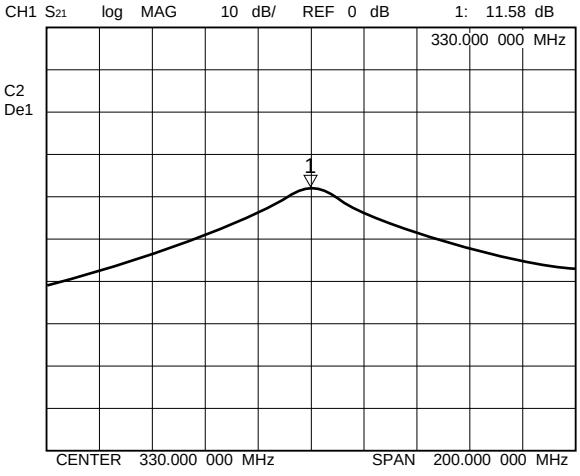


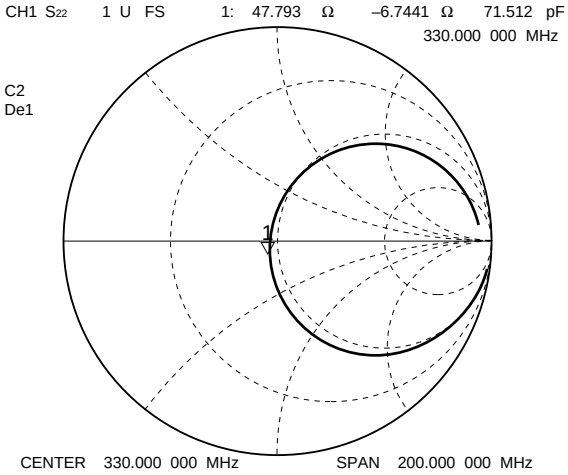
– TEST CIRCUIT 6 (matched to optimize NF) –

330 MHz V_{CC} = 1.00 V , I_{CC} = 0.55 mA NF = 3.14 dB



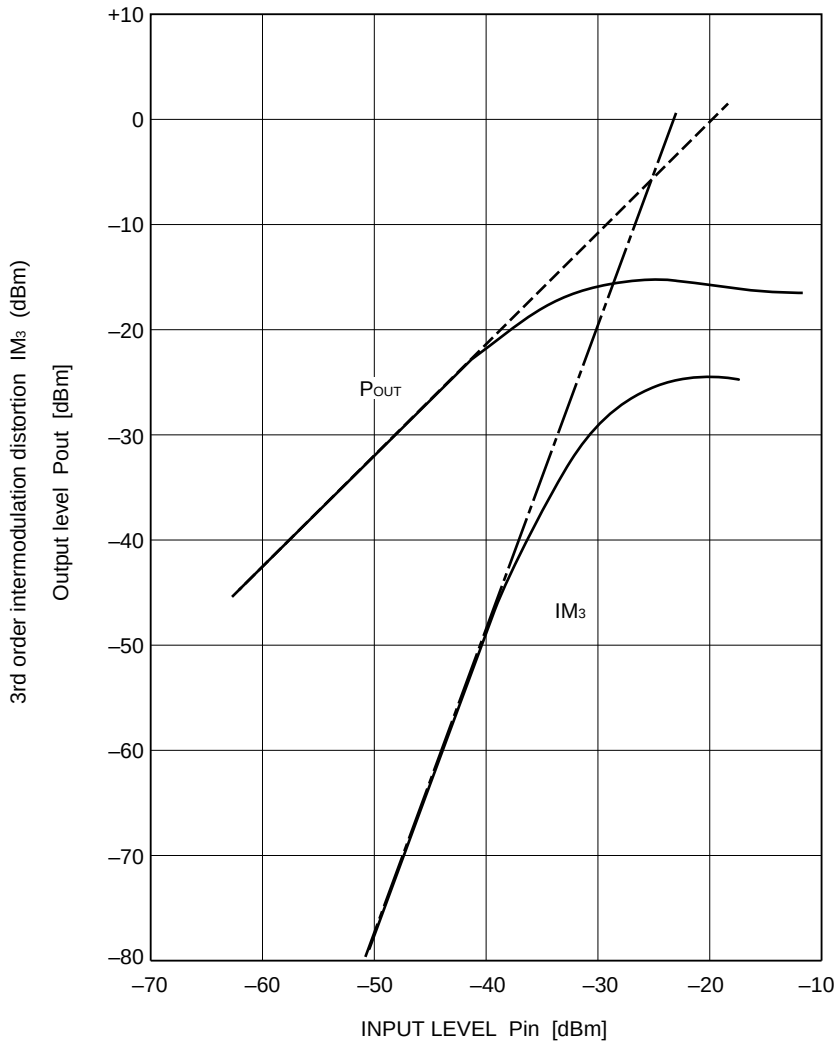




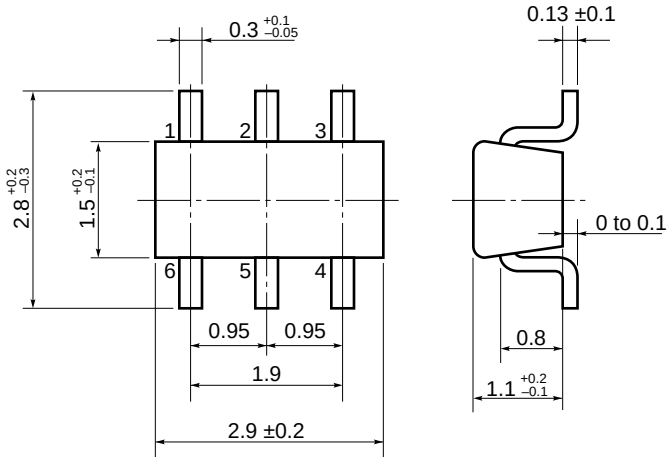


– TEST CIRCUIT 2 –

IM3 AND OUTPUT LEVEL vs. INPUT LEVEL (150 MHz)



6 PIN MINI MOLD PACKAGE DIMENSIONS (Unit: mm)



NOTE ON CORRECT USE

(1) Observe precautions for handling because of electro-static sensitive devices.

(2) Form a ground pattern as wide as possible to minimize ground impedance (to prevent undesired oscillation).

(3) Keep the track length of the ground pins as short as possible.

(4) The bypass capacitor (eg 1 000 pF) should be attached to the V_{CC} pin.

(5) The matching circuit must be each attached to input and output pins.

RECOMMENDED SOLDERING CONDITIONS

This product should be soldered in the following recommended conditions. Other soldering methods and conditions than the recommended conditions are to be consulted with our sales representatives.

μPC8102T

Soldering process	Soldering conditions	Recommended condition symbol
Infrared ray reflow	Package peak temperature: 235 ˚C, Hour: within 30 s. (more than 210 ˚C), Time: 3 time, Limited days: no.*	IR35-00-3
VPS	Package peak temperature: 215 ˚C, Hour: within 40 s. (more than 200 ˚C), Time: 3 time, Limited days: no.*	VP15-00-3
Wave Soldering	Soldering tub temperature: less than 260 ˚C, Hour: within 10 s. Time: 1 time, Limited days: no.*	WS60-00-1
Pin part heating	Pin area temperature: less than 300 ˚C, Hour: within 3 s/pin. Limited days: no.*	

***** It is the storage days after opening a dry pack, the storage conditions are 25 ˚C, less than 65 % RH.

Note The combined use of soldering method is to be avoided (However, except the pin area heating method).

For details of recommended soldering conditions for surface mounting, refer to information document **SEMICONDUCTOR DEVICE MOUNTING TECHNOLOGY MANUAL (C10535EJ7V0IF00)**.

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