

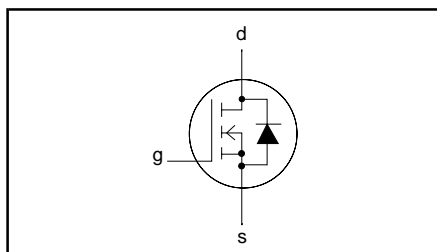
**N-channel TrenchMOS™ transistor
Logic level FET**

**PHP55N03LT, PHB55N03LT
PHD55N03LT**

FEATURES

- 'Trench' technology
- Very low on-state resistance
- Fast switching
- Low thermal resistance
- Logic level compatible

SYMBOL



QUICK REFERENCE DATA

| |
|--|
| $V_{DSS} = 25\text{ V}$ |
| $I_D = 55\text{ A}$ |
| $R_{DS(ON)} \leq 14\text{ m}\Omega (V_{GS} = 10\text{ V})$ |
| $R_{DS(ON)} \leq 18\text{ m}\Omega (V_{GS} = 5\text{ V})$ |

GENERAL DESCRIPTION

N-channel enhancement mode logic level field-effect power transistor in a plastic envelope using 'trench' technology.

Applications:-

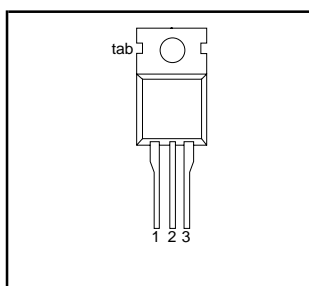
- High frequency computer motherboard d.c. to d.c. converters
- High current switching

The PHP55N03LT is supplied in the SOT78 (TO220AB) conventional leaded package.
The PHB55N03LT is supplied in the SOT404 (D²PAK) surface mounting package.
The PHD55N03LT is supplied in the SOT428 (DPAK)surface mounting package.

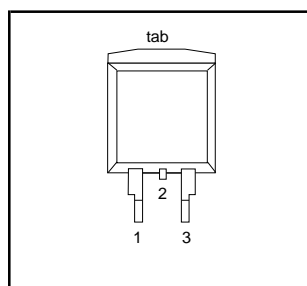
PINNING

| PIN | DESCRIPTION |
|-----|--------------------|
| 1 | gate |
| 2 | drain ¹ |
| 3 | source |
| tab | drain |

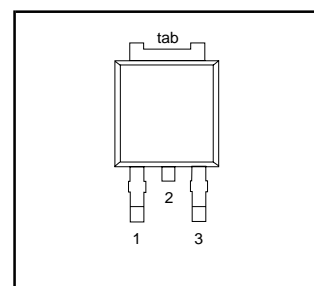
SOT78 (TO220AB)



SOT404 (D²PAK)



SOT428 (DPAK)



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

| SYMBOL | PARAMETER | CONDITIONS | MIN. | MAX. | UNIT |
|----------------|--|--|------|----------|------------------|
| V_{DSS} | Drain-source voltage | $T_j = 25\text{ }^\circ\text{C}$ to $175\text{ }^\circ\text{C}$ | - | 25 | V |
| V_{DGR} | Drain-gate voltage | $T_j = 25\text{ }^\circ\text{C}$ to $175\text{ }^\circ\text{C}$; $R_{GS} = 20\text{ k}\Omega$ | - | 25 | V |
| V_{GS} | Gate-source voltage (DC) | | - | ± 15 | V |
| V_{GSM} | Gate-source voltage (pulse peak value) | $T_j \leq 150\text{ }^\circ\text{C}$ | - | ± 20 | V |
| I_D | Drain current (DC) | $T_{mb} = 25\text{ }^\circ\text{C}$ | - | 55 | A |
| | | $T_{mb} = 100\text{ }^\circ\text{C}$ | - | 38 | A |
| I_{DM} | Drain current (pulse peak value) | $T_{mb} = 25\text{ }^\circ\text{C}$ | - | 220 | A |
| P_{tot} | Total power dissipation | $T_{mb} = 25\text{ }^\circ\text{C}$ | - | 103 | W |
| T_j, T_{stg} | Operating junction and storage temperature | | - 55 | 175 | $^\circ\text{C}$ |

¹ It is not possible to make connection to pin:2 of the SOT404 or SOT428 packages.

N-channel TrenchMOS™ transistor Logic level FET

PHP55N03LT, PHB55N03LT
PHD55N03LT

THERMAL RESISTANCES

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|----------------|--|--|------|------|------|------|
| $R_{th\ j-mb}$ | Thermal resistance junction to mounting base | | - | - | 1.45 | K/W |
| $R_{th\ j-a}$ | Thermal resistance junction to ambient | SOT78 package, in free air SOT404 and SOT428 packages, pcb mounted, minimum footprint | - | 60 | - | K/W |
| | | | - | 50 | - | K/W |

AVALANCHE LIMITING VALUE

| SYMBOL | PARAMETER | CONDITIONS | MIN. | MAX. | UNIT |
|-----------|---|--|------|------|------|
| W_{DSS} | Drain-source non-repetitive unclamped inductive turn-off energy | $I_D = 25\text{ A}$; $V_{DD} \leq 15\text{ V}$; $V_{GS} = 5\text{ V}$; $R_{GS} = 50\ \Omega$; $T_{mb} = 25\text{ °C}$ | - | 60 | mJ |

ELECTRICAL CHARACTERISTICS

$T_j = 25\text{ °C}$ unless otherwise specified

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---------------|----------------------------------|---|------|------|------|---------------|
| $V_{(BR)DSS}$ | Drain-source breakdown voltage | $V_{GS} = 0\text{ V}$; $I_D = 0.25\text{ mA}$; $T_j = -55\text{ °C}$ | 25 | - | - | V |
| $V_{GS(TO)}$ | Gate threshold voltage | $V_{DS} = V_{GS}$; $I_D = 1\text{ mA}$ $T_j = 175\text{ °C}$ $T_j = -55\text{ °C}$ | 1 | 1.5 | 2 | V |
| | | | 0.5 | - | - | V |
| | | | - | - | 2.3 | V |
| $R_{DS(ON)}$ | Drain-source on-state resistance | $V_{GS} = 10\text{ V}$; $I_D = 25\text{ A}$ $V_{GS} = 10\text{ V}$; $I_D = 25\text{ A}$ (SOT428 package) $V_{GS} = 5\text{ V}$; $I_D = 25\text{ A}$ $V_{GS} = 5\text{ V}$; $I_D = 25\text{ A}$; $T_j = 175\text{ °C}$ | - | 11 | 14 | m Ω |
| | | | - | 14 | 16 | m Ω |
| | | | - | 15 | 18 | m Ω |
| | | | - | - | 34 | m Ω |
| g_{fs} | Forward transconductance | $V_{DS} = 25\text{ V}$; $I_D = 25\text{ A}$ | 10 | 28 | - | S |
| I_{GSS} | Gate source leakage current | $V_{GS} = \pm 5\text{ V}$; $V_{DS} = 0\text{ V}$ | - | 10 | 100 | nA |
| I_{DSS} | Zero gate voltage drain current | $V_{DS} = 25\text{ V}$; $V_{GS} = 0\text{ V}$; $T_j = 175\text{ °C}$ | - | 0.05 | 10 | μA |
| | | | - | - | 500 | μA |
| $Q_{g(tot)}$ | Total gate charge | $I_D = 55\text{ A}$; $V_{DD} = 15\text{ V}$; $V_{GS} = 5\text{ V}$ | - | 20 | - | nC |
| Q_{gs} | Gate-source charge | | - | 8 | - | nC |
| Q_{gd} | Gate-drain (Miller) charge | | - | 9 | - | nC |
| $t_{d\ on}$ | Turn-on delay time | $V_{DD} = 15\text{ V}$; $I_D = 25\text{ A}$; | - | 7 | 15 | ns |
| t_r | Turn-on rise time | $V_{GS} = 10\text{ V}$; $R_G = 5\ \Omega$ | - | 56 | 80 | ns |
| $t_{d\ off}$ | Turn-off delay time | Resistive load | - | 57 | 80 | ns |
| t_f | Turn-off fall time | | - | 38 | 50 | ns |
| L_d | Internal drain inductance | Measured tab to centre of die | - | 3.5 | - | nH |
| L_d | Internal drain inductance | Measured from drain lead to centre of die (SOT78 package only) | - | 4.5 | - | nH |
| L_s | Internal source inductance | Measured from source lead to source bond pad | - | 7.5 | - | nH |
| C_{iss} | Input capacitance | $V_{GS} = 0\text{ V}$; $V_{DS} = 20\text{ V}$; $f = 1\text{ MHz}$ | - | 1230 | - | pF |
| C_{oss} | Output capacitance | | - | 354 | - | pF |
| C_{rss} | Feedback capacitance | | - | 254 | - | pF |

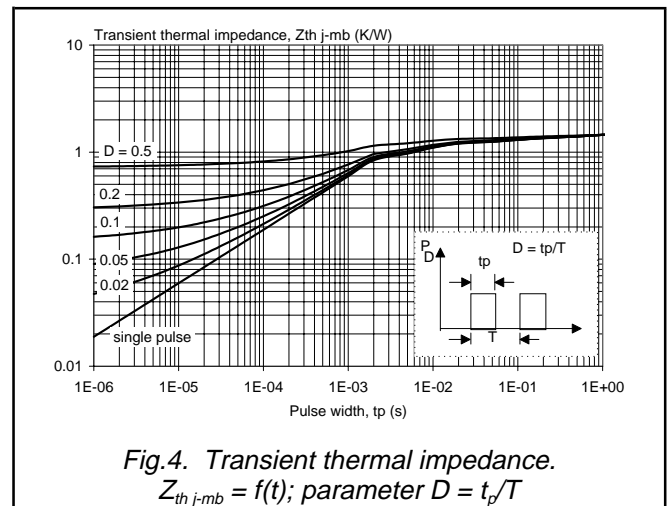
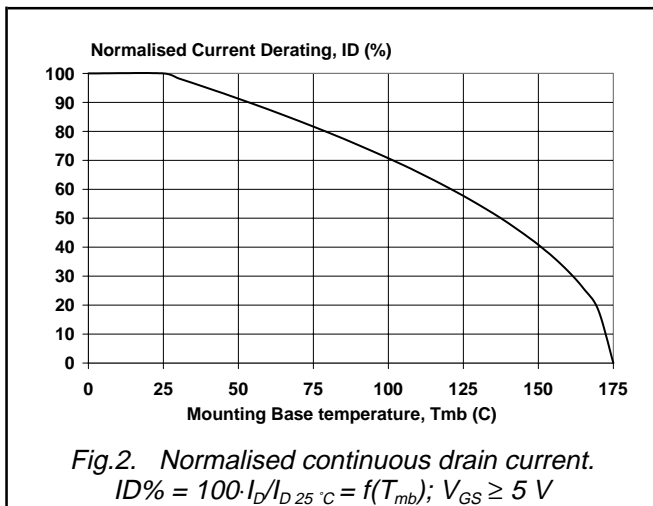
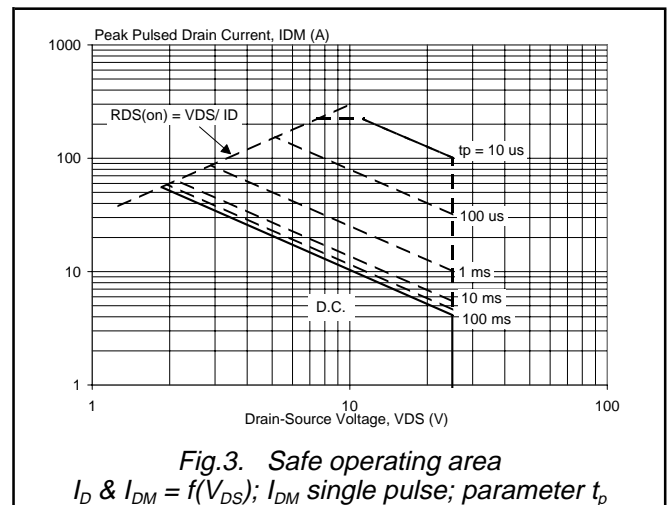
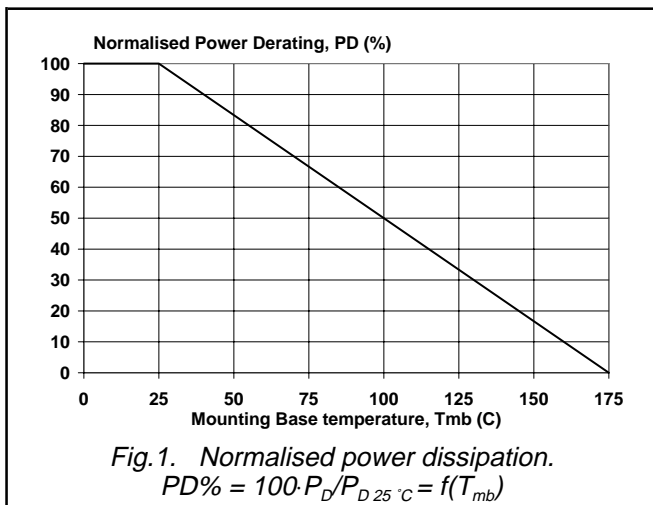
N-channel TrenchMOS™ transistor
Logic level FET

PHP55N03LT, PHB55N03LT
PHD55N03LT

REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS

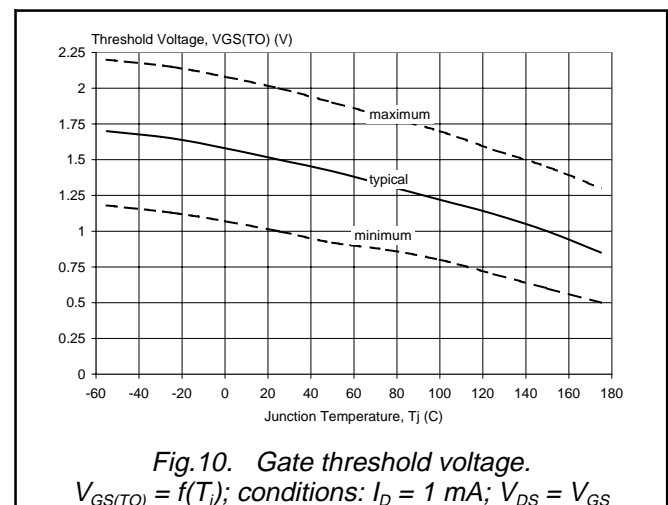
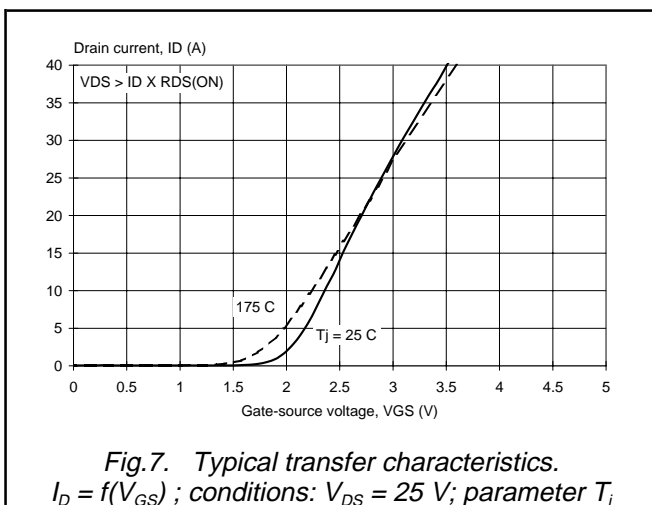
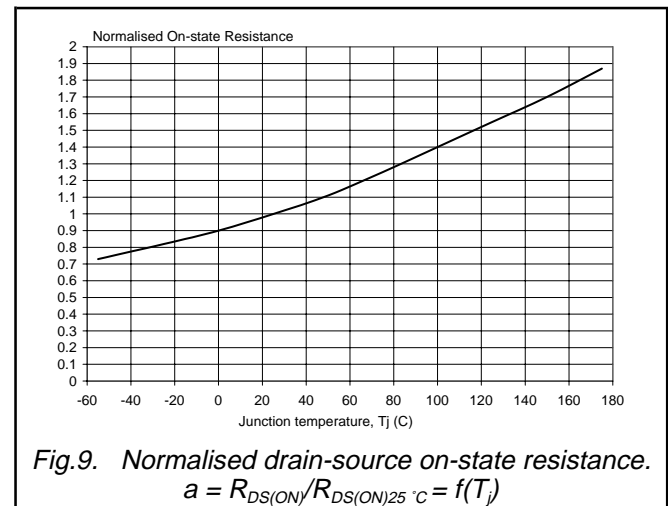
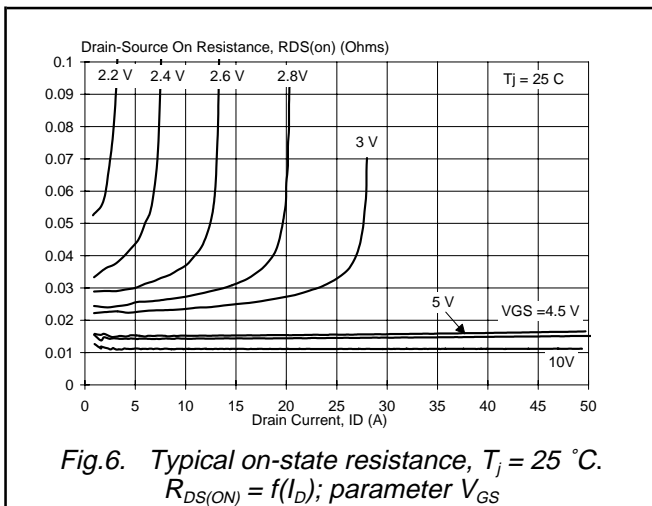
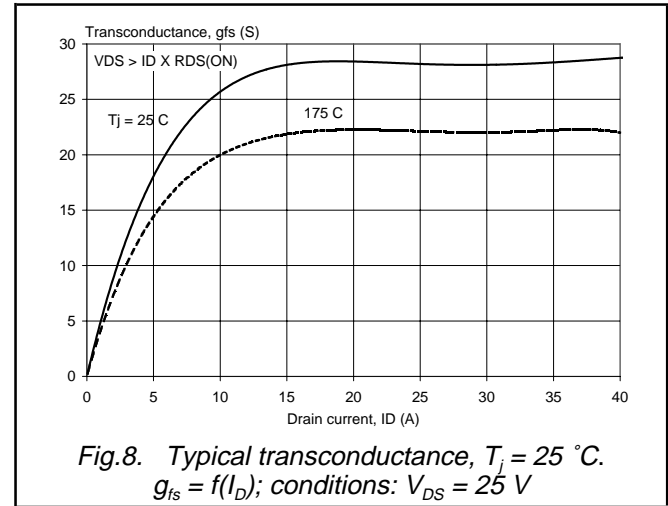
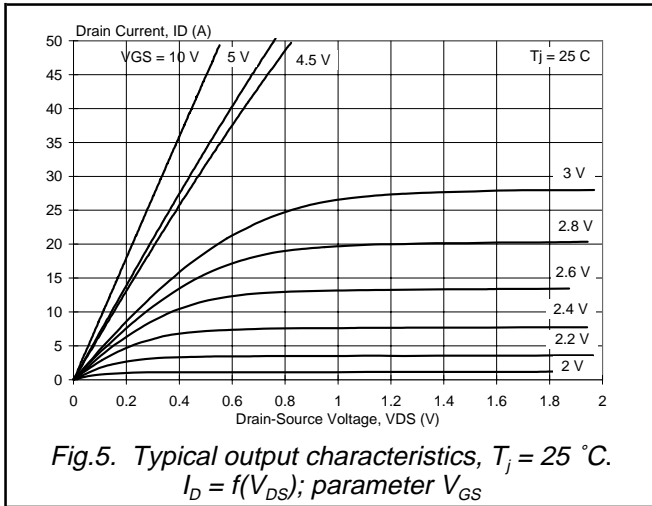
T_j = 25°C unless otherwise specified

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|-----------------|--|---|------|------------|----------|------|
| I _S | Continuous source current (body diode) | | - | - | 55 | A |
| I _{SM} | Pulsed source current (body diode) | | - | - | 220 | A |
| V _{SD} | Diode forward voltage | I _F = 25 A; V _{GS} = 0 V I _F = 55 A; V _{GS} = 0 V | - | 0.9 1.0 | 1.2 - | V |
| t _{rr} | Reverse recovery time | I _F = 20 A; -di _F /dt = 100 A/μs; V _{GS} = 0 V; V _R = 25 V | - | 87 | - | ns |
| Q _{rr} | Reverse recovery charge | | - | 0.1 | - | μC |



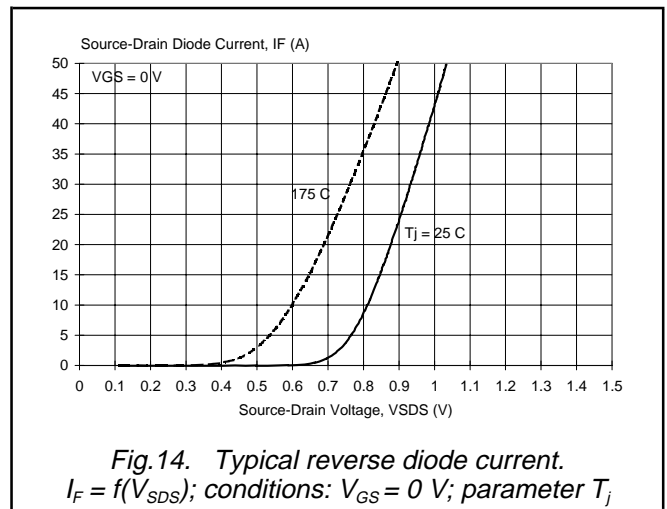
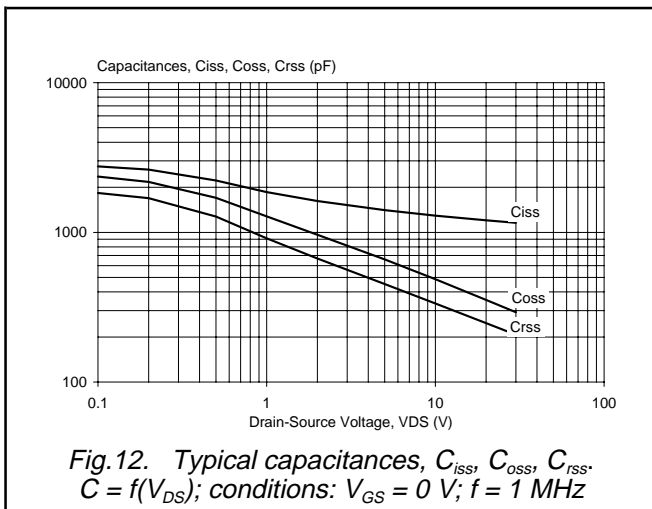
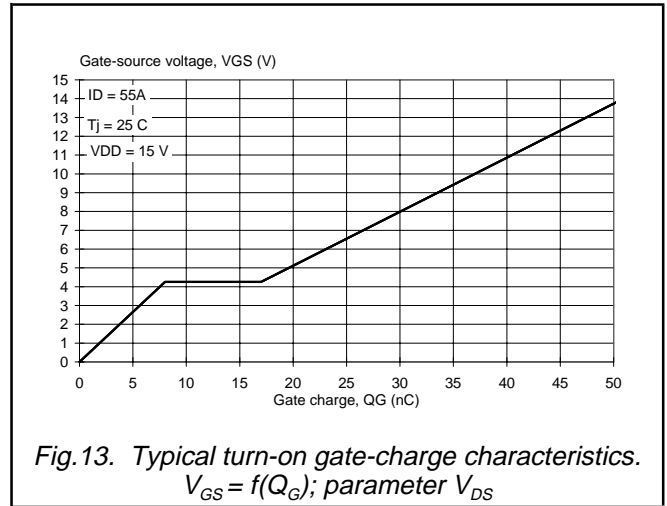
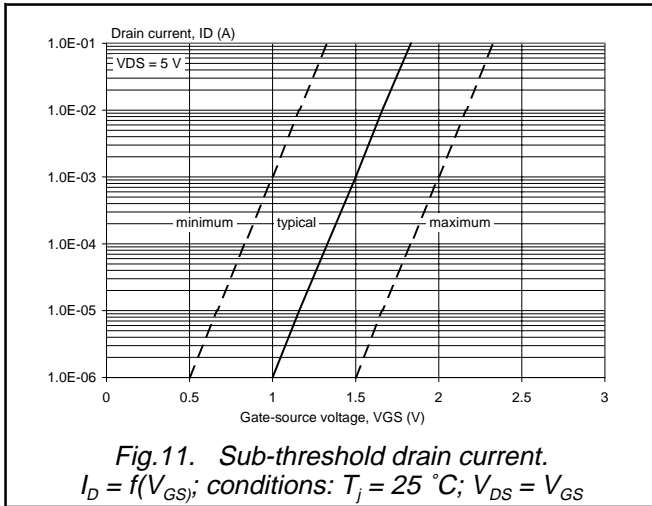
N-channel TrenchMOS™ transistor
Logic level FET

PHP55N03LT, PHB55N03LT
PHD55N03LT



N-channel TrenchMOS™ transistor
Logic level FET

PHP55N03LT, PHB55N03LT
PHD55N03LT



N-channel TrenchMOS™ transistor
Logic level FET

PHP55N03LT, PHB55N03LT
PHD55N03LT

MECHANICAL DATA

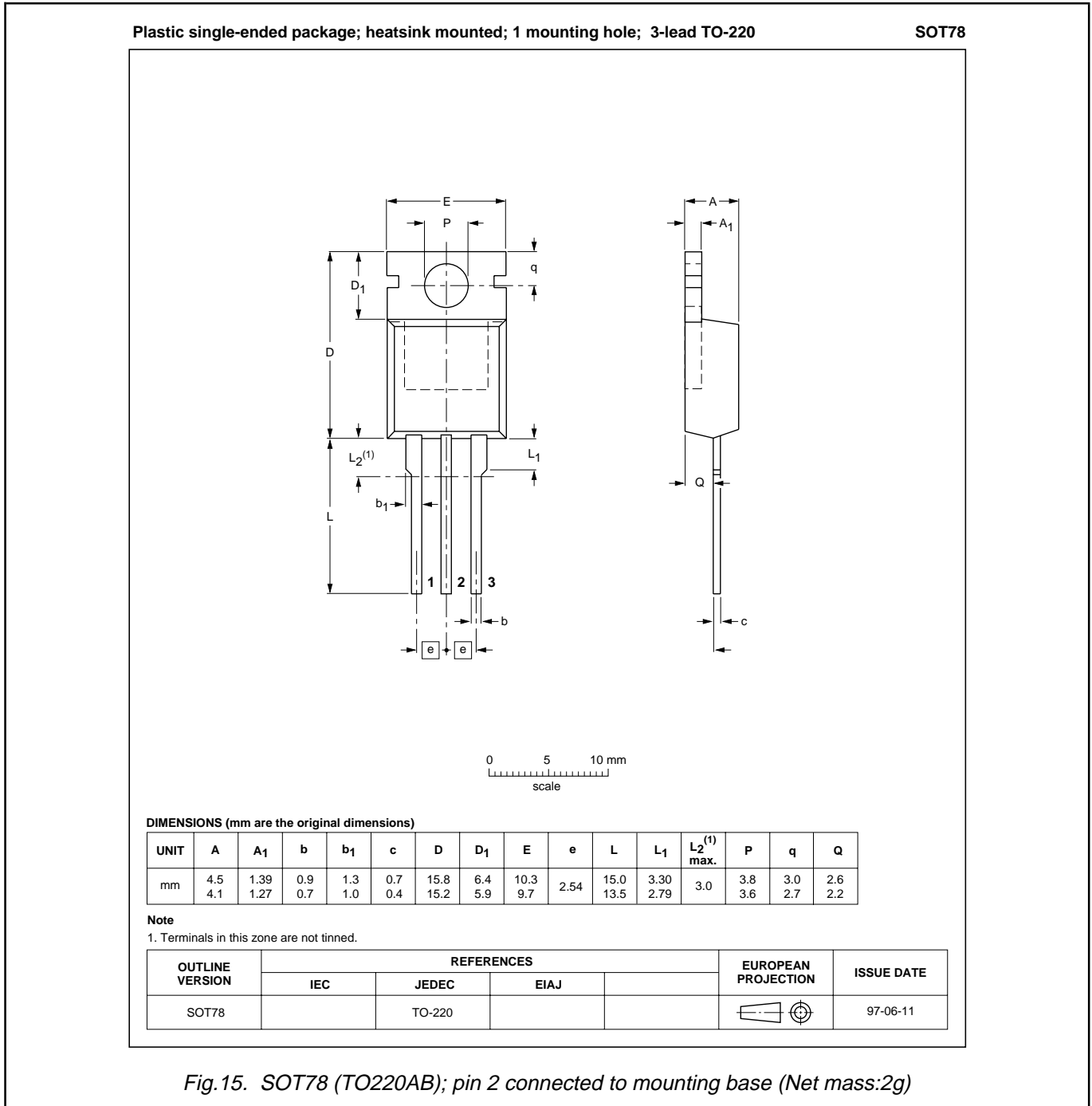


Fig. 15. SOT78 (TO220AB); pin 2 connected to mounting base (Net mass:2g)

Notes

1. This product is supplied in anti-static packaging. The gate-source input must be protected against static discharge during transport or handling.
2. Refer to mounting instructions for SOT78 (TO220AB) package.
3. Epoxy meets UL94 V0 at 1/8".

N-channel TrenchMOS™ transistor
Logic level FET

PHP55N03LT, PHB55N03LT
PHD55N03LT

MECHANICAL DATA

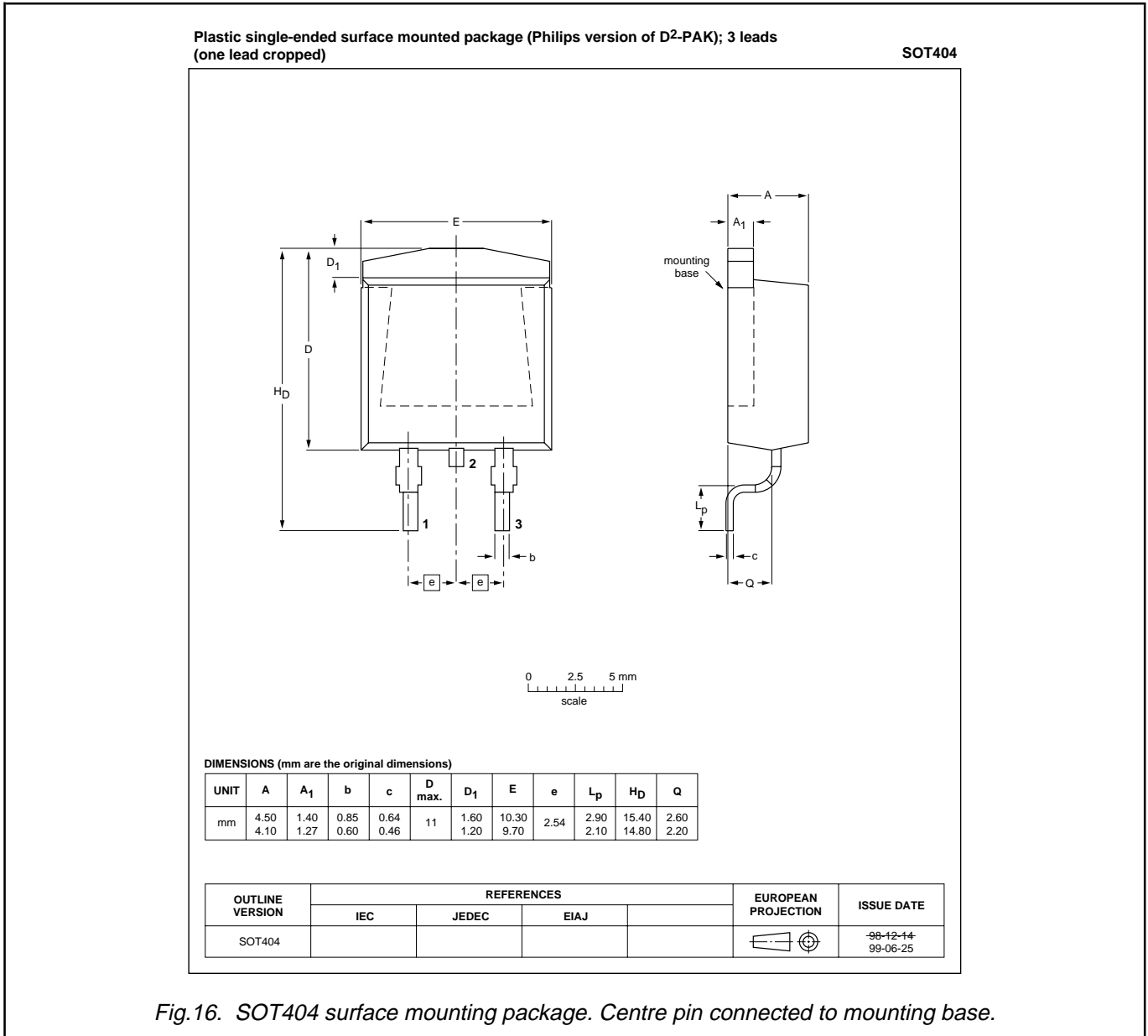


Fig.16. SOT404 surface mounting package. Centre pin connected to mounting base.

Notes

1. This product is supplied in anti-static packaging. The gate-source input must be protected against static discharge during transport or handling.
2. Refer to SMD Footprint Design and Soldering Guidelines, Data Handbook SC18.
3. Epoxy meets UL94 V0 at 1/8".

N-channel TrenchMOS™ transistor
Logic level FET

PHP55N03LT, PHB55N03LT
PHD55N03LT

MOUNTING INSTRUCTIONS

Dimensions in mm

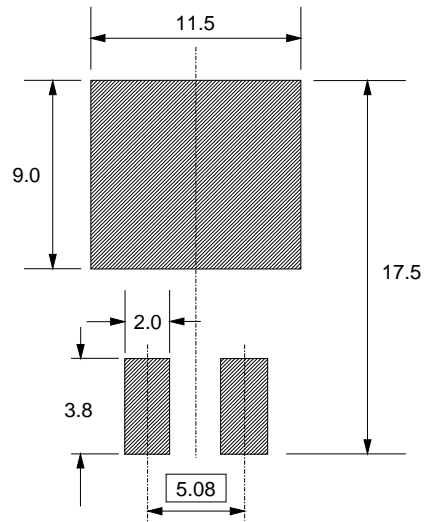


Fig.17. SOT404 : soldering pattern for surface mounting.

N-channel TrenchMOS™ transistor
Logic level FET

PHP55N03LT, PHB55N03LT
PHD55N03LT

MECHANICAL DATA

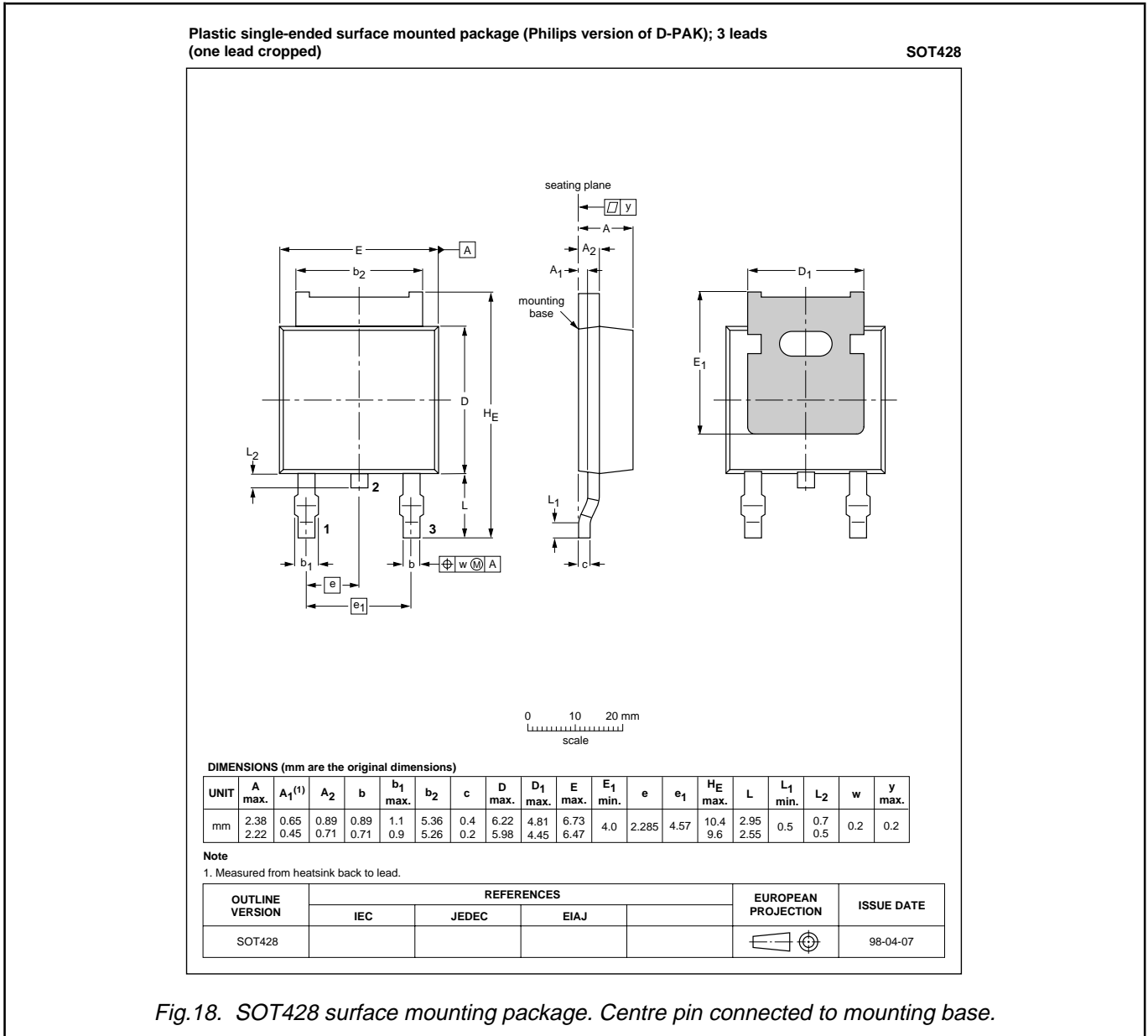


Fig.18. SOT428 surface mounting package. Centre pin connected to mounting base.

Notes

1. This product is supplied in anti-static packaging. The gate-source input must be protected against static discharge during transport or handling.
2. Refer to SMD Footprint Design and Soldering Guidelines, Data Handbook SC18.
3. Epoxy meets UL94 V0 at 1/8".

N-channel TrenchMOS™ transistor
Logic level FET

PHP55N03LT, PHB55N03LT
PHD55N03LT

MOUNTING INSTRUCTIONS

Dimensions in mm

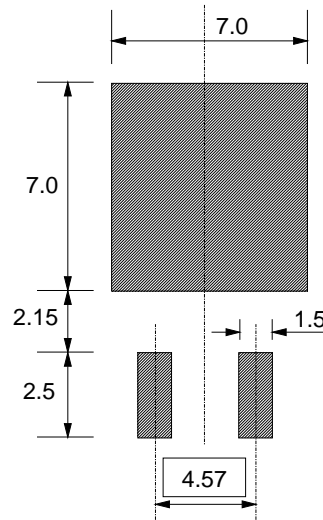


Fig.19. SOT428 : soldering pattern for surface mounting.

N-channel TrenchMOS™ transistor
Logic level FET

PHP55N03LT, PHB55N03LT
PHD55N03LT

DEFINITIONS

| | |
|--|---|
| Data sheet status | |
| Objective specification | This data sheet contains target or goal specifications for product development. |
| Preliminary specification | This data sheet contains preliminary data; supplementary data may be published later. |
| Product specification | This data sheet contains final product specifications. |
| Limiting values | |
| Limiting values are given in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of this specification is not implied. Exposure to limiting values for extended periods may affect device reliability. | |
| Application information | |
| Where application information is given, it is advisory and does not form part of the specification. | |
| © Philips Electronics N.V. 1999 | |
| All rights are reserved. Reproduction in whole or in part is prohibited without the prior written consent of the copyright owner. | |
| The information presented in this document does not form part of any quotation or contract, it is believed to be accurate and reliable and may be changed without notice. No liability will be accepted by the publisher for any consequence of its use. Publication thereof does not convey nor imply any license under patent or other industrial or intellectual property rights. | |

LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices or systems where malfunction of these products can be reasonably expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.