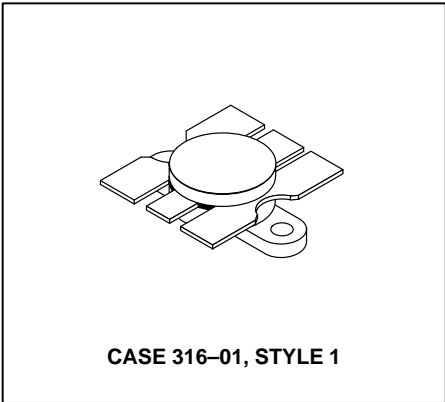


The RF Line

NPN Silicon

RF Power Transistor



Designed for 12.5 Volt UHF large-signal, common emitter, class-C amplifier applications in industrial and commercial FM equipment operating to 520 MHz.

- Specified 12.5 Volt, 512 MHz Characteristics
 - Output Power = 65 Watts
 - Minimum Gain = 4.15 dB
 - Minimum Efficiency = 50%
- Characterized with Series Equivalent Large-Signal Impedance Parameters from 400 to 520 MHz
- Built-In Matching Network for Broadband Operation
- Triple Ion Implanted for More Consistent Characteristics
- Implanted Emitter Ballast Resistors for Improved Ruggedness
- Silicon Nitride Passivated
- Capable of Surviving Load Mismatch Stress at all Phase Angles with 20:1 VSWR @ 15.5 Vdc and 2.0 dB Overdrive

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	16.5	Vdc
Collector-Emitter Voltage	V_{CES}	38	Vdc
Emitter-Base Voltage	V_{EBO}	4.0	Vdc
Collector Current — Continuous	I_C	15	Adc
Total Device Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C	P_D	175 1.0	Watts W/°C
Storage Temperature Range	T_{stg}	- 65 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.0	°C/W

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
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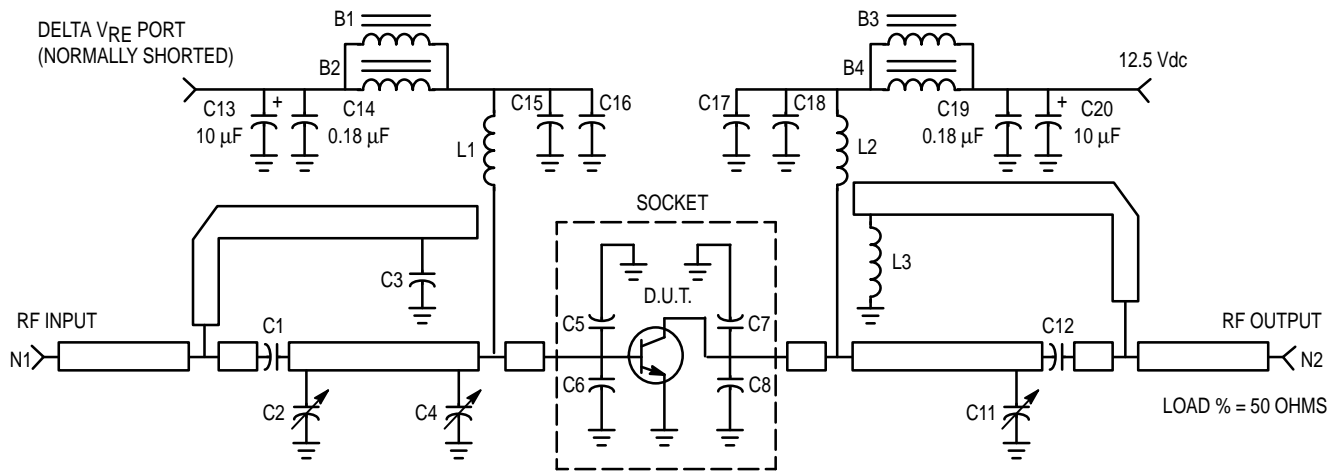
OFF CHARACTERISTICS

Collector-Emitter Breakdown Voltage ($I_C = 50 \text{ mAdc}$, $I_B = 0$)	$V_{(BR)CEO}$	16.5	29	—	Vdc
Collector-Emitter Breakdown Voltage ($I_C = 50 \text{ mAdc}$, $V_{BE} = 0$)	$V_{(BR)CES}$	38	45	—	Vdc
Emitter-Base Breakdown Voltage ($I_E = 10 \text{ mAdc}$, $I_C = 0$)	$V_{(BR)EBO}$	4.0	4.6	—	Vdc
Collector Cutoff Current ($V_{CE} = 15 \text{ Vdc}$, $V_{BE} = 0$, $T_C = 25^\circ\text{C}$)	I_{CES}	—	0.1	10	mAdc

(continued)

ELECTRICAL CHARACTERISTICS — continued ($T_C = 25^\circ\text{C}$ unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
ON CHARACTERISTICS					
DC Current Gain ($I_C = 10 \text{ Adc}$, $V_{CE} = 5.0 \text{ Vdc}$)	h_{FE}	40	85	120	—
DYNAMIC CHARACTERISTICS					
Output Capacitance ($V_{CB} = 12.5 \text{ Vdc}$, $I_E = 0$, $f = 1.0 \text{ MHz}$)	C_{ob}	—	170	220	pF
FUNCTIONAL TESTS (In Motorola Test Fixture. See Figure 1.)					
Output Power ($V_{CC} = 12.5 \text{ Vdc}$, $P_{in} = 25 \text{ W}$, $f = 470 \text{ \& } 512 \text{ MHz}$)	P_{out}	65	—	—	W
Collector Efficiency ($V_{CC} = 12.5 \text{ Vdc}$, $P_{out} = 65 \text{ W}$, $f = 470 \text{ \& } 512 \text{ MHz}$)	η	50	60	—	%
Output Mismatch Stress ($V_{CC} = 15.5 \text{ Vdc}$, $P_{in} = 32 \text{ W}$, $f = 512 \text{ MHz}$, VSWR 20:1, All Phase Angles)	ψ	No Degradation in Output Power			



- B1–B4 — Long Bead, Fair Rite (2743019446)
- C1 — 56 pF, Chip Capacitor, Murata Erie
- C2 — 1–20 pF Trimmer, Johanson–JMC 5501 PG26J200
- C3 — 39 pF, Chip Capacitor, Murata Erie
- C4 — 1–20 pF Trimmer, Johanson–JMC 5501
- C5 — 33 pF, Miniature Clamped Mica, SAHA
- C6 — 33 pF, Miniature Clamped Mica, SAHA
- C7 — 33 pF, Miniature Clamped Mica, SAHA
- C8 — 27 pF, Miniature Clamped Mica, SAHA
- C11 — 1–20 pF Trimmer, Johanson–JMC 5501 PG26J200
- C12 — 110 pF, Chip Capacitor, Murata Erie
- C13 — 10 μF , 50 V Electrolytic, Panasonic–ECEV1HV100R
- C14 — 0.18 μF Chip Capacitor
- C15 — 130 pF, Chip Capacitor, Murata Erie

- C16 — 130 pF, Chip Capacitor, Murata Erie
- C17 — 130 pF, Chip Capacitor, Murata Erie
- C18 — 130 pF, Chip Capacitor, Murata Erie
- C19 — 0.18 μF Chip Capacitor
- C20 — 10 μF , 50 V Electrolytic, Panasonic–ECEV1HV100R
- Board — 1/16" Glass Teflon, $\epsilon_r = 2.55$, Keene (GX–0600–55–22)
- L1, L2 — 5 Turns, 20 AWG, ID 0.126"
- L3 — 2 Turns, 26 AWG, ID 0.073"
- N1, N2 — Type N Flange, Omni Spectra (3052–1648–10)

- Murata Erie Chip Capacitors — GRH710COGxxxx100VBE
- SAHA Mini Clamped Mica Capacitors — 3HS0006–xx

Figure 1. 512 MHz Test Circuit

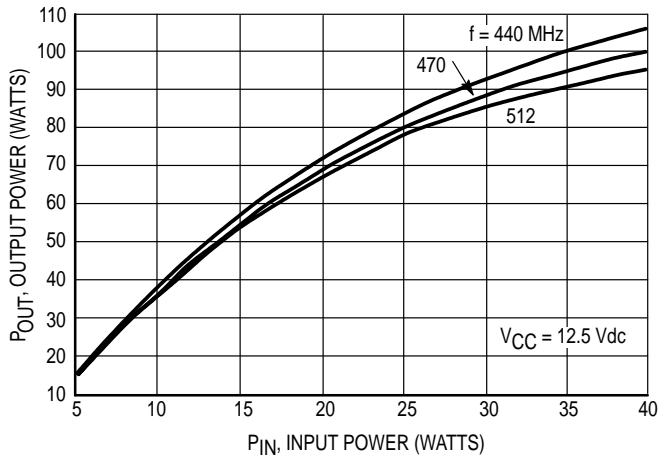


Figure 2. Output Power versus Input Power

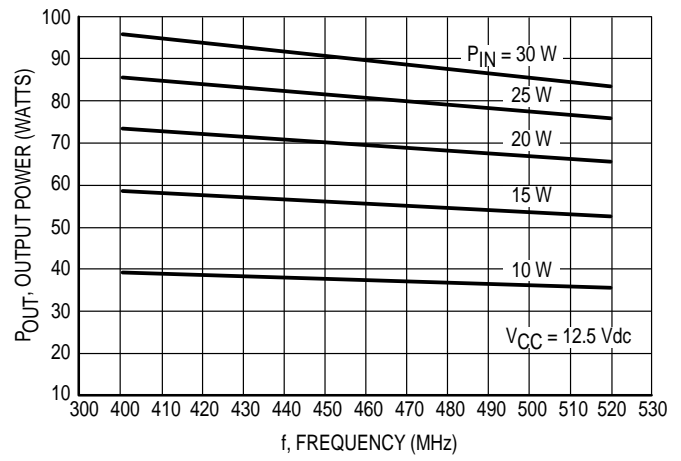


Figure 3. Output Power versus Frequency

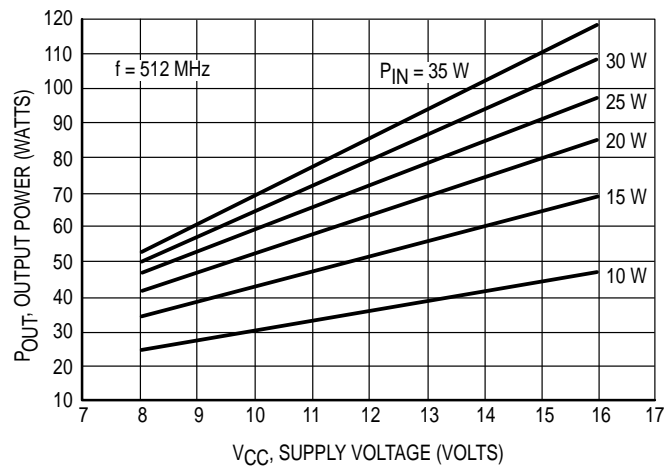
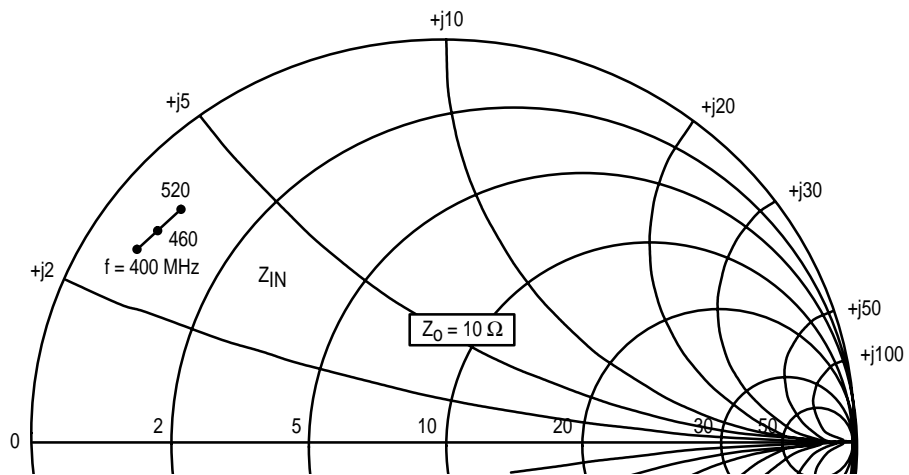
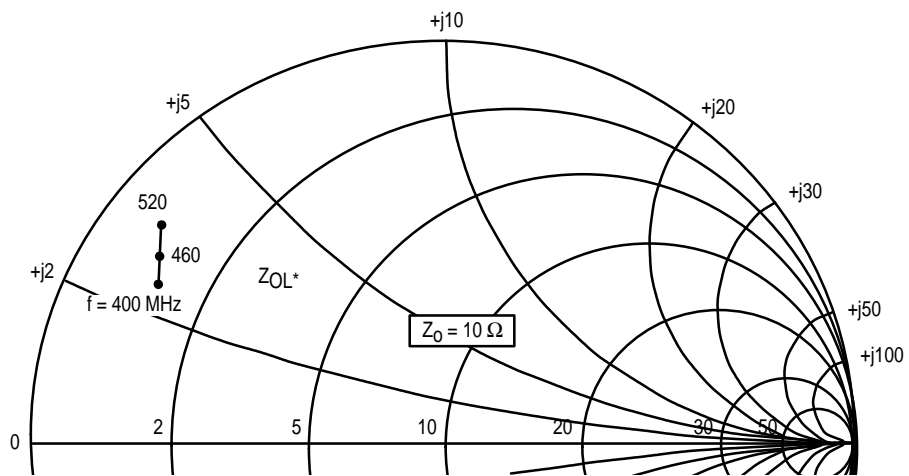


Figure 4. Output Power versus Supply Voltage



$V_{CC} = 12.5 \text{ V}$ $P_0 = 70 \text{ W}$

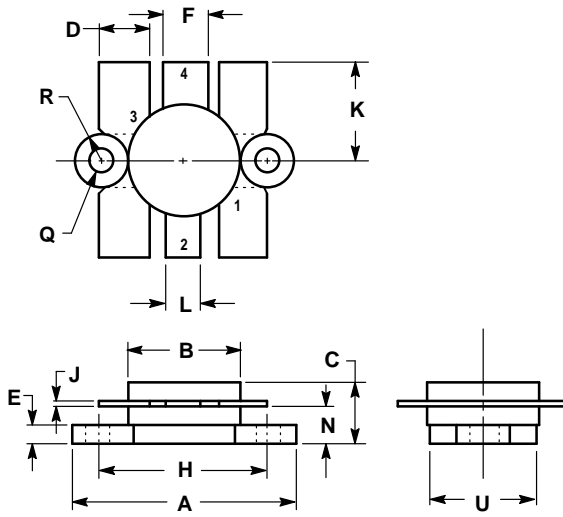
f MHz	Z_{IN} OHMS	Z_{OL}^* OHMS
400	$0.62 + j2.8$	$1.20 + j2.5$
440	$0.72 + j3.1$	$1.10 + j2.8$
480	$0.81 + j3.3$	$0.94 + j3.1$
520	$0.90 + j3.6$	$0.80 + j3.4$



Z_{OL}^* = Conjugate of optimum load impedance into which the device operates at a given output power, voltage and frequency.

Figure 5. Series Equivalent Input and Output Impedances

PACKAGE DIMENSIONS




NOTES:
1. FLANGE IS ISOLATED IN ALL STYLES.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	24.38	25.14	0.960	0.990
B	12.45	12.95	0.490	0.510
C	5.97	7.62	0.235	0.300
D	5.33	5.58	0.210	0.220
E	2.16	3.04	0.085	0.120
F	5.08	5.33	0.200	0.210
H	18.29	18.54	0.720	0.730
J	0.10	0.15	0.004	0.006
K	10.29	11.17	0.405	0.440
L	3.81	4.06	0.150	0.160
N	3.81	4.31	0.150	0.170
Q	2.92	3.30	0.115	0.130
R	3.05	3.30	0.120	0.130
U	11.94	12.57	0.470	0.495

STYLE 1:
PIN 1. EMITTER
2. COLLECTOR
3. EMITTER
4. BASE

**CASE 316-01
ISSUE D**

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