Advance Information
64K x 18 Bit BurstRAM
Synchronous Fast Static RAM
With Burst Counter and Self–Timed Write
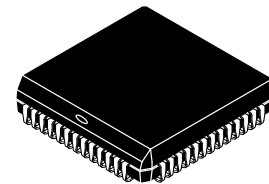
The MCM67H618B is a 1,179,648 bit synchronous fast static random access memory designed to provide a burstable, high–performance, secondary cache for the i486™ and Pentium™ microprocessors. It is organized as 65,536 words of 18 bits, fabricated with Motorola's high–performance silicon–gate BiCMOS technology. The device integrates input registers, a 2–bit counter, high speed SRAM, and high drive capability outputs onto a single monolithic circuit for reduced parts count implementation of cache data RAM applications. Synchronous design allows precise cycle control with the use of an external clock (K). BiCMOS circuitry reduces the overall power consumption of the integrated functions for greater reliability.

Addresses (A0 – A15), data inputs (D0 – D17), and all control signals except output enable (G) are clock (K) controlled through positive–edge–triggered noninverting registers.

Bursts can be initiated with either address status processor (ADSP) or address status cache controller (ADSC) input pins. Subsequent burst addresses can be generated internally by the MCM67H618B (burst sequence imitates that of the i486 and Pentium) and controlled by the burst address advance (ADV) input pin. The following pages provide more detailed information on burst controls.
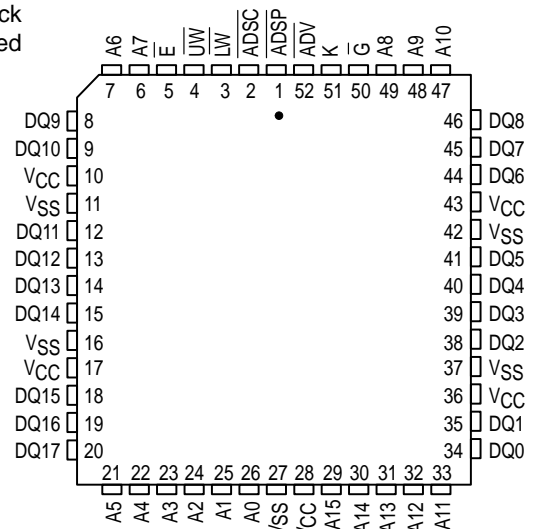
Write cycles are internally self–timed and are initiated by the rising edge of the clock (K) input. This feature eliminates complex off–chip write pulse generation and provides increased flexibility for incoming signals.

Dual write enables (LW and UW) are provided to allow individually writeable bytes. LW controls DQ0 – DQ8 (the lower bits), while UW controls DQ9 – DQ17 (the upper bits).

This device is ideally suited for systems that require wide data bus widths and cache memory. See Figure 2 for applications information.

- Single 5 V ± 5% Power Supply
- Fast Access Times: 9/10/12 ns Max
- Byte Writeable via Dual Write Enables
- Internal Input Registers (Address, Data, Control)
- Internally Self–Timed Write Cycle
- ADSP, ADSC, and ADV Burst Control Pins
- Asynchronous Output Enable Controlled Three–State Outputs
- Common Data Inputs and Data Outputs
- 3.3 V I/O Compatible
- High Board Density 52–Lead PLCC Package
- ADSP Disabled with Chip Enable (E) — Supports Address Pipelining

MCM67H618B

FN PACKAGE
PLASTIC
CASE 778–02

PIN ASSIGNMENT

Pin	Signal		Pin	Signal
8	DQ9		46	DQ8
9	DQ10		45	DQ7
10	V_{CC}		44	DQ6
11	V_{SS}		43	V_{CC}
12	DQ11		42	V_{SS}
13	DQ12		41	DQ5
14	DQ13		40	DQ4
15	DQ14		39	DQ3
16	V_{SS}		38	DQ2
17	V_{CC}		37	V_{SS}
18	DQ15		36	V_{CC}
19	DQ16		35	DQ1
20	DQ17		34	DQ0

Top pins (7–47): A6, A7, E, UW, LW, ADSC, ADSP, ADV, K, G, A8, A9, A10
Bottom pins (21–33): A5, A4, A3, A2, A1, A0, VSS, VCC, A15, A14, A13, A12, A11

| PIN NAMES	
A0 – A15	Address Inputs
K	Clock
ADV	Burst Address Advance
LW	Lower Byte Write Enable
UW	Upper Byte Write Enable
ADSC	Controller Address Status
ADSP	Processor Address Status
E	Chip Enable
G	Output Enable
DQ0 – DQ17	Data Input/Output
V_{CC}	+ 5 V Power Supply
V_{SS}	Ground

All power supply and ground pins must be connected for proper operation of the device.

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This document contains information on a new product. Specifications and information herein are subject to change without notice.

MOTOROLA

BLOCK DIAGRAM (See Note)
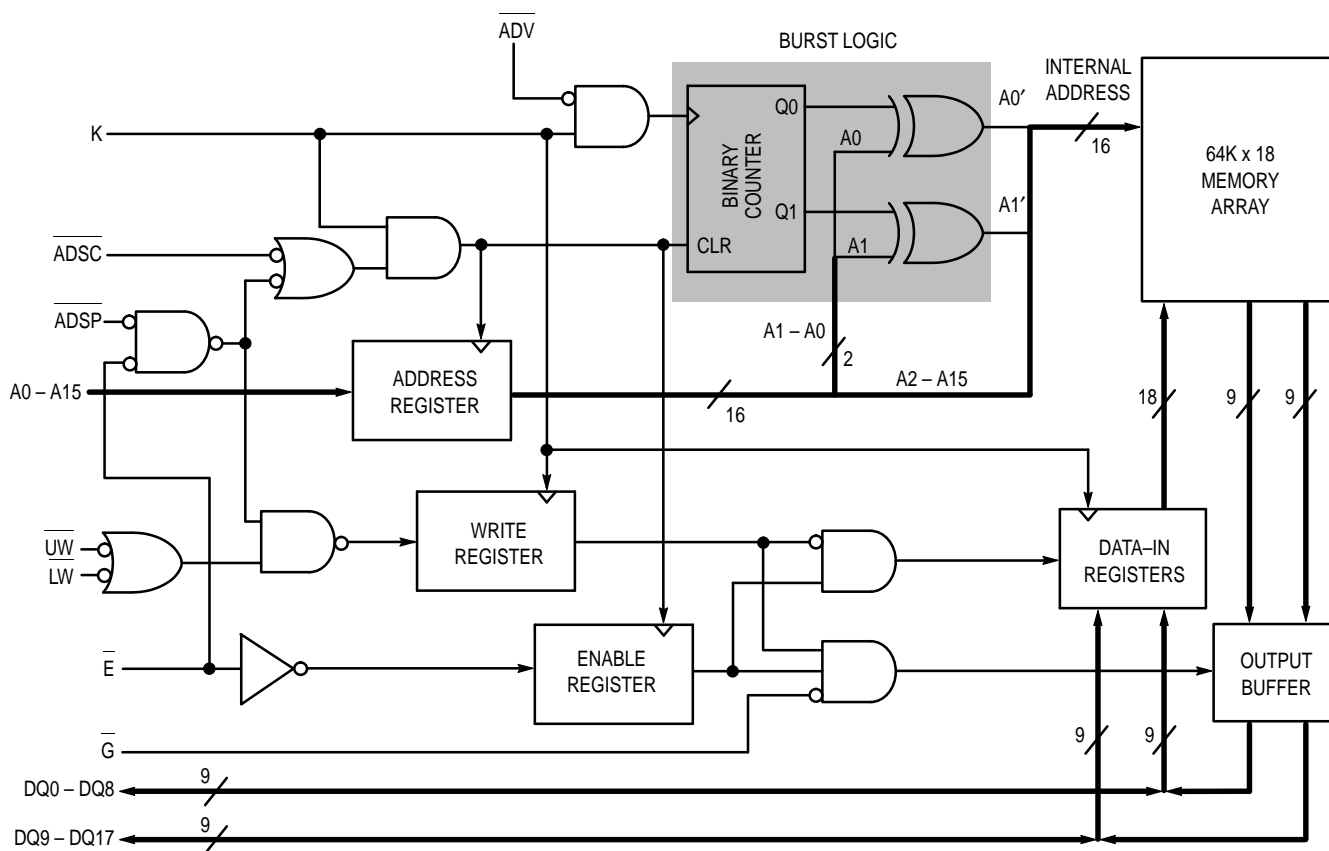
NOTE: All registers are positive–edge triggered. The ADSC or ADSP signals control the duration of the burst and the start of the next burst. When ADSP and E are sampled low, any ongoing burst is interrupted and a read (independent of W and ADSC) is performed using the new external address. Alternatively, an ADSP–initiated two cycle WRITE can be performed by asserting ADSP, E, and a valid address on the first cycle, then negating both ADSP and ADSC and asserting LW and/or UW with valid data on the second cycle (see Single Write Cycle in WRITE CYCLES timing diagram). Note that when E and ADSC are high, ADSP is ignored — the external address is not registered in this case.

When ADSC is sampled low (and ADSP is sampled high), any ongoing burst is interrupted and a read or write (dependent on W) is performed using the new external address. Chip enable (E) is sampled only when a new base address is loaded. After the first cycle of the burst, ADV controls subsequent burst cycles. When ADV is sampled low, the internal address is advanced prior to the operation. When ADV is sampled high, the internal address is not advanced, thus inserting a wait state into the burst sequence accesses. Upon completion of a burst, the address will wrap around to its initial state. See **BURST SEQUENCE TABLE**. Write refers to either or both byte write enables (LW, UW).

BURST SEQUENCE TABLE (See Note)

External Address	A15 – A2	A1	A0
1st Burst Address	A15 – A2	A1	A0
2nd Burst Address	A15 – A2	A1	A0
3rd Burst Address	A15 – A2	A1	A0

NOTE: The burst wraps around to its initial state upon completion.

SYNCHRONOUS TRUTH TABLE (See Notes 1, 2, and 3)

E	ADSP	ADSC	ADV	UW or LW	K	Address Used	Operation
H	X	L	X	X	L–H	N/A	Deselected
L	L	X	X	X	L–H	External Address	Read Cycle, Begin Burst
L	H	L	X	L	L–H	External Address	Write Cycle, Begin Burst
L	H	L	X	H	L–H	External Address	Read Cycle, Begin Burst
X	H	H	L	L	L–H	Next Address	Write Cycle, Continue Burst
X	H	H	L	H	L–H	Next Address	Read Cycle, Continue Burst
X	H	H	H	L	L–H	Current Address	Write Cycle, Suspend Burst
X	H	H	H	H	L–H	Current Address	Read Cycle, Suspend Burst
H	X	H	L	L	L–H	Next Address	Write Cycle, Continue Burst
H	X	H	L	H	L–H	Next Address	Read Cycle, Continue Burst
H	X	H	H	L	L–H	Current Address	Write Cycle, Suspend Burst
H	X	H	H	H	L–H	Current Address	Read Cycle, Suspend Burst

NOTES:
1. X means Don't Care.
2. All inputs except G must meet setup and hold times for the low–to–high transition of clock (K).
3. Wait states are inserted by suspending burst.

ASYNCHRONOUS TRUTH TABLE (See Notes 1 and 2)

Operation	G	I/O Status
Read	L	Data Out
Read	H	High–Z
Write	X	High–Z — Data In
Deselected	X	High–Z

NOTES:
1. X means Don't Care.
2. For a write operation following a read operation, $\overline{G}$ must be high before the input data required setup time and held high through the input data hold time.

ABSOLUTE MAXIMUM RATINGS (Voltages Referenced to V_{SS} = 0 V)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	– 0.5 to + 7.0	V
Voltage Relative to V_{SS} for Any Pin Except V_{CC}	V_{in}, V_{out}	– 0.5 to V_{CC} + 0.5	V
Output Current (per I/O)	I_{out}	± 30	mA
Power Dissipation	P_D	1.6	W
Temperature Under Bias	T_{bias}	– 10 to + 85	°C
Ambient Temperature	T_A	0 to +70	°C
Storage Temperature	T_{stg}	– 55 to + 125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high–impedance circuit.

This BiCMOS memory circuit has been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established.

This device contains circuitry that will ensure the output devices are in High–Z at power up.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 5%, T_A = 0 to + 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS (Voltages Referenced to V_{SS} = 0 V)

Parameter	Symbol	Min	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.75	5.25	V
Input High Voltage	V_{IH}	2.2	V_{CC} + 0.3**	V
Input Low Voltage	V_{IL}	– 0.5*	0.8	V

* V_{IL} (min) = – 0.5 V dc; V_{IL} (min) = – 2.0 V ac (pulse width ≤ 20.0 ns) for I ≤ 20.0 mA.
** V_{IH} (max) = V_{CC} + 0.3 V dc; V_{IH} (max) = V_{CC} + 2.0 V ac (pulse width ≤ 20.0 ns) for I ≤ 20.0 mA.

DC CHARACTERISTICS AND SUPPLY CURRENTS

Parameter	Symbol	Min	Max	Unit
Input Leakage Current (All Inputs, V_{in} = 0 to V_{CC})	$I_{lkg(I)}$	—	± 1.0	µA
Output Leakage Current (G = V_{IH})	$I_{lkg(O)}$	—	± 1.0	µA
AC Supply Current (Device Selected, All Outputs Open, Freq = Max) MCM67H618B–9 MCM67H618B–10 MCM67H618B–12	I_{CCA}	—	TBD	mA
CMOS Standby Supply Current (Device Deselected, Freq = 0, V_{CC} = Max, All Inputs Static at CMOS Levels V_{in} ≤ V_{SS} + 0.2 V or ≥ V_{CC} – 0.2 V)	I_{SB2}	—	TBD	mA
Clock Running (Device Deselected, Freq = Max, V_{CC} = Max, All Inputs Toggling at CMOS Levels V_{in} ≤ V_{SS} + 0.2 V or ≥ V_{CC} – 0.2 V)	I_{SB4}	—	TBD	mA
Output Low Voltage (I_{OL} = + 8.0 mA)	V_{OL}	—	0.4	V
Output High Voltage (I_{OH} = – 4.0 mA)	V_{OH}	2.4	3.3	V

NOTE: Good decoupling of the local power supply should always be used. DC characteristics are guaranteed for all possible i486 and Pentium bus cycles.

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Parameter	Symbol	Typ	Max	Unit
Input Capacitance	C_{in}	4	5	pF
Input/Output Capacitance	$C_{I/O}$	6	8	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V $\pm$ 5%, T_A = 0 to + 70°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level . . . . 1.5 V
Input Pulse Levels . . . . 0 to 3.0 V
Input Rise/Fall Time . . . . 3 ns

Output Timing Reference Level . . . . 1.5 V
Output Load . . . . See Figure 1 Unless Otherwise Noted

READ/WRITE CYCLE TIMING (See Notes 1, 2, 3, and 4)

Parameter	Symbol	MCM67H618B–9 Min	MCM67H618B–9 Max	MCM67H618B–10 Min	MCM67H618B–10 Max	MCM67H618B–12 Min	MCM67H618B–12 Max	Unit	Notes
Cycle Time	t_{KHKH}	15	—	16.6	—	20	—	ns	
Clock Access Time	t_{KHQV}	—	9	—	10	—	12	ns	5
Output Enable to Output Valid	t_{GLQV}	—	5	—	5	—	6	ns	
Clock High to Output Active	t_{KHQX1}	6	—	6	—	6	—	ns	
Clock High to Output Change	t_{KHQX2}	3	—	3	—	3	—	ns	
Output Enable to Output Active	t_{GLQX}	0	—	0	—	0	—	ns	
Output Disable to Q High–Z	t_{GHQZ}	—	6	—	7	—	7	ns	6
Clock High to Q High–Z	t_{KHQZ}	3	6	3	7	3	7	ns	
Clock High Pulse Width	t_{KHKL}	5	—	5	—	6	—	ns	
Clock Low Pulse Width	t_{KLKH}	5	—	5	—	6	—	ns	
Setup Times: Address, Address Status, Data In, Write, Address Advance, Chip Enable	t_{AVKH}, t_{ADSVKH}, t_{DVKH}, t_{WVKH}, t_{ADVVKH}, t_{EVKH}	2.5	—	2.5	—	2.5	—	ns	7
Hold Times: Address, Address Status, Data In, Write, Address Advance, Chip Enable	t_{KHAX}, t_{KHADSX}, t_{KHDX}, t_{KHWX}, t_{KHADVX}, t_{KHEX}	0.5	—	0.5	—	0.5	—	ns	7

NOTES:
1. In setup and hold times, W (write) refers to either one or both byte write enables LW and UW.
2. A read cycle is defined by UW and LW high or ADSP low for the setup and hold times. A write cycle is defined by LW or UW low and ADSP high for the setup and hold times.
3. All read and write cycle timings are referenced from K or G.
4. G is a don't care when UW or LW is sampled low.
5. Maximum access times are guaranteed for all possible i486 and Pentium external bus cycles.
6. Transition is measured $\pm$ 500 mV from steady–state voltage. This parameter is sampled rather than 100% tested. At any given voltage and temperature, t_{KHQZ} max is less than t_{KHQZ1} min for a given device and from device to device.
7. This is a synchronous device. All addresses must meet the specified setup and hold times for *ALL* rising edges of K whenever ADSP or ADSC is low, and the chip is selected. All other synchronous inputs must meet the specified setup and hold times for *ALL* rising edges of K when the chip is enabled. Chip enable must be asserted at each rising edge of clock for the device (when ADSC is low) to remain enabled.
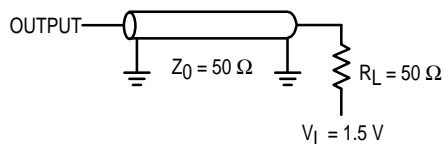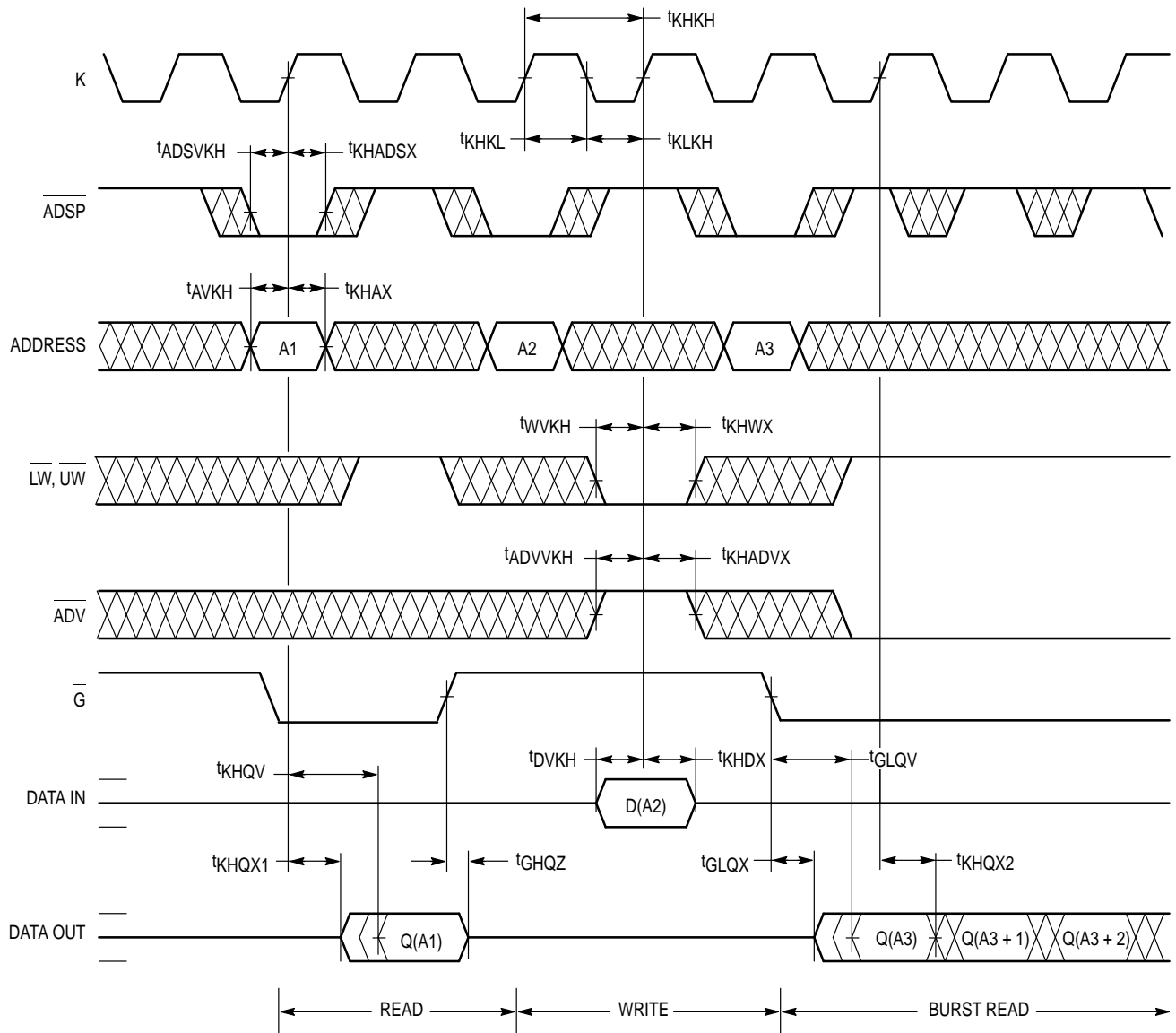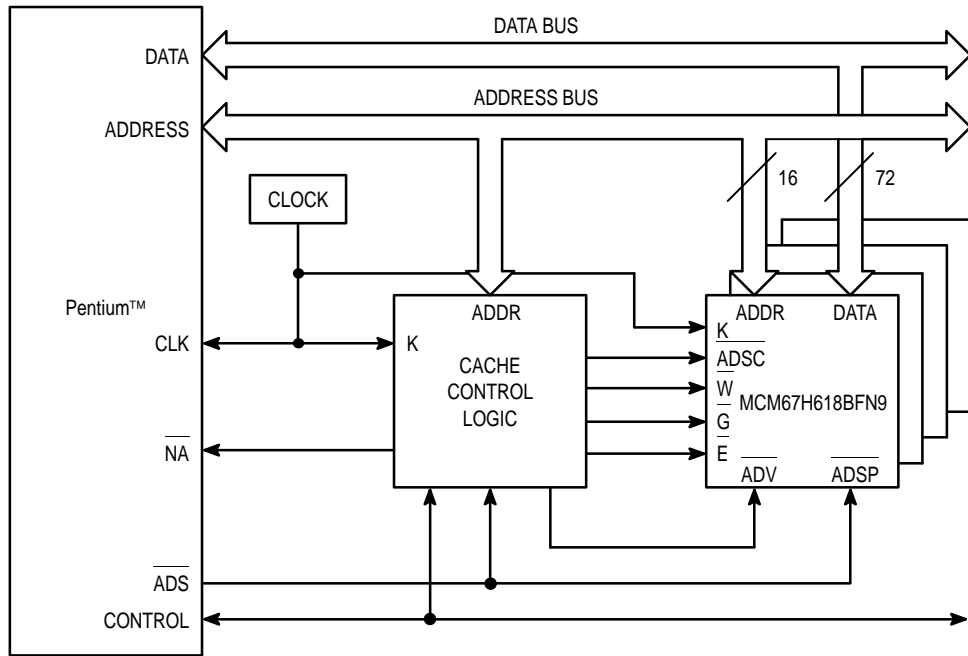

OUTPUT — $Z_0 = 50\ \Omega$ — $R_L = 50\ \Omega$ — $V_L = 1.5$ V

Figure 1. Test Load

READ CYCLES

NOTE: Q(A2) represents the first output data from the base address A2; Q(A2 + 1) represents the next output data in the burst sequence with A2 as the base address.

WRITE CYCLES

The timing diagram shows the following signals (top to bottom): K, $\overline{ADSP}$, $\overline{ADSC}$, ADDRESS, $\overline{LW}$, $\overline{UW}$, $\overline{E}$, $\overline{ADV}$, $\overline{G}$, DATA IN, DATA OUT.

Timing parameters labeled: t_{KHKH}, t_{KHKL}, t_{KLKH}, t_{KHADSX}, t_{ADSVKH}, t_{KHADSX}, t_{AVKH}, t_{KHAX}, t_{KHWX}, t_{WVKH}, t_{EVKH}, t_{KHEX}, $t_{KHADV/X}$, t_{ADVVKH}, t_{GHQZ}, t_{DVKH}, t_{KHDX}.

Annotations: "$\overline{ADSC}$ STARTS NEW BURST", "$\overline{W}$ IS IGNORED FOR FIRST CYCLE WHEN $\overline{ADSP}$ INITIATES BURST", "$\overline{ADV}$ SUSPENDS BURST".

Address labels: A1, A2, A3. Data labels: D(A1), D(A2), D(A2 + 1), D(A2 + 2), D(A2 + 3), D(A3), D(A3 + 1), D(A3 + 2). Data out: Q(An − 1), Q(An).

Cycle labels at bottom: BURST READ, SINGLE WRITE, BURST WRITE (WITH A SUSPENDED CYCLE), NEW BURST WRITE.

COMBINATION READ/WRITE CYCLE ($\overline{E}$ Low, $\overline{ADSC}$ High)

APPLICATION EXAMPLE

512K Byte Burstable, Secondary Cache
Using Four MCM67H618BFN9s with a 66 MHz Pentium

Figure 2.

ORDERING INFORMATION
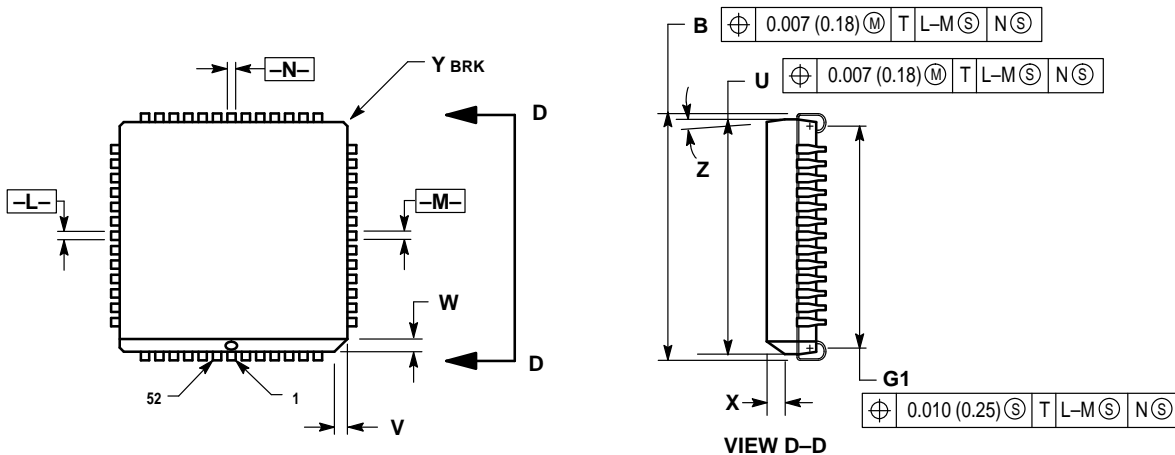### (Order by Full Part Number)

<u>**MCM**</u>   <u>**67H618B**</u>   <u>**XX**</u>   <u>**XX**</u>

Motorola Memory Prefix ————————┘   │   │   └———— Speed (9 = 9 ns, 10 = 10 ns, 12 = 12 ns)

Part Number ————————————————————————┘   └———————————— Package (FN = PLCC)
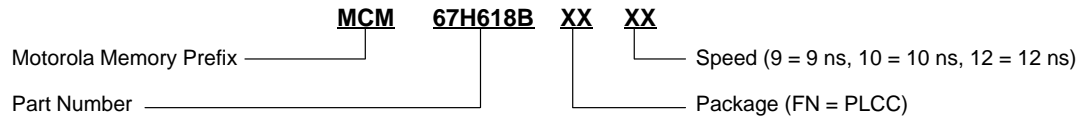
Full Part Numbers — MCM67H618BFN9   MCM67H618BFN10   MCM67H618BFN12

PACKAGE DIMENSIONS

FN PACKAGE
52–LEAD PLCC
CASE 778–02

| B | ⊕ | 0.007 (0.18) Ⓜ | T | L–M Ⓢ | N Ⓢ |

| U | ⊕ | 0.007 (0.18) Ⓜ | T | L–M Ⓢ | N Ⓢ |

| ⊕ | 0.010 (0.25) Ⓢ | T | L–M Ⓢ | N Ⓢ |

VIEW D–D

| A | ⊕ | 0.007 (0.18) Ⓜ | T | L–M Ⓢ | N Ⓢ |

| R | ⊕ | 0.007 (0.18) Ⓜ | T | L–M Ⓢ | N Ⓢ |

| ⬠ | 0.004 (0.100) |

–T– SEATING PLANE

VIEW S

| ⊕ | 0.010 (0.25) Ⓢ | T | L–M Ⓢ | N Ⓢ |

| H | ⊕ | 0.007 (0.18) Ⓜ | T | L–M Ⓢ | N Ⓢ |

| F | ⊕ | 0.007 (0.18) Ⓜ | T | L–M Ⓢ | N Ⓢ |

VIEW S
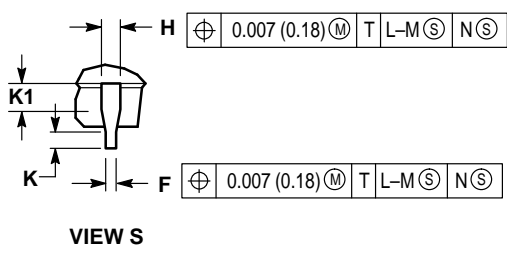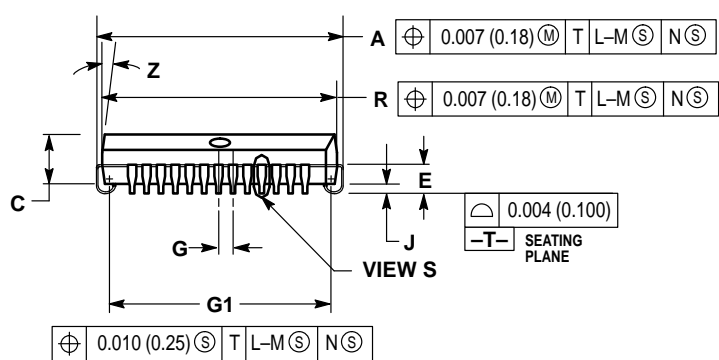
NOTES:
1. DATUMS –L–, –M–, AND –N– DETERMINED WHERE TOP OF LEAD SHOULDER EXITS PLASTIC BODY AT MOLD PARTING LINE.
2. DIMENSION G1, TRUE POSITION TO BE MEASURED AT DATUM –T–, SEATING PLANE.
3. DIMENSIONS R AND U DO NOT INCLUDE MOLD FLASH. ALLOWABLE MOLD FLASH IS 0.010 (0.250) PER SIDE.
4. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
5. CONTROLLING DIMENSION: INCH.
6. THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM BY UP TO 0.012 (0.300). DIMENSIONS R AND U ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, TIE BAR BURRS, GATE BURRS AND INTERLEAD FLASH, BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.
7. DIMENSION H DOES NOT INCLUDE DAMBAR PROTRUSION OR INTRUSION. THE DAMBAR PROTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE GREATER THAN 0.037 (0.940). THE DAMBAR INTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE SMALLER THAN 0.025 (0.635).

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	0.785	0.795	19.94	20.19
B	0.785	0.795	19.94	20.19
C	0.165	0.180	4.20	4.57
E	0.090	0.110	2.29	2.79
F	0.013	0.019	0.33	0.48
G	0.050 BSC		1.27 BSC	
H	0.026	0.032	0.66	0.81
J	0.020	—	0.51	—
K	0.025	—	0.64	—
R	0.750	0.756	19.05	19.20
U	0.750	0.756	19.05	19.20
V	0.042	0.048	1.07	1.21
W	0.042	0.048	1.07	1.21
X	0.042	0.056	1.07	1.42
Y	—	0.020	—	0.50
Z	2 °	10 °	2 °	10 °
G1	0.710	0.730	18.04	18.54
K1	0.040	—	1.02	—

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                                              – US & Canada ONLY 1–800–774–1848
INTERNET : http://motorola.com/sps

JAPAN: Nippon Motorola Ltd.; SPD, Strategic Planning Office; 4–32–1,
Nishi–Gotanda; Shinagawa–ku, Tokyo 141, Japan. 81–3–5487–8488

ASIA/PACIFIC: Motorola Semiconductors H.K. Ltd.; 8B Tai Ping Industrial Park,
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