MOTOROLA

Chip Errata
DSP56301 Digital Signal Processor
Mask: 2K30A

General remark: In order to prevent the use of instructions or sequences of instructions that do not operate correctly, we encourage you to use the "lint563" program to identify such cases and use alternative sequences of instructions. This program is available as part of the Motorola DSP Tools CLAS package.

Silicon Errata

Errata Number	Errata Description	Applies to Mask
ES133	Description (added 8/16/2001): Some K30A devices shipped under an XC part number are subject to a problem if operated in DMA mode 5. The problem occurs if two consecutive host commands are sent to the DSP. The second host command is received, the corresponding answer message is composed, and the DMA channel is set up correctly to transmit the message to the host. However, the message is never sent. The host port status register shows a host transmit data request (bit HTRQ in HSTR is set.) DTDn is never set, indicating there has been no terminated transfer. Sequences of: 1. data, 2. host command to terminate the transfer, and 3. acknowledgement from the host work properly and can be repeated as often as needed. If a second host command is sent to the DSP, without first sending data, the DMA channel locks up. This problem has proven to be low level to date, occurring at a rate of about 350 ppm. The product's performance regarding this issue does not drift over time; that is, it is not a reliability risk. The problem can also be manifested in other modes when more than one DMA channel is operating, with two or more channels moving data while one is servicing the PCI FIFO. In this case, the channel servicing the PCI FIFO stalls and the PCI bus enters an endless state of retries.	2K30A

Documentation Errata

Errata Number	Document Update	Applies to Mask
ED1	Description (revised 11/9/98): XY memory data move does not work properly if the X-memory move destination is internal I/O and the Y-memory move source is a register used as destination in the previous adjacent move from non Y-memory OR the Y-memory move destination is a register used as source in the next adjacent move to non Y-memory. Here are examples of the two cases (where x:(r1) is a peripheral): Example 1: `move #$12,y0` `move x0,x:(r7) y0,y:(r3) (while x:(r7) is a peripheral).` Example 2: `mac x1,y0,a x1,x:(r1)+ y:(r6)+,y0` `move y0,y1` This is not a bug, but a documentation update. Any of the following alternatives can be used: a. Separate these two consecutive moves by any other instruction. b. Split XY Data Move to two moves.	2K30A
ED2	Description (added 10/09/1997): $\overline{BL}$ pin timings T198 and T199 in the Data Sheet are changed, improving the arbitration latency: T198 is 5 ns (max), T199 is 0 ns (min). This is not a bug, but a documentation update.	2K30A
ED3	Description (added 10/09/1997): A one-word conditional branch instruction at LA-1 is not allowed. This is not a bug, but a documentation update.	2K30A

Errata Number	Document Update	Applies to Mask
ED4	Description (added 10/09/1997): The following instructions should not start at address LA: MOVE to/from Program space {MOVEM, MOVEP (only the P space options)} This is not a bug but a documentation update (Appendix B, DSP56300 Family Manual).	2K30A
ED6	Description (added 4/13/98): When the $\overline{\text{HIRQ}}$ pin is used in pulse mode (HIRH=0 in DCTR), the LT[7:0] value (in CLAT) should not be zero. This is not a bug but a documentation update.	2K30A
ED7	Description (added 1/27/98): When activity passes from one DMA channel to another and the DMA interface accesses external memory (which requires one or more wait states), the DACT and DCH status bits in the DMA Status Register (DSTR) may indicate improper activity status for DMA Channel 0 (DACT = 1 and DCH[2:0] = 000). Workaround: None. **Pertains to:** DSP56300 Family Manual, Sections 8.1.6.3 and 8.1.6.4	2K30A
ED8	Description (added 10/09/1997): The timing for HSAK is no longer qualified by the data strobe. The new timing numbers are: a. **T318**—HSAK assertion from HA0–HA10 and HAEN valid is 30.0 ns maximum. b. **T319**—HSAK assertion hold from HA0-HA10 and NAEN not valid is 2.0 ns minimum. This is not a bug, but a documentation update of a specification change.	2K30A

Errata Number	Document Update	Applies to Mask
ED9	Description (added 1/27/98): When the SCI is configured in Synchronous mode, internal clock, and all the SCI pins are enabled simultaneously, an extra pulse of 1 DSP clock length is provided on the SCLK pin. Workaround: a. Enable an SCI pin other than SCLK. b. In the next instruction, enable the remaining SCI pins, including the SCLK pin. **Pertains to:** UM, SCI Chapter (Use the 302 UM as your reference, Section 8.4.2, "SCI Initialization")	2K30A
ED10	Description (added 5/13/98): The HI32 may operate improperly in PCI mode when the TWSD bit is set in the HCTR register. Workaround: Do not set the TWSD bit in the HCTR register; this bit is reserved. This is a documentation change.	2K30A
ED12	Description (added 5/13/98): When the HI32 is in PCI mode, the HTF control bits affect the address insertion (the IAE bit is set in the DPCR register) in the same way they affect the transferred data. Address as appears on the PCI bus: $12345678 **HTF[1:0]** — **Inserted Address** 00 — $005678, $001234 01 — $345678 10 — $345678 11 — $123456 Workaround: This is a documentation update.	2K30A

Errata Number	Document Update	Applies to Mask
ED13	Description (added 5/15/98): When the HI32 is in PCI mode, the Insert Address Enable control bit (IAE=1) can be set only with the Receive Buffer Lock Enable control bit set (RBLE=1 in the DPCR register.)	2K30A
ED15	Description (added 7/21/98): The DRAM Control Register (DCR) should not be changed while refresh is enabled. If refresh is enabled only a write operation that disables refresh is allowed. Workaround: First disable refresh by clearing the BREN bit, than change other bits in the DCR register, and finally enable refresh by setting the BREN bit.	2K30A
ED17	Description (added 9/28/98): In all DSP563xx technical datasheets, a note is to be added under "AC Electrical Characteristics" that although the minimum value for "Frequency of Extal" is 0MHz, the device AC test conditions are 15MHz and rated speed. Workaround: N/A	2K30A
ED18	Description (added 11/2/98): The PCI host must not change the values of the HBE[3:0] bits during PCI read transactions from the HI32 as a PCI target.	2K30A
ED19	Description (added 11/9/98): To guarantee the proper HI32 operation, the DMA should service the HI32 under the following restrictions: • Two DMA channels should not service the DRXR FIFO if master and slave data is mixed there. • The DMA data transfers should not be concurrent with the 56300 Core data transfers to/from the same HI32 data FIFO.	2K30A

Errata Number	Document Update	Applies to Mask
ED20	Description (added 11/24/98): In the Technical Datasheet Voh-TTL should be listed at 2.4 Volts, not as: `TTL = Vcc-0.4` Workaround: This is a documentation update.	2K30A
ED21	Description (added 11/24/98): In the Technical Datasheet Iol should be listed as 1.6 mA, not as 3.0 mA. Workaround: This is a documentation update.	2K30A
ED24	Description (added 11/24/98): The technical datasheet supplies a maximum value for internal supply current in Normal, Wait, and Stop modes. These values will be removed because we will specify only a "Typical" current. Workaround: This is a documentation update.	2K30A

Errata Number	Document Update	Applies to Mask
ED25	Description (added 12/16/98): Current definition: HDTC is set if SRRQ and MRRQ are cleared (i.e. the host-to-DSP data path is emptied by DSP56300 core reads) under one of the following conditions: • a non-exclusive PCI write transaction to the HTXR terminates or completes • $\overline{\text{HLOCK}}$ is negated after the completion of an exclusive write access to the HTXR • the HI32 initiates a read transaction. The HI32 disconnects (retry or disconnect-C) forthcoming write accesses to the HTXR as long as HDTC is set. New definition: HDTC is set if SRRQ and MRRQ are cleared (i.e. the host-to-DSP data path is emptied by DSP56300 Core reads) under one of the following conditions: • a non-exclusive PCI write transaction to the HTXR terminates or completes • $\overline{\text{HLOCK}}$ is negated after the completion of an exclusive write access to the HTXR. The HI32 disconnects (retry or disconnect-C) forthcoming write accesses to the HTXR as long as HDTC is set. Note: The HDTC bit is not set after a read transaction initiated by the HI32 as a PCI master. Workaround: NTR	2K30A

Errata Number	Document Update	Applies to Mask
ED26	Description (added 1/6/99): The specification DMA Chapter is wrong. "Due to the DSP56300 Core pipeline, after DE bit in DCRx is set, the corresponding DTDx bit in DSTR will be cleared only after two instruction cycles." Should be replaced with: "Due to the DSP56300 Core pipeline, after DE bit in DCRx is set, the corresponding DTDx bit in DSTR will be cleared only after three instruction cycles."	2K30A
ED27	Description (added 1/12/99): The PBGA mechanical package drawing in the 56301 and 56305 data sheets is incorrect. The figure numbers of the incorrect drawings are Figure 3-6 for the 56301 and Figure 3-3 for the 56305. The only incorrect part is the bottom view above the label "VIEW M-M." This view erroneously shows the number of pins on the package to be 256, but the actual number of pins is 252. In the drawing, the four balls in the corners should not appear. **Pertains to:** Data sheet. To get the art, call Gordon Fowkes and ask.	2K30A

Errata Number	Document Update	Applies to Mask
ED28	Description (added 1/7/1997; identified as Documentation Errata 2/1/99): When two consecutive LAs have a conditional branch instruction at LA-1 of the internal loop, the part does not operate properly. For example, the following sequence may generate incorrect results: `DO #5, LABEL1` `NOP` `DO #4, LABEL2` `NOP` `MOVE (R0) +` `BSCC _DEST ; conditional branch at LA-1 of internal loop` `NOP ; internal LA LABEL2` `NOP ; external LA LABEL1` `NOP` `NOP` `_DEST NOP` `NOP` `RTS` Workaround: Put an additional NOP between LABEL2 and LABEL1.	2K30A
ED29	Description (added 9/12/1997; identified as a Documentation errata 2/1/99): When the ESSI transmits data with the CRA Word Length Control bits (WL[2:0]) = 100, the ESSI is designed to duplicate the last bit of the 24-bit transmission eight times to fill the 32-bit shifter. Instead, after shifting the 24-bit word correctly, eight 0s are being shifted. Workaround: None at this time.	2K30A

Errata Number	Document Update	Applies to Mask
ED30	Description (added 9/12/1997; identified as a Documentation errata 2/1/99): When the ESSI transmits data in the On-Demand mode (i.e., MOD = 1 in CRB and DC[4:0] = $00000 in CRA) with WL[2:0] = 100, the transmission does not work properly. Workaround: To ensure correct operation, do not use the On-Demand mode with the WL[2:0] = 100 32-bit Word-Length mode.	2K30A
ED31	Description (added 9/12/1997; modified 9/15/1997; identified as a Documentation errata 2/1/99): Programming the ESSI to use an internal frame sync (i.e., SCD2 = 1 in CRB) causes the SC2 and SC1 signals to be programmed as outputs. If however, the corresponding multiplexed pins are programmed by the Port Control Register (PCR) to be GPIOs, then the GPIO Port Direction Register (PRR) chooses their direction, but this causes the ESSI to use an external frame sync if GPI is selected. **Note:** This errata and workaround apply to both ESSI0 and ESSI1. Workaround: To assure correct operation, either program the GPIO pins as outputs or configure the pins in the PCR as ESSI signals. **Note:** The default selection for these signals after reset is GPI.	2K30A
ED32	Description (added 11/9/98; identified as a Documentation errata 2/1/99): When returning from a long interrupt (by RTI instruction), and the first instruction after the RTI is a move to a DALU register (A, B, X, Y), the move may not be correct, if the 16-bit arithmetic mode bit (bit 17 of SR) is changed due to the restoring of SR after RTI. Workaround: Replace the RTI with the following sequence: `movec ssl,sr` `nop` `rti`	2K30A

Errata Number	Document Update	Applies to Mask
ED33	Description (added 12/16/98; identified as a Documentation errata 2/1/99): When Stack Extension mode is enabled, a use of the instructions BRKcc or ENDDO inside do loops might cause an improper operation. If the loop is non nested and has no nested loop inside it, the erratais relevant only if LA or LC values are being used outside the loop. Workaround: If Stack Extension is used, emulate the BRKcc or ENDDO as in the following examples. We split between two cases, finite loops and do forever loops. `1) Finite DO loops (i.e. not DO FOREVER loops)` `==========` `BRKcc` `Original code:` `do #N,label1` `.....` `.....` `do #M,label2` `.....` `.....` `BRKcc` `.....` `.....` `label2` `.....` `.....` `label1` Will be replaced by: `do #N, label1` `.....` `.....` `do #M, label2` `.....` `.....` `Jcc fix_brk_routine` `.....` `.....`	2K30A

Errata Number	Document Update	Applies to Mask
ED33 cont.	nop_before_label2 nop ; This instruction must be NOP. label2 .... label1 .... fix_brk_routine move #1,lc jmp nop_before_label2 ENDDO ------ Original code: do #M,label1 .... do #N,label2 .... ENDDO .... label2 .... label1 Will be replaced by: do #M, label1 .... do #N, label2 .... JMP fix_enddo_routine	

Errata Number	Document Update	Applies to Mask
ED33 cont.	nop_after_jmp NOP ; This instruction must be NOP. .... label2 .... label1 .... fix_enddo_routine move #1,lc move #nop_after_jmp,la jmp nop_after_jmp 2) DO FOREVER loops ========== BRKcc ----- Original code: do #M,label1 .... do forever,label2 .... BRKcc .... label2 .... label1	

Errata Number	Document Update	Applies to Mask
ED33 cont.	Will be replaced by: `do #M,label1` `.....` `.....` `do forever,label2` `.....` `.....` `JScc fix_brk_forever_routine ; <---` `note: JScc and not Jcc` `.....` `.....` `nop_before_label2` `nop ; This instruction must be NOP.` `label2` `.....` `.....` `label1` `....` `....` `fix_brk_forever_routine` `move ssh,x:<..> ; <..> is some reserved not used address (for temporary data)` `move #nop_before_label2,ssh` `bclr #16,ssl ;` `move #1,lc` `rti ; <---- note: "rti" and not "rts" !` `ENDDO` `------` `Original code:` `do #M,label1` `.....` `.....`	

Errata Number	Document Update	Applies to Mask
ED33 cont.	do forever,label2 .... ENDDO .... label2 .... label1 Will be replaced by: do #M,label1 .... do forever,label2 .... JSR fix_enddo_routine ; <--- note: JSR and not JMP nop_after_jmp NOP ; This instruction should be NOP .... label2 .... label1 .... fix_enddo_routine nop move #1,lc bclr #16,ssl move #nop_after_jmp,la rti ; <--- note: "rti" and not "rts" **Pertains to:** DSP56300 Family Manual, Section B-4.2, “General Do Restrictions.”	

Errata Number	Document Update	Applies to Mask
ED34	Description (added 1/5/99; identified as a Documentation errata 2/1/99): When stack extansion is enabled, the read result from stack may be improper if two previous executed instructions cause sequential read and write operations with SSH. Two cases are possible: Case 1: For the first executed instruction: move from SSH or bit manipulation on SSH (i.e. jclr, brclr, jset, brset, btst, bsset, jsset, bsclr, jsclr). For the second executed instruction: move to SSH or bit manipulation on SSH (i.e. jsr, bsr, jscc, bscc). For the third executed instruction: an SSL or SSH read from the stack result may be improper - move from SSH or SSL or bit manipulation on SSH or SSL (i.e., bset, bclr, bchg, jclr, brclr, jset, brset, btst, bsset, jsset, bsclr, jsclr). Workaround: Add two NOP instructions before the third executed instruction. Case 2: For the first executed instruction: bit manipulation on SSH (i.e. bset, bclr, bchg). For the second executed instruction: an SSL or SSH read from the stack result may be improper - move from SSH or SSL or bit manipulation on SSH or SSL (i.e., bset, bclr, bchg, jclr, brclr, jset, brset, btst, bsset, jsset, bsclr, jsclr). Workaround: Add two NOP instructions before the second executed instruction. **Pertains to:** DSP56300 Family Manual, Appendix B, add a new section called “Stack Extension Enable Restrictions.” Cover all cases. Also, in Section 6.3.11.15, add a cross reference to this new section.	2K30A

Errata Number	Document Update	Applies to Mask
ED37	Description (added 4/19/99): In paragraph 6.1.1.11 on page 6-12 of the 301 User's Manual, there is an error, as follows: "HIRQ_ is asserted by the HI32 when a host interrupt request (recieve and/or transmit) is generated in the HI32" Workaround/correction: Should be: "HIRQ_ is asserted by the HI32 when a host interrupt request (receive and/or transmit) is generated in the HI32 (as described in paragraphs 6.2.1.1, 6.2.1.1 and 6.2.1.4)."	2K30A
ED38	Description (added 7/14/99): If Port A is used for external accesses, the BAT bits in the AAR3-0 registers must be initialized to the SRAM access type (i.e. BAT = 01) or to the DRAM access type (i.e. BAT = 10). To ensure proper operation of Port A, this initialization must occur even for an AAR register that is not used during any Port A access. Note that at reset, the BAT bits are initialized to 00. **Pertains to:** *DSP56300 Family Manual*, Port A Chapter (Chapter 9 in Revision 2), description of the BAT[1 –0] bits in the AAR3 - AAR0 registers. Also pertains to the core chapter in device-specific user's manuals that include a description of the AAR3 - AAR0 registers with bit definitions (usually Chapter 4).	2K30A

Errata Number	Document Update	Applies to Mask
ED40	Description (added 11/11/99): When an instruction with all the following conditions follows a repeat instruction, then the last move will be corrupted.: 1. The repeated instruction is from external memory. 2. The repeated instruction is a DALU instruction that includes 2 DAL registers, one as a source, and one as destination (e.g. tfr, add). 3. The repeated instruction has a double move in parallel to the DALU instruction: one move's source is the destination of the DALU instruction (causing a DALU interlock); the other move's destination is the source of the DALU instruction. Example: rep #number tfr x0,a x(r0)+,x0 a,y0 ; This instruction is from external memory |__|_____|------|----------> This is condition 3 second part. |_____|----------> This is condition 3, first part - DALU interlock In this example, the second iteration before the last, the "x(r0)+,x0" doesn't happen. On the first iteration before the last, the X0 register is fixed with the "x(r0)+,x0", but the "tfr x0,a" gets the wrong value from the previous iteration's X0. Thus, at the last iteration the A register is fixed with "tfr x0,a", but the "a,y0" transfers the wrong value from the previous iteration's A register to Y0. Workaround: 1. Use the DO instruction instead; mask any necessary interrupts before the DO. 2. Run the REP instructions from internal memory. 3. Don't make DALU interlocks in the repeated instruction. After the repeat make the move. In the example above, all the "move a,y0" are redundant so it can be done in the next instruction: `rep #number` `tfr x0,a x(r0)+,x0` `move a,y0` If no interrupts before the move is a must, mask the interrupts before the REP. **Pertains to:** *DSP56300 Family Manual*, Rev. 2, Section A.3, "Instruction Sequence Restrictions."	2K30A

Errata Number	Document Update	Applies to Mask
ED42	Description (added on 3/22/2000) The DMA End-of-Block-Transfer interrupt cannot be used if DMA is operating in the mode in which DE is not cleared at the end of the block transfer (DTM = 100 or 101). **Pertains to:** *DSP56300 Family Manual*, Rev. 2, Section 10.4.1.2, "End-of-Block-Transfer Interrupt." Also, Section 10.5.3.5, "DMA Control Registers (DCR[5–0]," discussion of bits 21 – 19 (DTM bits).	2K30A

Errata Number	Document Update	Applies to Mask
ED46	Description (added 12/10/2001): The following sequence gives erroneous results: 1) A different slave on the bus terminates a transaction (for example, assertion of "stop"). 2) Immediately afterwards (no more than one PCI clock), the chip's memory space control/status register at PCI address ADDR is read in a single-word transaction. In this transaction, the chip drives to the bus the data corresponding to the register at PCI address ADDR+4, instead of the requested ADDR. NOTE: ADDR is the PCI address of one of the following registers: HCTR (ADDR=$10), HSTR (ADDR=$14), or HCVR (ADDR=$18), and not the data register. Workaround: The user should find a way to set/clear at least one bit in the control/status registers to clearly differentiate between them. For example, you can set HNMI in the HCVR, as this bit will always be 0 in the HSTR. If NMI cannot be used, then HCVR{HV4,HV3,HV2} and HSTR{HF5,HF4,HF3} can be set in any combinations that distinguish between HCVR and HSTR data reads. **Pertains to**: *DSP56301 User's Manual*: Put this errata text as a note in the description of the HCTR (p. 6-48), the HSTR (p. 6-57), and the HCVR (p. 6-59). These page numbers are for Revision 3 of the manual. *DSP56305 User's Manual*: Put this errata text as a note in the description of the HCTR (p. 6-54), the HSTR (p. 6-68), and the HCVR (p. 6-72). These page numbers are for Revision 1of the manual.	2K30A
ED49	Description: (added 6/14/2002) The 5V tolerant pins of the PCI bus do not meet the leakage requirement of the 5V PCI specification when configured as inputs. When connected with pull-up resistors to the 5V supply, the pin voltage value will not reach the supply value, but will reach the Vih value defined by the spec. This does not have an impact on 3V PCI compliance.	2K30A

Errata Number	Document Update	Applies to Mask
ED51	Description (added 12/19/2002): The BSDL file does not correctly reflect the 24-bit port A portion of the BSR. According to the BSDL file, the directional control of these bits is split into two even groups of 12, each group controlled by a single control cell. However, in order to work correctly, these two control bits should always be programmed with the same value in order to control all 24 bits of port A as a unique grouping.	2K30A

NOTES

1. An over-bar (i.e., $\overline{xxxx}$) indicates an active-low signal.
2. The letters seen to the right of the errata tell which DSP56301 mask numbers apply.
3. The Motorola DSP website has additional documentation updates that can be accessed at the following URL:

   http://www.motorola-dsp.com/
4. Information contained in the addendum to the DSP56301 data sheet applies to all members of the DSP56300 core family, as appropriate (i.e, references to the HI32 port do not apply to the DSP56302 and DSP56303).

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