NTD4302

Power MOSFET 68 Amps, 30 Volts

N−Channel DPAK

ON Semiconductor®

http://onsemi.com

Features

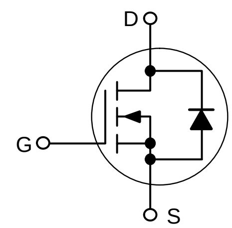
- Ultra Low $R_{DS(on)}$
- Higher Efficiency Extending Battery Life
- Logic Level Gate Drive
- Diode Exhibits High Speed, Soft Recovery
- Avalanche Energy Specified
- I_{DSS} Specified at Elevated Temperature
- DPAK Mounting Information Provided

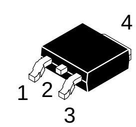
Applications

- DC−DC Converters
- Low Voltage Motor Control
- Power Management in Portable and Battery Powered Products: i.e., Computers, Printers, Cellular and Cordless Telephones, and PCMCIA Cards

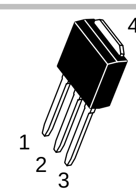
$V_{(BR)DSS}$	$R_{DS(on)}$ TYP	I_D MAX
30 V	7.8 mΩ @ 10 V	68 A

N−Channel



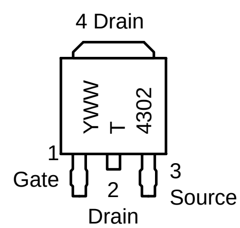


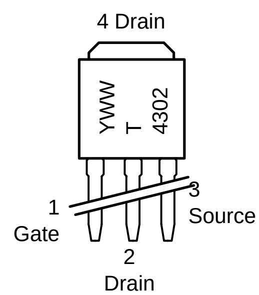
CASE 369AA
DPAK
(Surface Mount)
STYLE 2



CASE 369D
DPAK
(Straight Lead)
STYLE 2

MARKING DIAGRAM & PIN ASSIGNMENTS





T4302 = Device Code
Y = Year
WW = Work Week

ORDERING INFORMATION

Device	Package	Shipping
NTD4302	DPAK	75 Units/Rail
NTD4302−1	DPAK Straight Lead	75 Units/Rail
NTD4302T4	DPAK	2500 Tape & Reel

MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain−to−Source Voltage	V_{DSS}	30	Vdc
Gate−to−Source Voltage − Continuous	V_{GS}	±20	Vdc
Thermal Resistance − Junction−to−Case Total Power Dissipation @ T_C = 25°C Continuous Drain Current @ T_C = 25°C (Note 4) Continuous Drain Current @ T_C = 100°C	 $R_{\theta JC}$ P_D I_D I_D	 1.65 75 68 43	 °C/W Watts Amps Amps
Thermal Resistance − Junction−to−Ambient (Note 2) Total Power Dissipation @ T_A = 25°C Continuous Drain Current @ T_A = 25°C Continuous Drain Current @ T_A = 100°C Pulsed Drain Current (Note 3)	 $R_{\theta JA}$ P_D I_D I_D I_{DM}	 67 1.87 11.3 7.1 36	 °C/W Watts Amps Amps Amps
Thermal Resistance − Junction−to−Ambient (Note 1) Total Power Dissipation @ T_A = 25°C Continuous Drain Current @ T_A = 25°C Continuous Drain Current @ T_A = 100°C Pulsed Drain Current (Note 3)	 $R_{\theta JA}$ P_D I_D I_D I_{DM}	 120 1.04 8.4 5.3 28	 °C/W Watts Amps Amps Amps
Operating and Storage Temperature Range	T_J, T_{stg}	−55 to 150	°C
Single Pulse Drain−to−Source Avalanche Energy − Starting T_J = 25°C (V_{DD} = 30 Vdc, V_{GS} = 10 Vdc, Peak I_L = 17 Apk, L = 5.0 mH, R_G = 25 Ω)	E_{AS}	722	mJ
Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 10 seconds	T_L	260	°C

1. When surface mounted to an FR4 board using the minimum recommended pad size.
2. When surface mounted to an FR4 board using 0.5 sq. in. drain pad size.
3. Pulse Test: Pulse Width = 300 μs, Duty Cycle = 2%.
4. Current Limited by Internal Lead Wires.

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain−Source Breakdown Voltage (V_{GS} = 0 Vdc, I_D = 250 μA)		$V_{(BR)DSS}$	30	−	−	Vdc
Positive Temperature Coefficient			−	25	−	mV/°C
Zero Gate Voltage Drain Current (V_{GS} = 0 Vdc, V_{DS} = 30 Vdc, T_J = 25°C)		I_{DSS}	−	−	1.0	μAdc
(V_{GS} = 0 Vdc, V_{DS} = 30 Vdc, T_J = 125°C)			−	−	10	
Gate−Body Leakage Current (V_{GS} = ±20 Vdc, V_{DS} = 0 Vdc)		I_{GSS}	−	−	±100	nAdc
ON CHARACTERISTICS						
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 250 μAdc)		$V_{GS(th)}$	1.0	1.9	3.0	Vdc
Negative Temperature Coefficient			−	−3.8	−	
Static Drain−Source On−State Resistance (V_{GS} = 10 Vdc, I_D = 20 Adc)		$R_{DS(on)}$	−	0.0078	0.010	Ω
(V_{GS} = 10 Vdc, I_D = 10 Adc)			−	0.0078	0.010	
(V_{GS} = 4.5 Vdc, I_D = 5.0 Adc)			−	0.010	0.013	
Forward Transconductance (V_{DS} = 15 Vdc, I_D = 10 Adc)		gFS	−	20	−	Mhos
DYNAMIC CHARACTERISTICS						
Input Capacitance	(V_{DS} = 24 Vdc, V_{GS} = 0 Vdc, f = 1.0 MHz)	C_{iss}	−	2050	2400	pF
Output Capacitance		C_{oss}	−	640	800	
Reverse Transfer Capacitance		C_{rss}	−	225	310	
SWITCHING CHARACTERISTICS (Note 6)						
Turn−On Delay Time	(V_{DD} = 25 Vdc, I_D = 1.0 Adc, V_{GS} = 10 Vdc, R_G = 6.0 Ω)	$t_{d(on)}$	−	11	20	ns
Rise Time		t_r	−	15	25	
Turn−Off Delay Time		$t_{d(off)}$	−	85	130	
Fall Time		t_f	−	55	90	
Turn−On Delay Time	(V_{DD} = 25 Vdc, I_D = 1.0 Adc, V_{GS} = 10 Vdc, R_G = 2.5 Ω)	$t_{d(on)}$	−	11	20	ns
Rise Time		t_r	−	13	20	
Turn−Off Delay Time		$t_{d(off)}$	−	55	90	
Fall Time		t_f	−	40	75	
Turn−On Delay Time	(V_{DD} = 24 Vdc, I_D = 20 Adc, V_{GS} = 10 Vdc, R_G = 2.5 Ω)	$t_{d(on)}$	−	15	−	ns
Rise Time		t_r	−	25	−	
Turn−Off Delay Time		$t_{d(off)}$	−	40	−	
Fall Time		t_f	−	58	−	
Gate Charge	(V_{DS} = 24 Vdc, I_D = 2.0 Adc, V_{GS} = 10 Vdc)	Q_T	−	55	80	nC
		Q_{gs} (Q1)	−	5.5	−	
		Q_{gd} (Q2)	−	15	−	
BODY−DRAIN DIODE RATINGS (Note 5)						
Diode Forward On−Voltage (I_S = 2.3 Adc, V_{GS} = 0 Vdc)		V_{SD}	−	0.75	1.0	Vdc
(I_S = 20 Adc, V_{GS} = 0 Vdc)			−	0.90	−	
(I_S = 2.3 Adc, V_{GS} = 0 Vdc, T_J = 125°C)			−	0.65	−	
Reverse Recovery Time	(I_S = 2.3 Adc, V_{GS} = 0 Vdc, dI_S/dt = 100 A/μs)	t_{rr}	−	39	65	ns
		t_a	−	20	−	
		t_b	−	19	−	
Reverse Recovery Stored Charge		Q_{rr}	−	0.043	−	μC

5. Indicates Pulse Test: Pulse Width = 300 μsec max, Duty Cycle ≤ 2%.
6. Switching characteristics are independent of operating junction temperature.

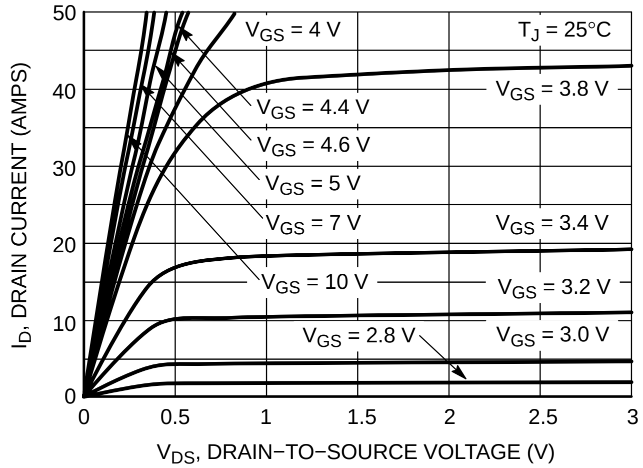


Figure 1. On−Region Characteristics

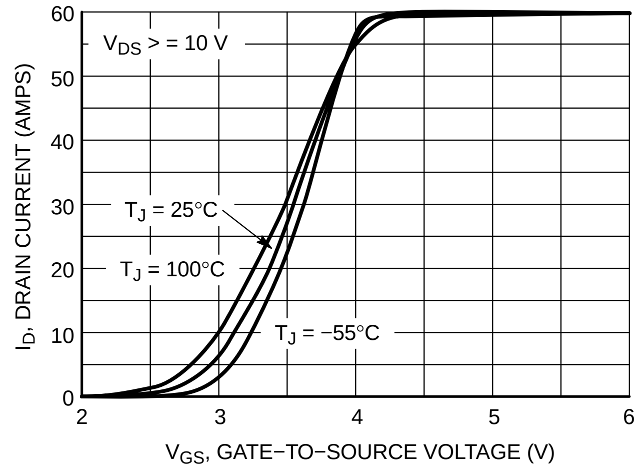


Figure 2. Transfer Characteristics

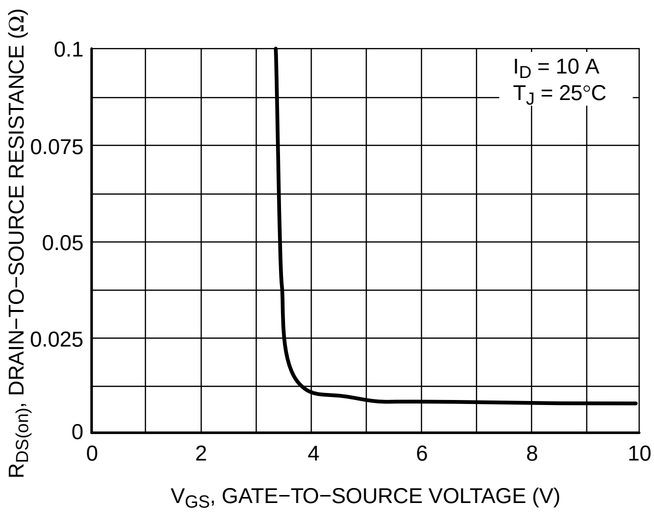


Figure 3. On−Resistance vs. Gate−To−Source Voltage

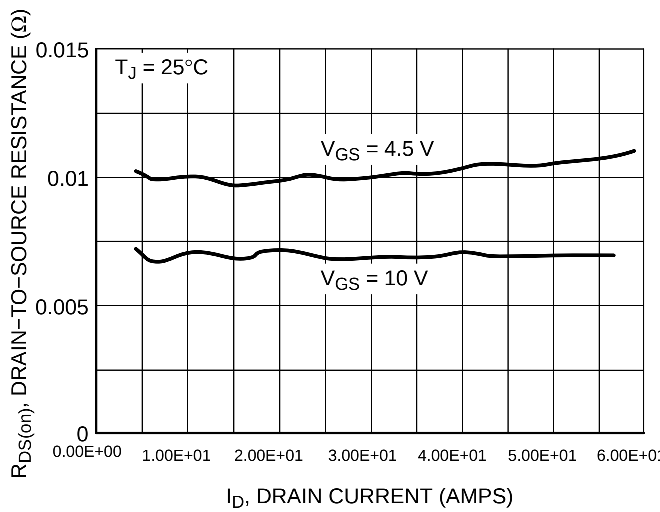


Figure 4. On−Resistance vs. Drain Current and Gate Voltage

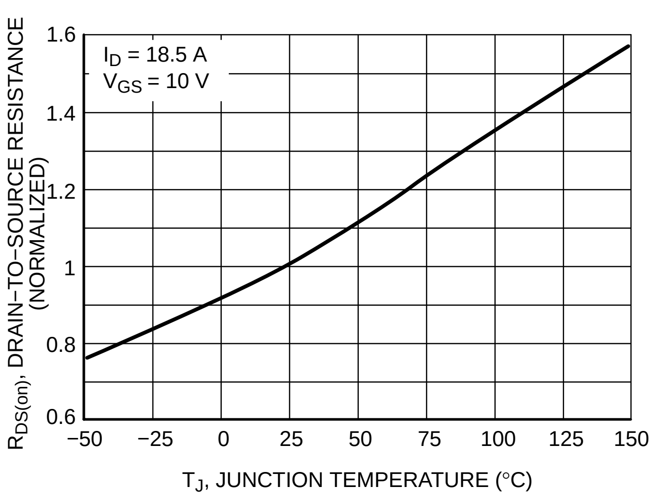


Figure 5. On−Resistance Variation with Temperature

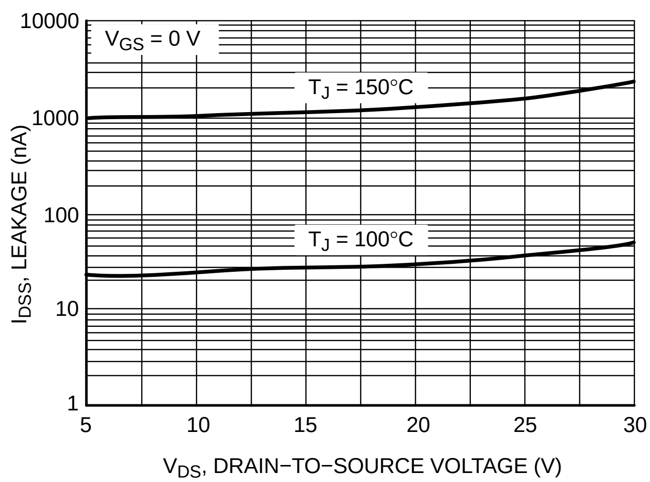


Figure 6. Drain−To−Source Leakage Current vs. Voltage

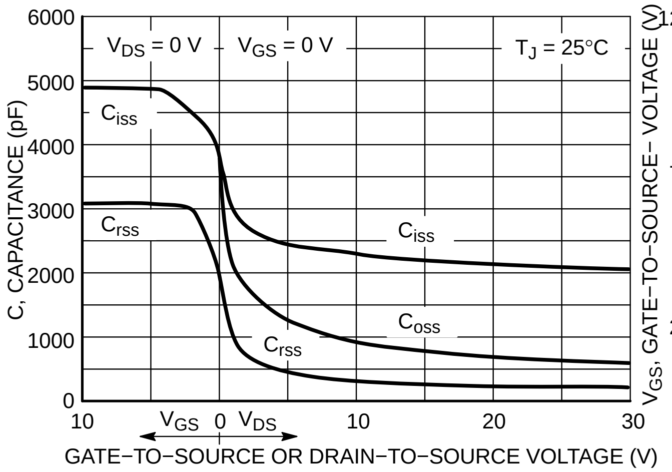


Figure 7. Capacitance Variation

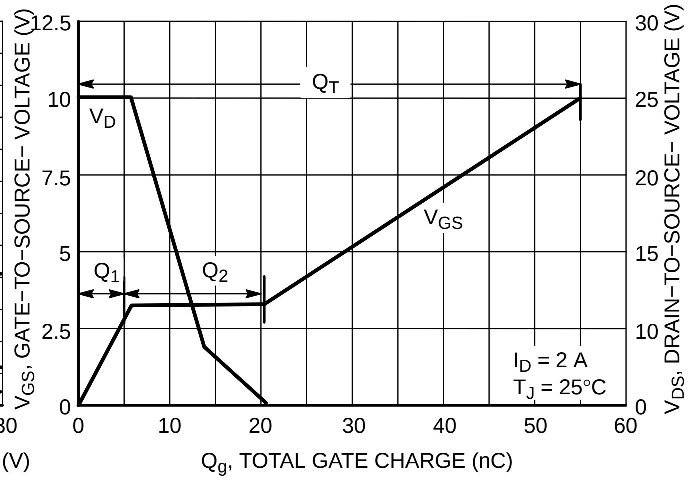


Figure 8. Gate−to−Source and Drain−to−Source Voltage vs. Total Charge

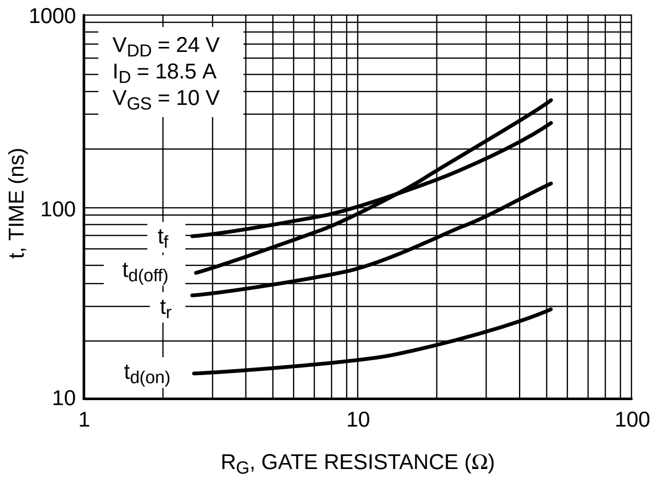


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

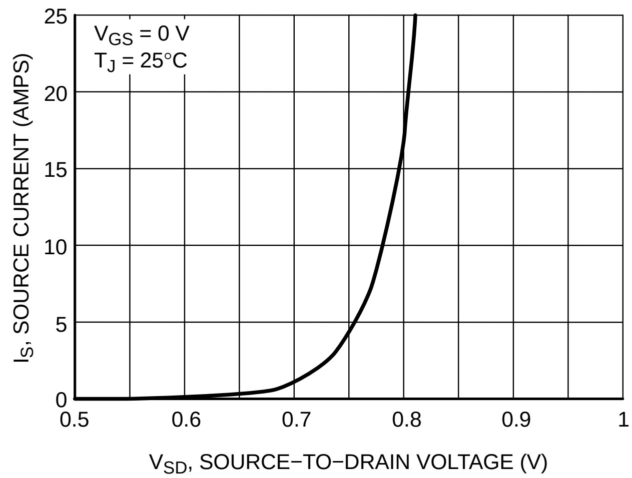


Figure 10. Diode Forward Voltage vs. Current

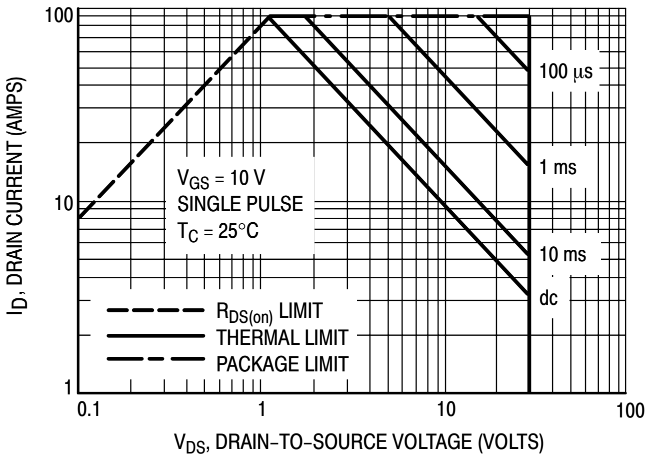


Figure 11. Maximum Rated Forward Biased Safe Operating Area

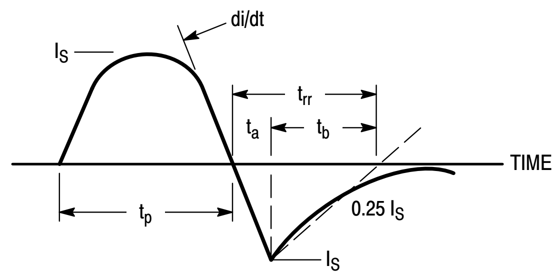


Figure 12. Diode Reverse Recovery Waveform

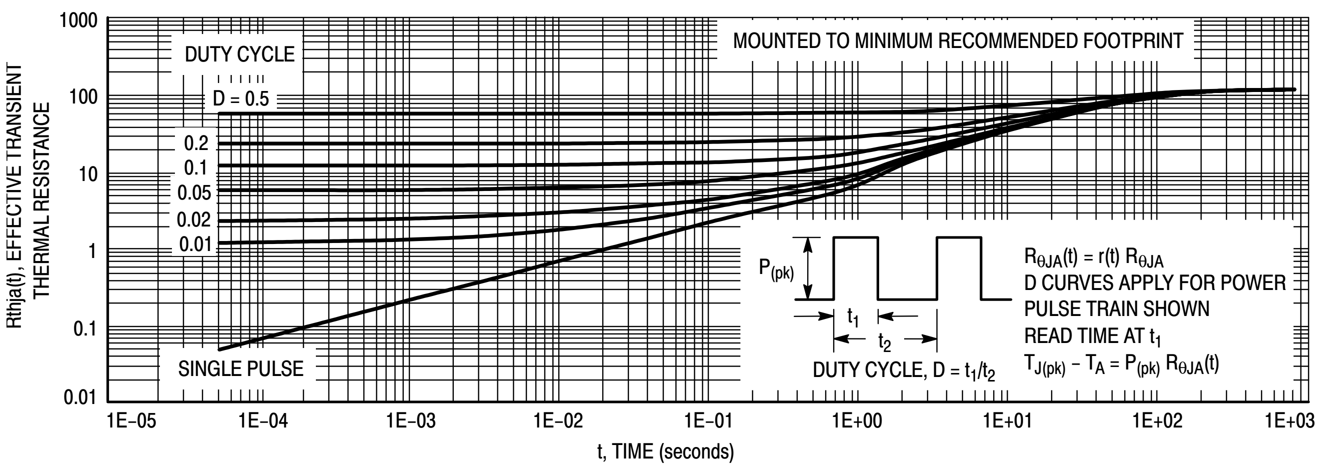
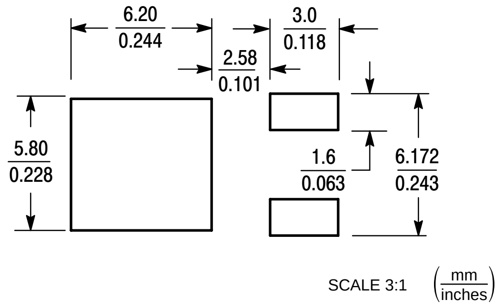


Figure 13. Thermal Response − Various Duty Cycles

INFORMATION FOR USING THE DPAK SURFACE MOUNT PACKAGE

RECOMMENDED FOOTPRINT FOR SURFACE MOUNTED APPLICATIONS

Surface mount board layout is a critical portion of the total design. The footprint for the semiconductor packages must be the correct size to ensure proper solder connection interface between the board and the package. With the correct pad geometry, the packages will self align when subjected to a solder reflow process.



SOLDER STENCIL GUIDELINES

Prior to placing surface mount components onto a printed circuit board, solder paste must be applied to the pads. Solder stencils are used to screen the optimum amount. These stencils are typically 0.008 inches thick and may be made of brass or stainless steel. For packages such as the SC−59, SC−70/SOT−323, SOD−123, SOT−23, SOT−143, SOT−223, SO−8, SO−14, SO−16, and SMB/SMC diode packages, the stencil opening should be the same as the pad size or a 1:1 registration. This is not the case with the DPAK and D^{2}PAK packages. If one uses a 1:1 opening to screen solder onto the drain pad, misalignment and/or “tombstoning” may occur due to an excess of solder. For these two packages, the opening in the stencil for the paste should be approximately 50% of the tab area. The opening for the leads is still a 1:1 registration. Figure 14 shows a typical stencil for the DPAK and D^{2}PAK packages. The pattern of the opening in the stencil for the drain pad is not critical as long as it allows approximately 50% of the pad to be covered with paste.

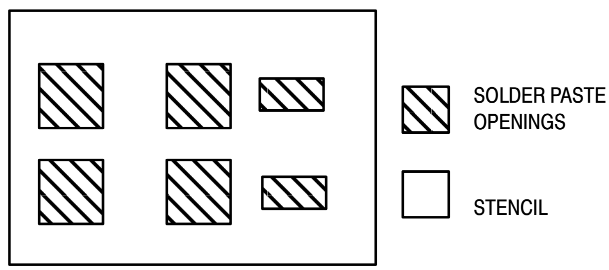


Figure 14. Typical Stencil for DPAK and D^{2}PAK Packages

SOLDERING PRECAUTIONS

The melting temperature of solder is higher than the rated temperature of the device. When the entire device is heated to a high temperature, failure to complete soldering within a short time could result in device failure. Therefore, the following items should always be observed in order to minimize the thermal stress to which the devices are subjected.

- Always preheat the device.
- The delta temperature between the preheat and soldering should be 100°C or less.*
- When preheating and soldering, the temperature of the leads and the case must not exceed the maximum temperature ratings as shown on the data sheet. When using infrared heating with the reflow soldering method, the difference shall be a maximum of 10°C.
- The soldering temperature and time shall not exceed 260°C for more than 10 seconds.
- When shifting from preheating to soldering, the maximum temperature gradient shall be 5°C or less.
- After soldering has been completed, the device should be allowed to cool naturally for at least three minutes. Gradual cooling should be used as the use of forced cooling will increase the temperature gradient and result in latent failure due to mechanical stress.
- Mechanical stress or shock should not be applied during cooling.

* * Soldering a device without preheating can cause excessive thermal shock and stress which can result in damage to the device.

* * Due to shadowing and the inability to set the wave height to incorporate other surface mount components, the D^{2}PAK is not recommended for wave soldering.

TYPICAL SOLDER HEATING PROFILE

For any given circuit board, there will be a group of control settings that will give the desired heat pattern. The operator must set temperatures for several heating zones and a figure for belt speed. Taken together, these control settings make up a heating "profile" for that particular circuit board. On machines controlled by a computer, the computer remembers these profiles from one operating session to the next. Figure 15 shows a typical heating profile for use when soldering a surface mount device to a printed circuit board. This profile will vary among soldering systems, but it is a good starting point. Factors that can affect the profile include the type of soldering system in use, density and types of components on the board, type of solder used, and the type of board or substrate material being used. This profile shows temperature versus time. The line on the graph shows the actual temperature that might be experienced on the surface of a test board at or near a central solder joint. The two profiles are based on a high density and a low density board. The Vitronics SMD310 convection/infrared reflow soldering system was used to generate this profile. The type of solder used was 62/36/2 Tin Lead Silver with a melting point between 177−189°C. When this type of furnace is used for solder reflow work, the circuit boards and solder joints tend to heat first. The components on the board are then heated by conduction. The circuit board, because it has a large surface area, absorbs the thermal energy more efficiently, then distributes this energy to the components. Because of this effect, the main body of a component may be up to 30 degrees cooler than the adjacent solder joints.

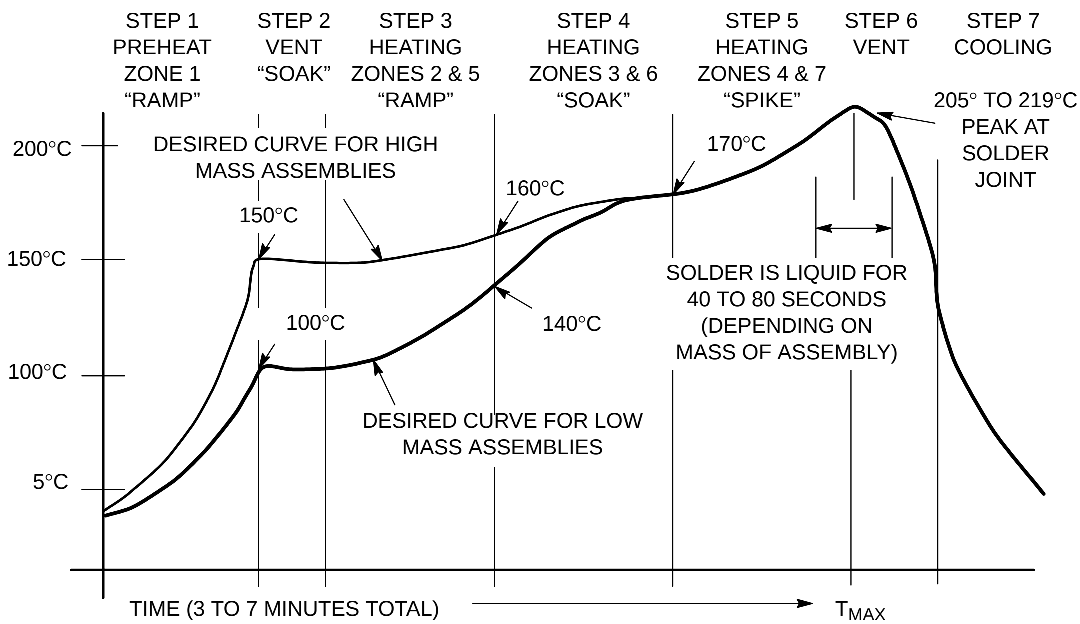
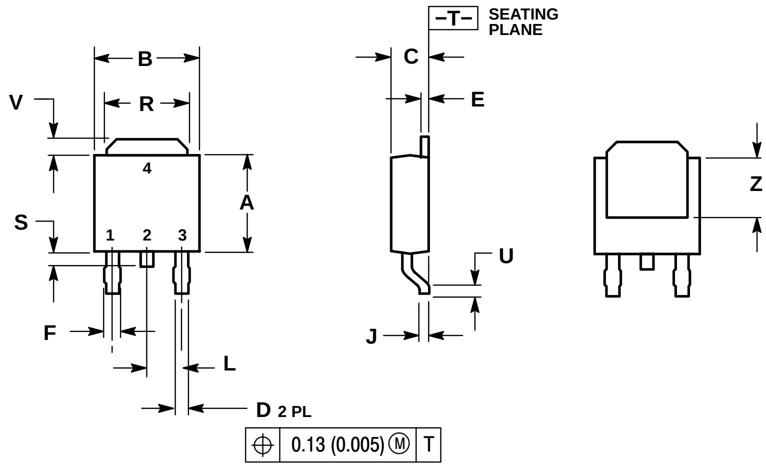


Figure 15. Typical Solder Heating Profile

PACKAGE DIMENSIONS

DPAK
CASE 369AA−01
ISSUE O



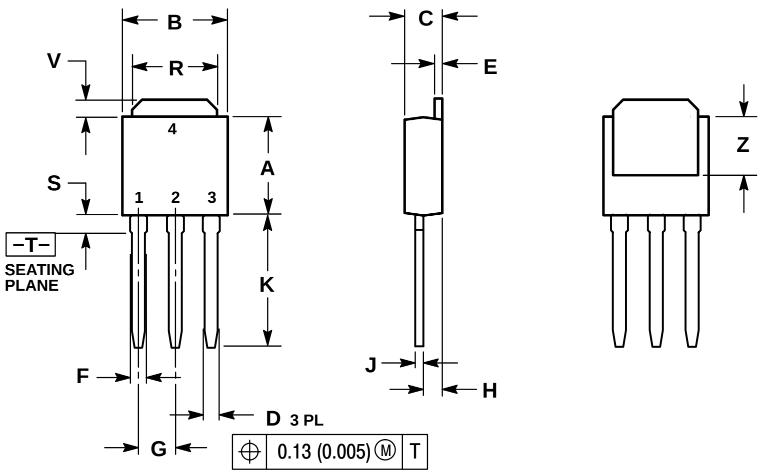
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.235	0.245	5.97	6.22
B	0.250	0.265	6.35	6.73
C	0.086	0.094	2.19	2.38
D	0.025	0.035	0.63	0.88
E	0.018	0.024	0.46	0.61
F	0.033	0.045	0.83	1.14
J	0.018	0.023	0.46	0.58
L	0.090 BSC		2.29 BSC	
R	0.180	0.215	4.57	5.45
S	0.025	0.040	0.63	1.01
U	0.020	−−−	0.51	−−−
V	0.035	0.050	0.89	1.27
Z	0.155	−−−	3.93	−−−

STYLE 2:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

PACKAGE DIMENSIONS

DPAK
CASE 369D−01
ISSUE O



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B	0.250	0.265	6.35	6.73
C	0.086	0.094	2.19	2.38
D	0.027	0.035	0.69	0.88
E	0.018	0.023	0.46	0.58
F	0.037	0.045	0.94	1.14
G	0.090 BSC		2.29 BSC	
H	0.034	0.040	0.87	1.01
J	0.018	0.023	0.46	0.58
K	0.350	0.380	8.89	9.65
R	0.180	0.215	4.45	5.45
S	0.025	0.040	0.63	1.01
V	0.035	0.050	0.89	1.27
Z	0.155	−−−	3.93	−−−

STYLE 2:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

PUBLICATION ORDERING INFORMATION

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