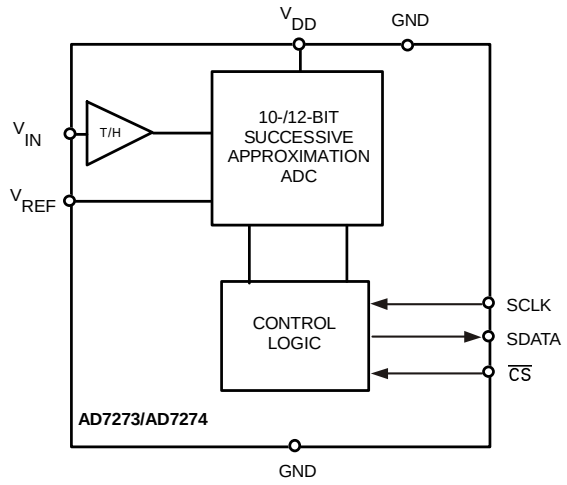
3MSPS,10-/12-Bit ADCs in 8-Lead TSOT

Preliminary Technical Data — AD7273/AD7274

FEATURES
Fast Throughput Rate: 3MSPS
Specified for V_{DD} of 2.35 V to 3.6V
Low Power:
13.5 mW max at 3MSPS with 3V Supplies
Wide Input Bandwidth:
70dB SNR at 1MHz Input Frequency
Flexible Power/Serial Clock Speed Management
No Pipeline Delays
High Speed Serial Interface
SPI™/QSPI™/MICROWIRE™/DSP Compatible
Power Down Mode: 1µA max
8-Lead TSOT Package
8-Lead MSOP Package

APPLICATIONS
Battery-Powered Systems
Personal Digital Assistants
Medical Instruments
Mobile Communications
Instrumentation and Control Systems
Data Acquisition Systems
High-Speed Modems
Optical Sensors

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD7273/AD7274 are 10-bit and 12-bit, high speed, low power, successive-approximation ADCs respectively. The parts operate from a single 2.35V to 3.6 V power supply and feature throughput rates up to 3 MSPS. The parts contain a low-noise, wide bandwidth track/hold amplifier which can handle input frequencies in excess of TBD MHz.

The conversion process and data acquisition are controlled using $\overline{CS}$ and the serial clock, allowing the devices to interface with microprocessors or DSPs. The input signal is sampled on the falling edge of $\overline{CS}$ and the conversion is also initiated at this point. The conversion rate is determined by the SCLK. There are no pipeline delays associated with the part.

The AD7273/AD7274 use advanced design techniques to achieve very low power dissipation at high throughput rates.

The reference for the parts is applied externally and can be in the range of 1.2V to $V_{DD.}$ This allows the widest dynamic input range to the ADC.

PRODUCT HIGHLIGHTS

1. 3MSPS ADCs in an 8-lead TSOT package.
2. High Throughput with Low Power Consumption.
3. Flexible Power/Serial Clock Speed Management.

   The conversion rate is determined by the serial clock allowing the conversion time to be reduced through the serial clock speed increase. This allows the average power consumption to be reduced when a power-down mode is used while not converting. The AD7273/ AD7274 features a power down mode to maximize power efficiency at lower throughput rates. Current consumption is 1 µA max when in Power Down mode.
4. Reference can be driven up to the power supply.
5. No Pipeline Delay.
   The parts feature a standard successive-approximation ADC with accurate control of the sampling instant via a $\overline{CS}$ input and once-off conversion control.

REV. PrB (6/04)

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781/329-4700 World Wide Web Site: http://www.analog.com
Fax: 781/326-8703 Analog Devices, Inc., 2004

AD7273-SPECIFICATIONS

(V_{DD}=+2.35 V to +3.6 V, V_{REF}= +2.5V , f_{SCLK}=52 MHz, f_{SAMPLE}=3 MSPS unless otherwise noted; T_A=T_{MIN} to T_{MAX}, unless otherwise noted.)

Parameter	B Grade[1]	Units	Test Conditions/Comments
DYNAMIC PERFORMANCE			f_{IN} = 1 MHz Sine Wave
Signal-to-Noise + Distortion (SINAD)[2]	61	dB min	
Total Harmonic Distortion (THD)[2]	-73	dB max	
Peak Harmonic or Spurious Noise (SFDR)[2]	-74	dB max	
Intermodulation Distortion (IMD)[2]			
Second Order Terms	-82	dB typ	fa= TBD kHz, fb= TBD kHz
Third Order Terms	-82	dB typ	fa= TBD kHz, fb= TBD kHz
Aperture Delay	TBD	ns typ	
Aperture Jitter	TBD	ps typ	
Full Power Bandwidth	TBD	MHz typ	@ 3 dB
Full Power Bandwidth	TBD	MHz typ	@ 0.1dB
Power Supply Rejection Ratio (PSRR)	TBD	dB typ	
DC ACCURACY			
Resolution	10	Bits	
Integral Nonlinearity[2]	±0.5	LSB max	
Differential Nonlinearity[2]	±0.5	LSB max	Guaranteed No Missed Codes to 10 Bits
Offset Error[2]	±1	LSB max	
	±TBD	LSB typ	
Gain Error[2]	±1	LSB max	
	±TBD	LSB typ	
Total Unadjusted Error (TUE)[2]	±TBD	LSB max	
ANALOG INPUT			
Input Voltage Range	0 to V_{REF}	Volts	
DC Leakage Current	±0.5	µA max	
Input Capacitance	TBD	pF typ	
REFERENCE INPUT			
V_{REF} Input Voltage Range	1.2 to V_{DD}	Vmin/Vmax	
DC leakage Current	±TBD	µA max	
Input Capacitance	TBD	pF max	
Input Impedance	TBD	kΩ typ	
LOGIC INPUTS			
Input High Voltage, V_{INH}	0.7(V_{DD})	V min	2.35V≤ Vdd ≤2.7V
	2	V min	2.7V< Vdd ≤ 3.6V
Input Low Voltage, V_{INL}	0.2(V_{DD})	V max	2.35V≤Vdd< 2.7V
	0.8	V max	2.7V ≤Vdd≤ 3.6V
Input Current, I_{IN}, SCLK Pin	±0.5	µA max	Typically TBD nA, V_{IN}= 0 V or V_{DD}
Input Current, I_{IN}, $\overline{CS}$ Pin	±TBD	µA max	
Input Capacitance, C_{IN}[3]	10	pF max	
LOGIC OUTPUTS			
Output High Voltage, V_{OH}	V_{DD} - 0.2	V min	I_{SOURCE}= 200 µA,V_{DD}= 2.35 V to 3.6 V
Output Low Voltage, V_{OL}	0.2	V max	I_{SINK}= 200µA
Floating-State Leakage Current	±1	µA max	
Floating-State Output Capacitance[3]	10	pF max	
Output Coding	Straight (Natural) Binary		
CONVERSION RATE			
Conversion Time	230	ns max	12 SCLK cycles with SCLK at 52 MHz
Track/Hold Acquisition Time[2]	50	ns max	
Throughput Rate	3	MSPS max	

NOTES
[1]Temperature range from –40°C to +85°C.
[2]See Terminology.
[3]Guaranteed by Characterization.

Specifications subject to change without notice.

AD7273-SPECIFICATIONS

(V_{DD}=+2.35 V to +3.6 V, V_{REF}= +2 .5V, f_{SCLK}=52 MHz, f_{SAMPLE}=3MSPS unless otherwise noted; T_A=T_{MIN} to T_{MAX}, unless otherwise noted.)

Parameter	B Grade[1]	Units	Test Conditions/Comments
POWER REQUIREMENTS			
V_{DD}	2.35/3.6	V min/Vmax	
I_{DD}			Digital I/Ps= 0V or V_{DD}
Normal Mode(Static)	2.5	mA typ	V_{DD}= 2.35V to 3.6V, SCLK On or Off
Normal Mode (Operational)	4.5	mA max	V_{DD}= 2.35V to 3.6V, f_{SAMPLE} = 3MSPS
Full Power-Down Mode (Static)	1	µA max	SCLK On or Off, typically TBD nA
Full Power-Down Mode (Dynamic)	TBD	mA typ	V_{DD}= 3V, f_{SAMPLE} = 1MSPS
Power Dissipation[4]			
Normal Mode (Operational)	13.5	mW max	V_{DD}=3V, f_{SAMPLE} = 3MSPS
Full Power-Down	3	µW max	V_{DD}=3V

NOTES
[1]Temperature range from –40°C to +85°C.
[2]See Terminology.
[3]Guaranteed by Characterization.
[4]See Power Versus Throughput Rate section.
Specifications subject to change without notice.

AD7274-SPECIFICATIONS

(V_{DD}=+2.35 V to +3.6 V, V_{REF}= +2.5V, f_{SCLK}=52 MHz, f_{SAMPLE}=3MSPS unless otherwise noted; T_A=T_{MIN} to T_{MAX}, unless otherwise noted.)

Parameter	B Grade[1]	Units	Test Conditions/Comments
DYNAMIC PERFORMANCE			f_{IN} = 1 MHz Sine Wave
Signal-to-Noise + Distortion (SINAD)[2]	70	dB min	
Signal-to-Noise Ratio (SNR)	71	dB min	
Total Harmonic Distortion (THD)[2]	-80	dB typ	
Peak Harmonic or Spurious Noise (SFDR)[2]	-82	dB typ	
Intermodulation Distortion (IMD)[2]			
Second Order Terms	-84	dB typ	fa= TBD kHz, fb= TBD kHz
Third Order Term	-84	dB typ	fa= TBD kHz, fb= TBD kHz
Aperture Delay	TBD	ns typ	
Aperture Jitter	TBD	ps typ	
Full Power Bandwidth	TBD	MHz typ	@ 3 dB
Full Power Bandwidth	TBD	MHz typ	@ 0.1dB
Power Supply Rejection Ratio (PSRR)	TBD	dB typ	
DC ACCURACY			
Resolution	12	Bits	
Integral Nonlinearity[2]	±1	LSB max	
Differential Nonlinearity[2]	±1	LSB max	Guaranteed No Missed Codes to 12 Bits
Offset Error[2]	±TBD	LSB max	
Gain Error[2]	±TBD	LSB max	
Total Unadjusted Error (TUE)[2]	±TBD	LSB max	
ANALOG INPUT			
Input Voltage Range	0 to V_{REF}	Volts	
DC Leakage Current	±0.5	µA max	
Input Capacitance	TBD	pF typ	
REFERENCE INPUT			
V_{REF} Input Voltage Range	1.2 to V_{DD}	Vmin/Vmax	
DC leakage Current	±TBD	µA max	
Input Capacitance	TBD	pF max	
Input Impedance	TBD	kΩ typ	
LOGIC INPUTS			
Input High Voltage, V_{INH}	0.7(V_{DD})	V min	2.35V≤ Vdd ≤2.7V
	2	V min	2.7V < Vdd≤ 3.6V
Input Low Voltage, V_{INL}	0.2(V_{DD})	V max	2.35V≤Vdd< 2.7V
	0.8	V max	2.7V ≤Vdd≤ 3.6V
Input Current, I_{IN},SCLK Pin	±0.5	µA max	Typically TBD nA, V_{IN}= 0 V or V_{DD}
Input Current, I_{IN}, $\overline{CS}$ Pin	±TBD	µA max	
Input Capacitance, C_{IN}[3]	10	pF max	
LOGIC OUTPUTS			
Output High Voltage, V_{OH}	V_{DD} - 0.2	V min	I_{SOURCE}= 200 µA;V_{DD}= 2.35 V to 3.6 V
Output Low Voltage, V_{OL}	0.2	V max	I_{SINK}=200 µA
Floating-State Leakage Current	±1	µA max	
Floating-State Output Capacitance[3]	10	pF max	
Output Coding	Straight (Natural) Binary		
CONVERSION RATE			
Conversion Time	270	ns max	14 SCLK Cycles with SCLK at 52 MHz
Track/Hold Acquisition Time[2]	50	ns max	
Throughput Rate	3	MSPS max	See Serial Interface Section

NOTES

[1]Temperature range from –40°C to +85°C.

[2]See Terminology.

[3]Guranteed by Characterization.

Specifications subject to change without notice.

AD7274 SPECIFICATIONS

(V_{DD}=+2.35 V to +3.6 V, V_{REF}= + 2.5V, f_{SCLK}=52 MHz, f_{SAMPLE}=3MSPS unless otherwise noted; T_A=T_{MIN} to T_{MAX}, unless otherwise noted.)

Parameter	B Grade[1]	Units	Test Conditions/Comments
POWER REQUIREMENTS			
V_{DD}	2.35/3.6	V min/Vmax	
I_{DD}			Digital I/Ps= 0V or V_{DD}
Normal Mode (Static)	2.5	mA typ	V_{DD}= 2.35V to 3.6V,SCLK On or Off
Normal Mode (Operational)	4.5	mA max	V_{DD}= 2.35V to 3.6V, f_{SAMPLE}=3MSPS
Full Power-Down Mode(Static)	1	µA max	SCLK On or Off, typically TBD nA
Full Power-Down Mode(Dynamic)	TBD	mA typ	V_{DD}= 3V, f_{SAMPLE}=1MSPS
Power Dissipation[4]			
Normal Mode (Operational)	13.5	mW max	V_{DD}= 3 V, f_{SAMPLE}= 3MSPS
Full Power-Down	3	µW max	V_{DD}= 3 V

NOTES
[1]Temperature range from –40°C to +85°C.
[2]See Terminology.
[3]Guranteed by Characterization.
[4] See Power Versus Throughput Rate section.
Specifications subject to change without notice.

TIMING SPECIFICATIONS[1] (V_{DD}= +2.35 V to +3.6 V; V_{REF} = 2.5V, T_A= T_{MIN} to T_{MAX}, unless otherwise noted.)

Parameter	Limit at T_{MIN}, T_{MAX} AD7273/AD7274	Units	Description
f_{SCLK} [2]	20	KHz min[3]	
	52	MHz max	
$t_{CONVERT}$	14 x t_{SCLK}		AD7274
	12 x t_{SCLK}		AD7273
t_{QUIET}	TBD	ns min	Minimum Quiet Time required between Bus Relinquish and start of Next Conversion
t_1	10	ns min	Minimum $\overline{CS}$ Pulse Width
t_2	TBD	ns min	$\overline{CS}$ to SCLK Setup Time
t_3 [4]	TBD	ns max	Delay from $\overline{CS}$ Until SDATA Three-State Disabled
t_4 [4]	TBD	ns max	Data Access Time After SCLK Falling Edge
t_5	0.4t_{SCLK}	ns min	SCLK Low Pulse Width
t_6	0.4t_{SCLK}	ns min	SCLK High Pulse Width
t_7 [4]	TBD	ns min	SCLK to Data Valid Hold Time
t_8 [5]	TBD	ns max	SCLK Falling Edge to SDATA Three-State
	TBD	ns min	SCLK Falling Edge to SDATA Three-State
$t_{power-up}$ [6]	TBD	µs max	Power Up Time from Full Power-down

NOTES

[1]Guaranteed by Characterization. All input signals are specified with tr=tf=5ns (10% to 90% of V_{DD}) and timed from a voltage level of 1.6Volts.

[2]Mark/Space ratio for the SCLK input is 40/60 to 60/40.

[3]Minimum f_{sclk} at which specifications are guaranteed.

[4]Measured with the load circuit of Figure 1 and defined as the time required for the output to cross the Vih or Vil voltage.

[5]t_8 is derived form the measured time taken by the data outputs to change 0.5 V when loaded with the circuit of Figure 1. The measured number is then extrapolated back to remove the effects of charging or discharging the 25 pF capacitor. This means that the time, t_8, quoted in the timing characteristics is the true bus relinquish time of the part and is independent of the bus loading.

[6]See Power-up Time section.

Specifications subject to change without notice.

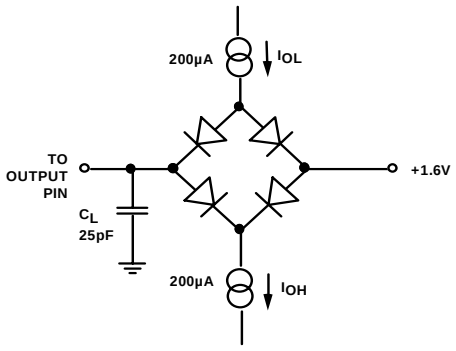


Figure 1. Load Circuit for Digital Output Timing Specifications

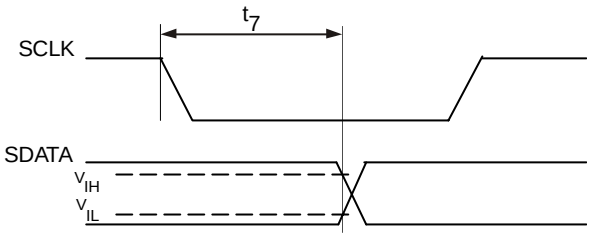


Figure 3. Hold time after SCLK falling edge

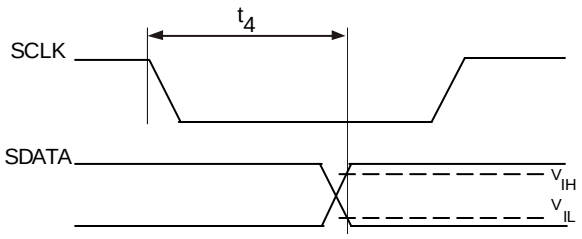


Figure 2. Access time after SCLK falling edge

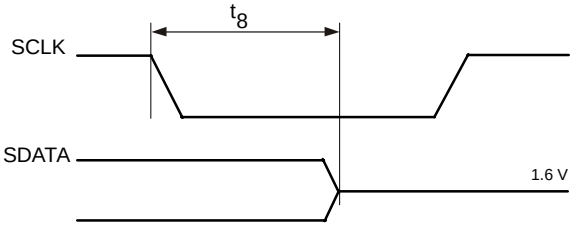


Figure 4. SCLK falling edge to SDATA Three-State

Figures 5 and 6 show some of the timing parameters from the Timing Specifications table.

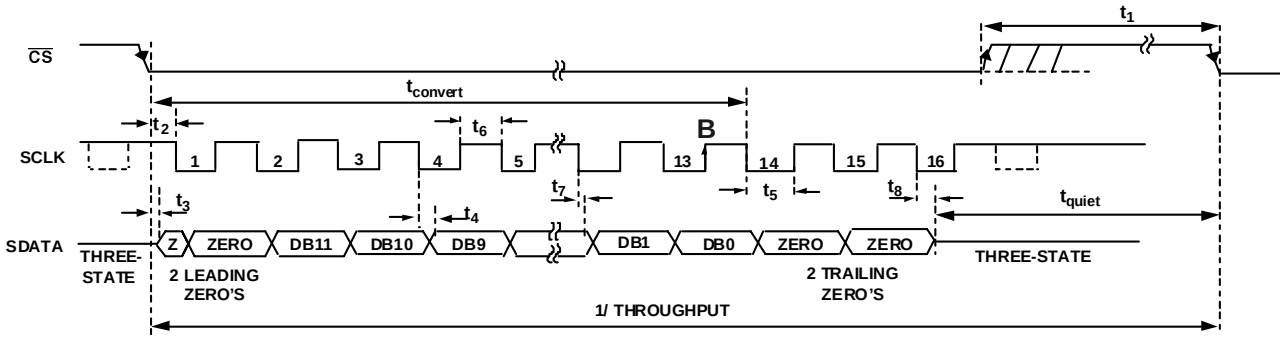


Figure 5. AD7274 Serial Interface Timing Diagram

Timing Example 1

From Figure 6, having f_{SCLK} = 52 MHz and a throughput of 3MSPS, gives a cycle time of $t_2 + 12.5(1/f_{SCLK}) + t_{ACQ}$ = 333 ns. With t_2 = TBD ns min, this leaves t_{ACQ} to be TBD ns. This TBD ns satisfies the requirement of 50 ns for t_{ACQ}. Figure 6 shows that, t_{ACQ} comprises of $2.5(1/f_{SCLK}) + t_8 + t_{QUIET}$, where t_8 = TBD ns max. This allows a value of TBD ns for t_{QUIET} satisfying the minimum requirement of TBD ns.

Timing Example 2

Having f_{SCLK} = 20 MHz and a throughput of 1.5 MSPS, gives a cycle time of $t_2 + 12.5(1/f_{SCLK}) + t_{ACQ}$ = 666 ns. With t_2 = TBD ns min, this leaves t_{ACQ} to be TBD ns. This TBD ns satisfies the requirement of 50 ns for t_{ACQ}. From Figure 6, t_{ACQ} comprises of $2.5(1/f_{SCLK}) + t_8 + t_{QUIET}$, where t_8 = TBD ns max. This allows a values of TBD ns for t_{QUIET} satisfying the minimum requirement of TBD ns.

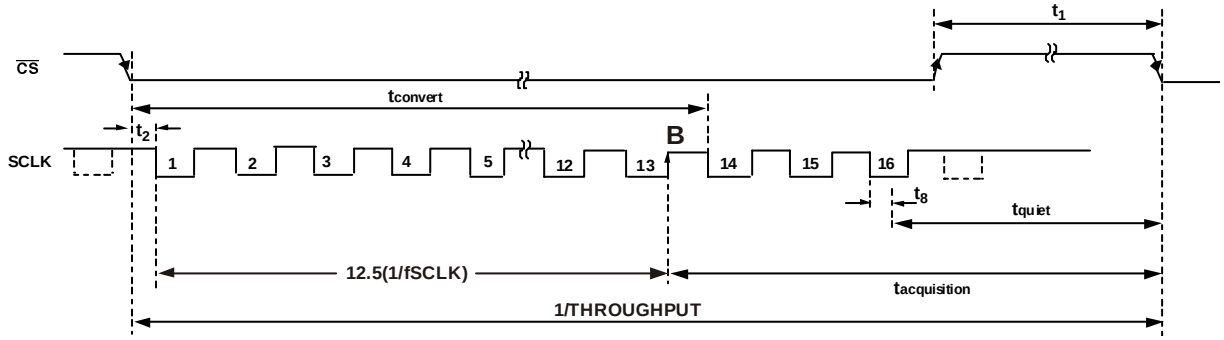


Figure 6. Serial Interface Timing Example

ABSOLUTE MAXIMUM RATINGS[1]

(T_A = +25°C unless otherwise noted)

V_{DD} to GND.....-0.3 V to TBD V
Analog Input Voltage to GND.....–0.3 V to V_{DD} + 0.3 V
Reference Input Voltage to GND...–0.3 V to V_{DD} + 0.3 V
Digital Input Voltage to GND.....–0.3 V to TBD V
Digital Output Voltage to GND....–0.3 V to V_{DD} + 0.3 V
Input Current to Any Pin Except Supplies[2].....±10 mA

Operating Temperature Range
Commercial (B Grade).....–40°C to +85°C
Storage Temperature Range.....–65°C to +150°C
Junction Temperature.....150°C

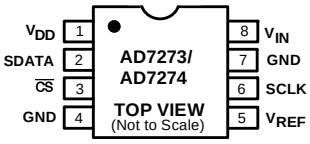
8-lead TSOT Package
θ_{JA} Thermal Impedance.....TBD°C/W
θ_{JC} Thermal Impedance.....TBD°C/W

8-lead MSOP Package
θ_{JA} Thermal Impedance.....205.9°C/W
θ_{JC} Thermal Impedance.....43.74°C/W

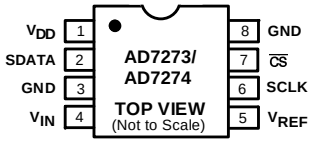
Lead Temperature Soldering
Reflow (10-30 secs).....+TBD°C
ESD.....TBDKV

NOTES
[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
[2]Transient currents of up to 100 mA will not cause SCR latch up.

PIN CONFIGURATION
AD7273/AD7274



8-lead MSOP



8-lead TSOT

ORDERING GUIDE

Model	Temperature Range	Linearity Error (LSB)[1]	Package Option	Package Description	Branding Information
AD7274BUJ-REEL	–40°C to +85°C	±1 max	UJ-8	TSOT	TBD
AD7274BRM	–40°C to +85°C	±1 max	RM-8	MSOP	TBD
AD7273BUJ-REEL	–40°C to +85°C	±0.5 max	UJ-8	TSOT	TBD
AD7273BRM	–40°C to +85°C	±0.5 max	RM-8	MSOP	TBD

NOTES
[1]Linearity error here refers to integral nonlinearity.

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD7273/AD7274 feature proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN FUNCTION DESCRIPTION

Pin Mnemonic	Function
$\overline{CS}$	Chip Select. Active low logic input. This input provides the dual function of initiating conversion on the AD7273/AD7274 and also frames the serial data transfer.
V_{DD}	Power Supply Input. The V_{DD} range for the AD7273/AD7274 is from +2.35V to +3.6V.
GND	Analog Ground. Ground reference point for all circuitry on the AD7273/AD7274. All analog input signals should be referred to this GND voltage.
V_{IN}	Analog Input. Single-ended analog input channel. The input range is 0 to V_{REF}.
V_{REF}	Voltage Reference Input. This pin becomes the reference voltage input and an external reference should be applied at this pin. The external reference input range is 1.2V to V_{DD}. A TBD μF capacitor should be tied between this pin and AGND.
SDATA	Data Out. Logic output. The conversion result from the AD7273/AD7274 is provided on this output as a serial data stream. The bits are clocked out on the falling edge of the SCLK input. The data stream from the AD7274 consists of two leading zeros followed by the 12 bits of conversion data followed by two trailing zeros, which is provided MSB first. The data stream from the AD7273 consists of two leading zeros followed by the 10 bits of conversion data followed by four trailing zeros, which is provided MSB first.
SCLK	Serial Clock. Logic input. SCLK provides the serial clock for accessing data from the part. This clock input is also used as the clock source for the AD7273/AD7274's conversion process.

TERMINOLOGY

Integral Nonlinearity (INL)
This is the maximum deviation from a straight line passing through the endpoints of the ADC transfer function. For the AD7273/AD7274, the endpoints of the transfer function are zero scale, a 1/2 LSB below the first code transition, and full scale, a point 1/2 LSB above the last code transition.

Differential Nonlinearity (DNL)
This is the difference between the measured and the ideal 1 LSB change between any two adjacent codes in the ADC.

Offset Error
This is the deviation of the first code transition (00 . . . 000) to (00 . . . 001) from the ideal, i.e, AGND + 0.5 LSB.

Gain Error
This is the deviation of the last code transition (111 . . . 110) to (111 . . . 111) from the ideal, i.e, V_{REF} – 1.5LSB after the offset error has been adjusted out.

Total Unadjusted Error (TUE)
This is a comprehensive specification which includes gain, linearity and offset errors.

Track/Hold Acquisition Time
The Track/Hold acquisition time is the time required for the output of the track/hold amplifier to reach its final value, within ±0.5 LSB, after the end of conversion. See Serial Interface section for more details.

Signal to Noise Ratio (SNR)
This is the measured ratio of signal to noise at the output to the A/D converter. The signal is the rms value of the sine wave input. Noise is the rms quantization error within the Nyquist bandwitdh (fs/2). The rms value of a sine wave is one half its peak to peak value divided by √2 and the rms value for the quantization noise is q/√12. The ratio is dependant on the number of quantization levels in the digitization process; the more levels, the smaller the quantization noise. For an ideal N-bit converter, the SNR is defined as:

$$SNR = 6.02\ N + 1.76\ dB$$

Thus for a 12-bit converter this is 74 dB, for a 10-bit converter it is 62 dB.
Practically, though, various error sources in the ADC cause the measured SNR to be less than the theoretical value. These errors occur due to integral and differential nonlinearities, internal AC noise sources, etc.

Signal-to- (Noise + Distortion) Ratio (SINAD)
This is the measured ratio of signal to (noise + distortion) at the output of the A/D converter. The signal is the rms value of the sine wave and noise is the rms sum of all nonfundamentals signals up to half the sampling frequency (fs/2), including harmonics but excluding dc.

Total Harmonic Distortion (THD)
Total harmonic distortion is the ratio of the rms sum of harmonics to the fundamental. It is defined as:

$$THD\ (dB) = 20 \log \frac{\sqrt{V_2^2 + V_3^2 + V_4^2 + V_5^2 + V_6^2}}{V_1}$$

where V_1 is the rms amplitude of the fundamental and V_2, V_3, V_4, V_5 and V_6 are the rms amplitudes of the second through the sixth harmonics.

Peak Harmonic or Spurious Noise (SFDR)
Peak harmonic or spurious noise is defined as the ratio of the rms value of the next largest component in the ADC output spectrum (up to $f_S/2$ and excluding dc) to the rms value of the fundamental. Normally, the value of this specification is determined by the largest harmonic in the spectrum, but for ADCs where the harmonics are buried in the noise floor, it will be a noise peak.

Intermodulation Distortion (IMD)
With inputs consisting of sine waves at two frequencies, fa and fb, any active device with nonlinearities will create distortion products at sum and difference frequencies of mfa ± nfb where m, n = 0, 1, 2, 3, etc. Intermodulation distortion terms are those for which neither m nor n are equal to zero. For example, the second order terms include (fa + fb) and (fa – fb), while the third order terms include (2fa + fb), (2fa – fb), (fa + 2fb) and (fa – 2fb).

The AD7273/AD7274 are tested using the CCIF standard where two input frequencies are used (see fa and fb in the specification page). In this case, the second order terms are usually distanced in frequency from the original sine waves while the third order terms are usually at a frequency close to the input frequencies. As a result, the second and third order terms are specified separately. The calculation of the intermodulation distortion is as per the THD specification where it is the ratio of the rms sum of the individual distortion products to the rms amplitude of the sum of the fundamentals expressed in dBs.

Power Supply Rejection Ratio (PSRR)
The power supply rejection ratio is defined as the ratio of the power in the ADC output at full-scale frequency, f, to the power of a 200 mV p-p sine wave applied to the ADC V_{DD} supply of frequency f_s.

$$\text{PSRR (dB)} = 10\ log\ (Pf/\ Pf_s)$$

Pf is the power at frequency f in the ADC output; Pf_s is the power at frequency f_s coupled onto the ADC V_{DD} supply.

Aperture Delay
This is the measured interval between the leading edge of the sampling clock and the point at which the ADC actually takes the sample.

Aperture Jitter
This is the sample-to-sample variation in the effective point in time at which the sample is taken.

CIRCUIT INFORMATION

The AD7273/AD7274 are high speed, low power, 10-/12-Bit, single supply, analog-to-digital converters (ADC) respectively. The parts can be operated from a +2.35V to +3.6V supply. When operated from any supply voltage within this range, the AD7273/AD7274 are capable of throughput rates of 3 MSPS when provided with a 52 MHz clock.

The AD7273/AD7274 provide the user with an on-chip track/hold, A/D converter, and a serial interface housed in an 8-lead TSOT or an 8-lead MSOP package, which offers the user considerable space saving advantages over alternative solutions. The serial clock input accesses data from the part but also provides the clock source for the successive-approximation A/D converter. The analog input range is 0 to V_{REF}. An external reference is required by the ADC and this reference can be in the range of 1.2V to V_{DD}.

The AD7273/AD7274 also feature a Power-Down option to allow power saving between conversions. The power down feature is implemented across the standard serial interface as described in the Modes of Operation section.

CONVERTER OPERATION

The AD7273/AD7274 is a successive-approximation analog-to-digital converter based around a charge redistribution DAC. Figures 7 and 8 show simplified schematics of the ADC. Figure 7 shows the ADC during its acquisition phase. SW2 is closed and SW1 is in position A, the comparator is balanced and the sampling capacitor acquires the signal on V_{IN}.

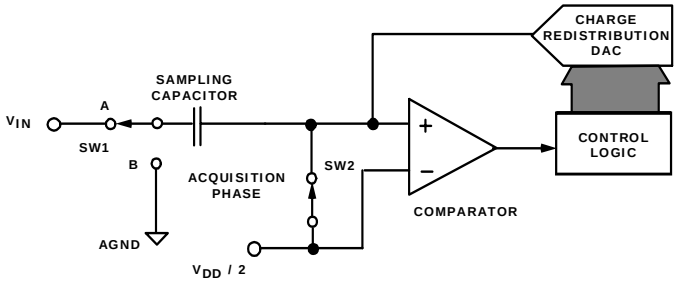


Figure 7. ADC Acquisition Phase

When the ADC starts a conversion, see Figure 8, SW2 will open and SW1 will move to position B causing the comparator to become unbalanced. The Control Logic and the Charge Redistribution DAC are used to add and subtract fixed amounts of charge from the sampling capacitor to bring the comparator back into a balanced condition. When the comparator is rebalanced the conversion is complete. The Control Logic generates the ADC output code. Figure 9 shows the ADC transfer function.

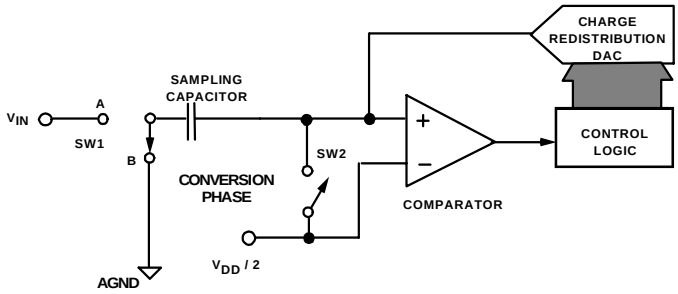


Figure 8. ADC Conversion Phase

ADC TRANSFER FUNCTION

The output coding of the AD7273/AD7274 is straight binary. The designed code transitions occur midway between succesive integer LSB values, i.e, 0.5LSB, 1.5LSBs, etc. The LSB size is $V_{REF}/4096$ for the AD7274, $V_{REF}/1024$ for the AD7273. The ideal transfer characteristic for the AD7273/AD7274 is shown in Figure 9.

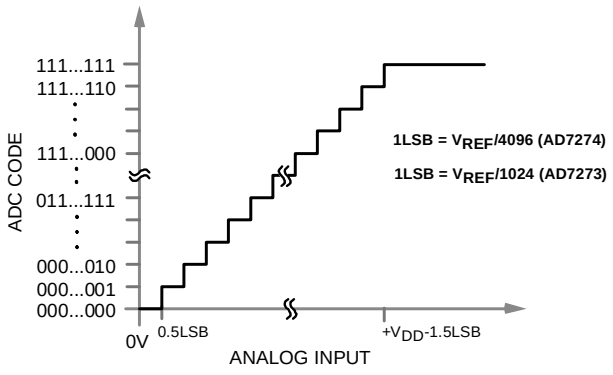


Figure 9. AD7273/AD7274 Transfer Characteristic

PERFORMANCE CURVES

Dynamic Performance curves

TPC 1 and TPC 2 show typical FFT plots for the AD7274 and AD7273 respectively, at 3 MSPS sample rate and TBD KHz input tone.

TPC 3 shows the Signal-to-(Noise+Distortion) Ratio performance versus Input frequency for various supply voltages while sampling at 3 MSPS with a SCLK frequency of 52 MHz for the AD7274.

TPC 4 shows the Signal to Noise Ratio (SNR) performance versus Input frequency for various supply voltages while sampling at 3 MSPS with a SCLK frequency of 52 MHz for the AD7274.

TPC 5 shows a graph of the Total Harmonic Distortion (THD) versus Analog input signal frequency for various supply voltages while sampling at 3 MSPS with a SCLK frequency of 52 MHz for the AD7274.

TPC 6 shows a graph of the Total Harmonic Distortion (THD) versus Analog input frequency for different source impedances when using a supply voltage of TBD V, SCLK frequency of 52 MHz and sampling at a rate of 3 MSPS for the AD7274. See Analog Input section.

TPC 7 shows the Power Supply Rejection Ratio (PSRR) versus Supply Ripple Frequency for the AD7274 when no decoupling is used. See PSRR in the Terminology section.

DC Accuracy curves

TPC 8and TPC 9 show typical INL and DNL performance for the AD7276.

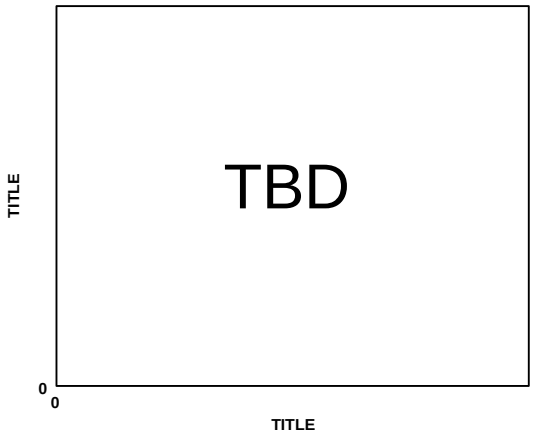
TP10 and TPC11 show Change in DNL and INL versus Reference Voltage when using a supply voltage of 3V.

Power Requirements curves

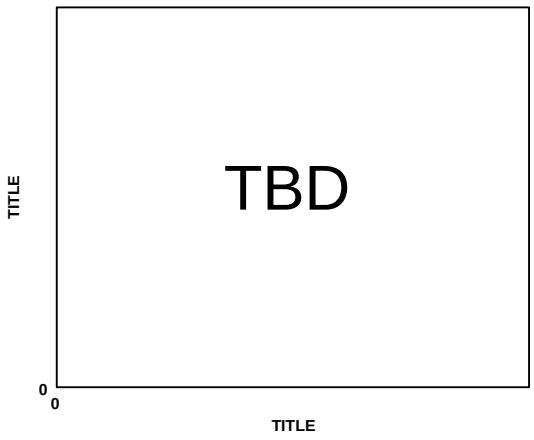
TPC12 shows Maximum current versus Supply voltage for the AD7274 with different SCLK frequencies.

See also Power versus Throughput Rate.

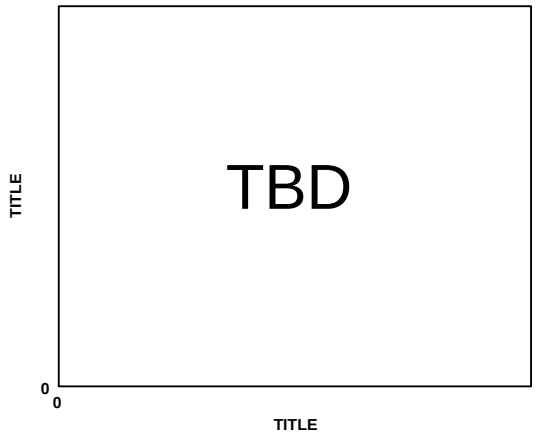
Typical Performance Characteristics



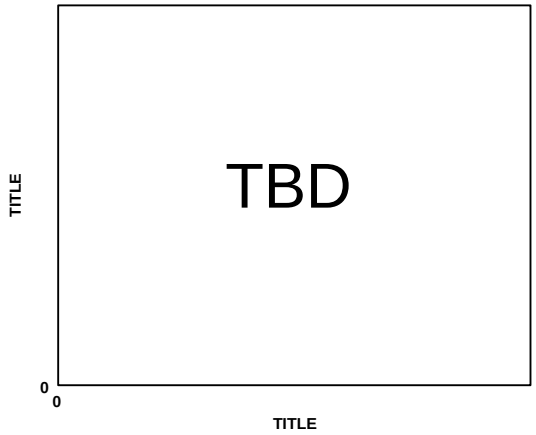
TPC 1. AD7274 Dynamic performance at 3 MSPS



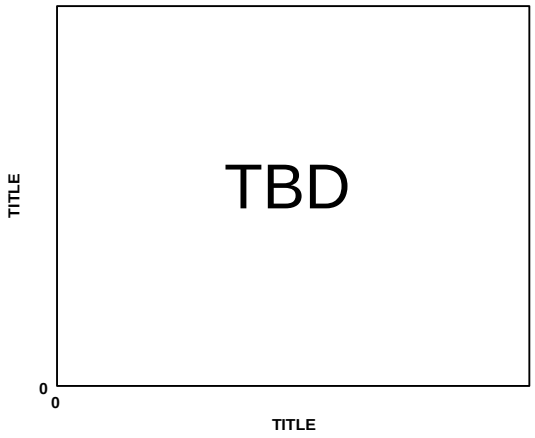
TPC 2. AD7273 Dynamic performance at 3 MSPS



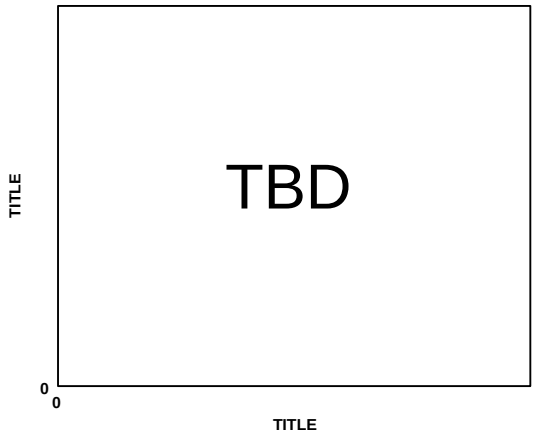
TPC 3. AD7274 SINAD vs Analog Input Frequency at 3 MSPS for various Supply Voltages



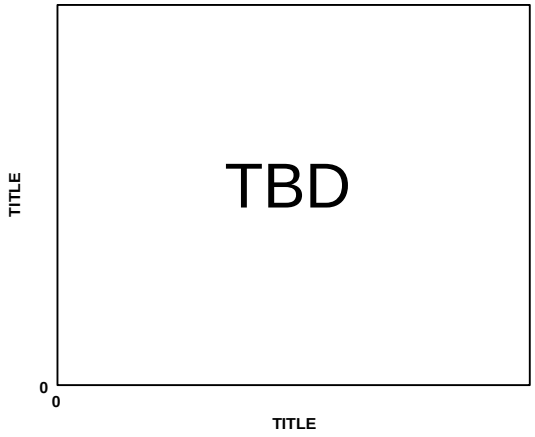
TPC 6. THD vs. Analog Input Frequency for various Source Impedance



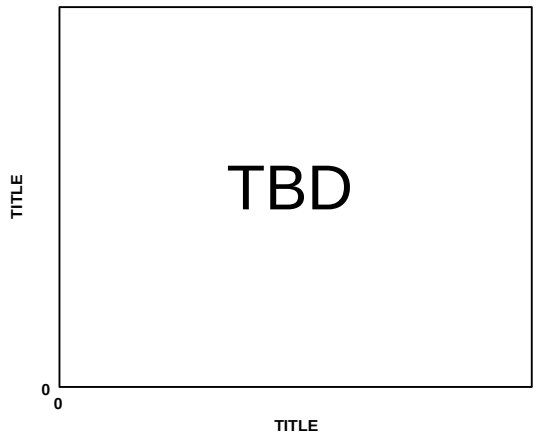
TPC 4. AD7274 SNR vs Analog Input Frequency at 3 MSPS for various Supply Voltages



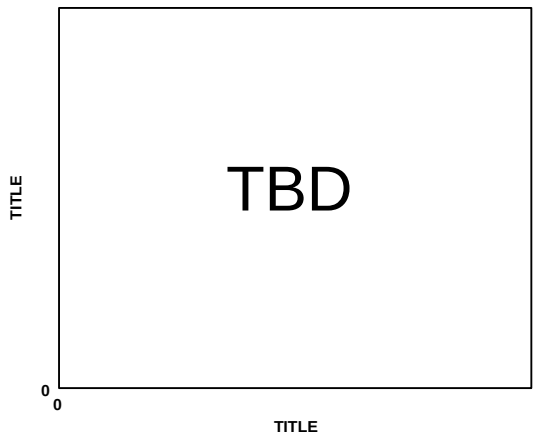
TPC 7. Power Supply Rejection Ratio (PSRR) versus Supply Ripple Frequency



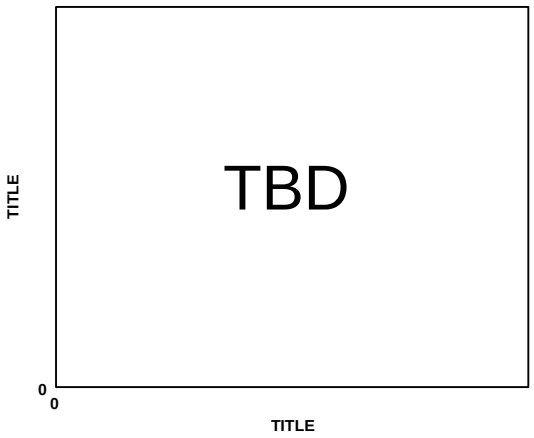
TPC 5. THD vs. Analog Input Frequency at 3 MSPS for various Supply Voltages



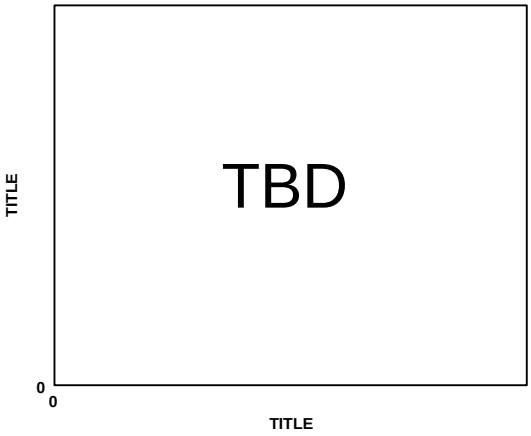
TPC 8. AD7276 INL performance



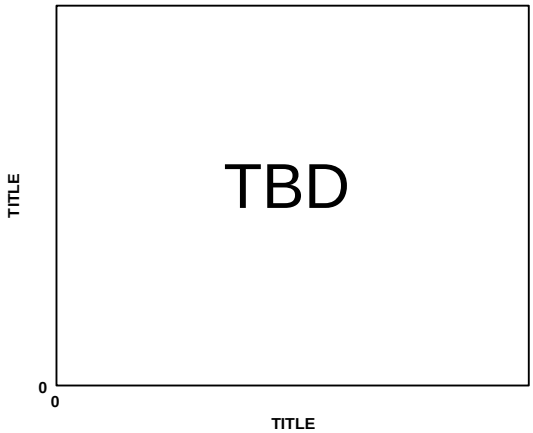
TPC 9. AD7276 DNL performance



TPC 12. Maximum current vs Supply voltage for different SCLK frequencies.



TPC 10. Change in INL versus Reference Voltage



TPC 11. Change in DNL versus Reference Voltage

TYPICAL CONNECTION DIAGRAM

Figure 10 shows a typical connection diagram for the AD7273/AD7274. An external reference must be applied to the ADC. This reference can be in the range of 1.2V to V_{DD}. A precision reference like the REF19X family or the ADR421 can be used to supply the reference voltage to the AD7273/AD7274.

The conversion result is output in a 16-bit word with two leading zeros followed by the 12-bit or 10-bit result. The 12-bit result from the AD7274 will be followed by two trailing zeros and the 10-bit result from the AD7273 will be followed by four trailing zeros.

Table I provides some typical performance data with various references under the same set-up conditions.

Voltage Reference	AD7274 SNR Performance TBD kHz Input
AD780@2.5V	TBD dB
REF192	TBD dB
ADR421	TBD dB
ADR291	TBD dB

Table I. AD7274 performance for various Voltage References IC

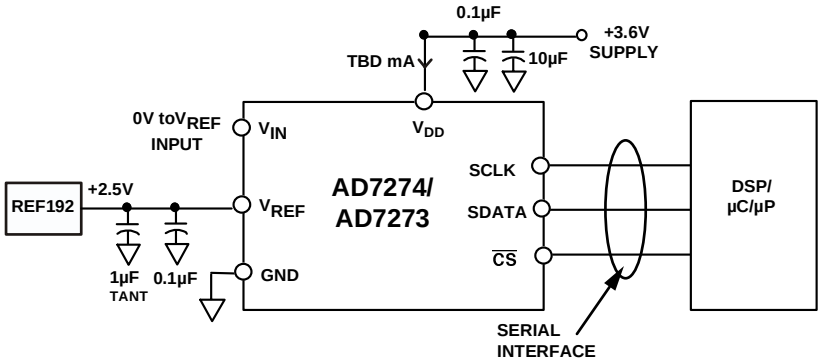


Figure 10. AD7273/AD7274 Typical Connection Diagram

Analog Input

Figure 11 shows an equivalent circuit of the analog input structure of the AD7273/AD7274. The two diodes D1 and D2 provide ESD protection for the analog inputs. Care must be taken to ensure that the analog input signal never exceeds the supply rails by more than 300mV. This will cause these diodes to become forward biased and start conducting current into the substrate. 10mA is the maximum current these diodes can conduct without causing irreversable damage to the part. The capacitor C1 in Figure 11 is typically about 4pF and can primarily be attributed to pin capacitance. The resistor R1 is a lumped component made up of the on resistance of a switch. This resistor is typically about TBDΩ. The capacitor C2 is the ADC sampling capacitor and has a capacitance of TBD pF typically. For ac applications, removing high frequency components from the analog input signal is recommended by use of a bandpass filter on the relevant analog input pin. In applications where harmonic distortion and signal to noise ratio are critical, the analog input should be driven from a low impedance source. Large source impedances will significantly affect the ac performance of the ADC. This may necessitate the use of an input buffer amplifier. The choice of the op-amp will be a function of the particular application.

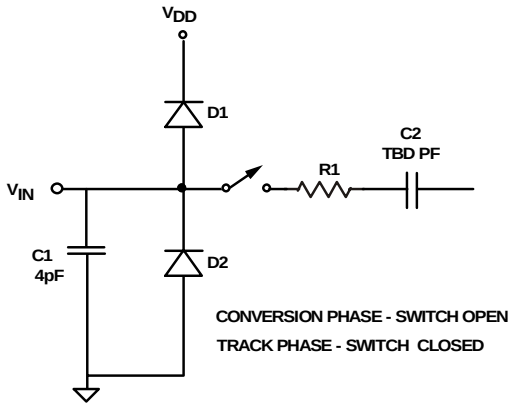


Figure 11. Equivalent Analog Input Circuit

Table II provides some typical performance data with various op-amps used as the input buffer under the same set-up conditions.

Op-amp in the input buffer	AD7274 SNR Performance TBD kHz Input
AD8510	TBD dB
AD8610	TBD dB
AD8038	TBD dB
AD8519	TBD dB

Table II. AD7274 performance for various Input Buffers

When no amplifier is used to drive the analog input, the source impedance should be limited to low values. The maximum source impedance will depend on the amount of total harmonic distortion (THD) that can be tolerated. The THD will increase as the source impedance increases and performance will degrade. See TPC6.

Digital Inputs

The digital inputs applied to the AD7273/AD7274 are not limited by the maximum ratings which limit the analog inputs. Instead, the digitals inputs applied can go to TBD V and are not restricted by the V_{DD} + 0.3V limit as on the analog inputs. For example, if the AD7273/AD7274 were operated with a V_{DD} of 3V then 5V logic levels could be used on the digital inputs. However, it is important to note that the data output on SDATA will still have 3V logic levels when V_{DD}= 3V. Another advantage of SCLK and $\overline{CS}$ not being restricted by the V_{DD} + 0.3V limit is the fact that power supply sequencing issues are avoided. If $\overline{CS}$ or SCLK are applied before V_{DD} then there is no risk of latch-up as there would be on the analog inputs if a signal greater than 0.3V was applied prior to V_{DD}.

MODES OF OPERATION

The mode of operation of the AD7273/AD7274 is selected by controlling the logic state of the $\overline{CS}$ signal during a conversion. There are two possible modes of operation, Normal Mode and Power-Down Mode. The point at which $\overline{CS}$ is pulled high after the conversion has been initiated will determine whether the AD7273/AD7274 will enter Power-Down Mode or not. Similarly, if already in Power-Down then $\overline{CS}$ can control whether the device will return to Normal operation or remain in Power-Down. These modes of operation are designed to provide flexible power management options. These options can be chosen to optimize the power dissipation/throughput rate ratio for different application requirements.

Normal Mode

This mode is intended for fastest throughput rate performance as the user does not have to worry about any power-up times with the AD7273/AD7274 remaining fully powered all the time. Figure 12 shows the general diagram of the operation of the AD7273/AD7274 in this mode.

The conversion is iniated on the falling edge of $\overline{CS}$ as described in the Serial Interface section. To ensure the part remains fully powered up at all times $\overline{CS}$ must remain low until at least 10 SCLK falling edges have elapsed after the falling edge of $\overline{CS}$. If $\overline{CS}$ is brought high any time after the 10th SCLK falling, the part will remain powered up but the conversion will be terminated and SDATA will go back into three-state.

For the AD7274 a minimum of 14 serial clock cycles are required to complete the conversion and access the complete conversion result. For the AD7273 a minimum of 12 serial clock cycles are required to complete the conversion and access the complete conversion result.

$\overline{CS}$ may idle high until the next conversion or may idle low until $\overline{CS}$ returns high sometime prior to the next conversion (effectively idling $\overline{CS}$ low).

Once a data transfer is complete (SDATA has returned to three-state), another conversion can be initiated after the quiet time, t_{QUIET}, has elapsed by bringing $\overline{CS}$ low again.

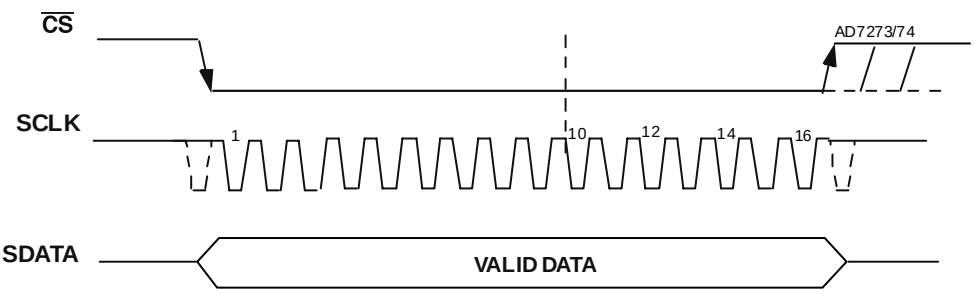


Figure 12. Normal Mode Operation

Power-Down Mode

This mode is intended for use in applications where slower throughput rates are required; either the ADC is powered down between each conversion, or a series of conversions may be performed at a high throughput rate and then the ADC is powered down for a relatively long duration between these bursts of several conversions. When the AD7273/AD7274 is in Power-Down, all analog circuitry is powered down.

To enter Power-Down, the conversion process must be interrupted by bringing $\overline{CS}$ high anywhere after the second falling edge of SCLK and before the 10th falling edge of SCLK as shown in Figure 13. Once $\overline{CS}$ has been brought high in this window of SCLKs, then the part will enter Power-Down and the conversion that was intiated by the falling edge of $\overline{CS}$ will be terminated and SDATA will go back into three-state. If $\overline{CS}$ is brought high before the second SCLK falling edge, then the part will remain in Normal Mode and will not power-down. This will avoid accidental power-down due to glitches on the $\overline{CS}$ line.

In order to exit this mode of operation and power the AD7273/AD7274 up again, a dummy conversion is performed. On the falling edge of $\overline{CS}$ the device will begin to power up, and will continue to power up as long as $\overline{CS}$ is held low until after the falling edge of the 10th SCLK. The device will be fully powered up once 16 SCLKs have elapsed and valid data will result from the next conversion as shown in Figure 14. If $\overline{CS}$ is brought high before the 10th falling edge of SCLK, then the AD7273/AD7274 will go back into Power- Down again. This avoids accidental power up due to glitches on the $\overline{CS}$ line or an inadvertent burst of 8 SCLK cycles while $\overline{CS}$ is low. So, although the device may begin to power up on the falling edge of $\overline{CS}$, it will power down again on the rising edge of $\overline{CS}$ as long as it occurs before the 10th SCLK falling edge.

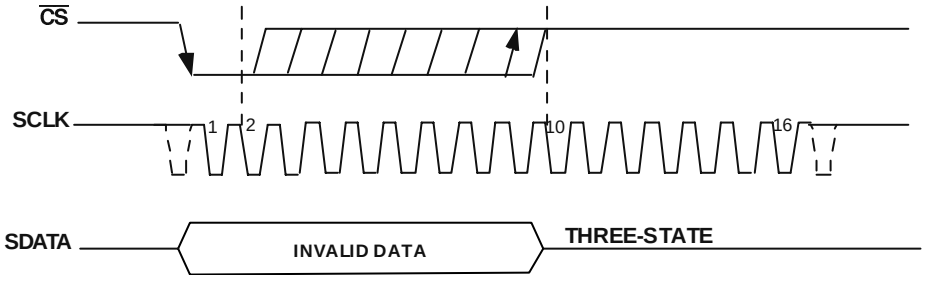


Figure 13. Entering Power Down Mode

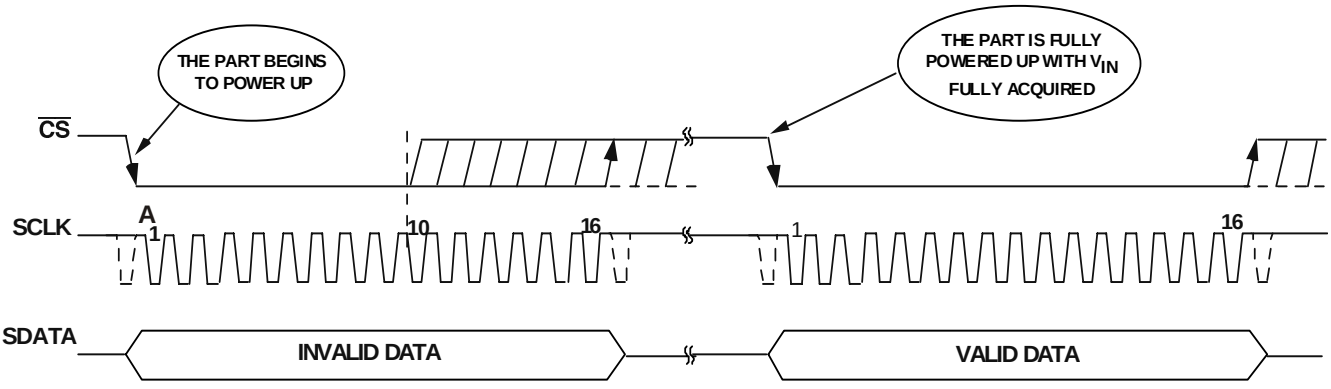


Figure 14. Exiting Power Down Mode

Power-up Time

The power-up time of the AD7273/AD7274 is TBD ns, which means that with any frequency of SCLK up to 52 MHz, one dummy cycle will always be sufficient to allow the device to power up. Once the dummy cycle is complete, the ADC will be fully powered up and the input signal will be acquired properly. The quite time t_{QUIET} must still be allowed from the point where the bus goes back into three-state after the dummy conversion, to the next falling edge of $\overline{CS}$. When running at 3 MSPS throughput rate, the AD7273/AD7274 will power up and acquire a signal within ±0.5 LSB in one dummy cycle, i.e. TBD ns.

When powering up from the Power-Down mode with a dummy cycle, as in Figure 14, the track and hold which was in hold mode while the part was powered down, returns to track mode after the first SCLK edge the part receives after the falling edge of $\overline{CS}$. This is shown as point A in Figure 14. Although at any SCLK frequency one dummy cycle is sufficient to power the device up and acquire V_{IN}, it does not necessarily mean that a full dummy cycle of 16 SCLKs must always elapse to power up the device and acquire V_{IN} fully; TBD ns will be sufficient to power the device up and acquire the input signal. If, for example, a 25 MHz SCLK frequency was applied to the ADC, the cycle time would be 640 ns. In one dummy cycle, 640 ns, the part would be powered up and V_{IN} acquired fully. However after TBD ns with a 25 MHz SCLK only TBD SCLK cycles would have elapsed. At this stage, the ADC would be fully powered up and the signal acquired. So, in this case the $\overline{CS}$ can be brought high after the 10th SCLK falling edge and brought low again after a time t_{QUIET} to initiate the conversion.

When power supplies are first applied to the AD7273/AD7274, the ADC may either power up in the Power-Down mode or in Normal mode. Because of this, it is best to allow a dummy cycle to elapse to ensure the part is fully powered up before attempting a valid conversion. Likewise, if it is intended to keep the part in the Power-Down mode while not in use and the user wishes the part to power up in Power-Down mode, then the dummy cycle may be used to ensure the device is in Power-Down by executing a cycle such as that shown in Figure 13. Once supplies are applied to the AD7273/AD7274, the power up time is the same as that when powering up from the Power-Down mode. It takes approximately TBD ns to power up fully if the part powers up in Normal mode. It is not necessary to wait TBD ns before executing a dummy cycle to ensure the desired mode of operation. Instead, the dummy cycle can occur directly after power is supplied to the ADC. If the first valid conversion is then performed directly after the dummy conversion, care must be taken to ensure that adequate acquisition time has been allowed. As mentioned earlier, when powering up from the Power-Down mode, the part will return to track upon the first SCLK edge applied after the falling edge of $\overline{CS}$. However, when the ADC powers up initially after supplies are applied, the track and hold will already be in track. This means, assuming one has the facility to monitor the ADC supply current, if the ADC powers up in the desired mode of operation and thus a dummy cycle is not required to change mode, then neither is a dummy cycle required to place the track and hold into track.

POWER VERSUS THROUGHPUT RATE

By using the Power-Down mode on the AD7273/AD7274 when not converting, the average power consumption of the ADC decreases at lower throughput rates. Figure 15 shows how as the throughput rate is reduced, the device remains in its Power-Down state longer and the average power consumption over time drops accordingly.

For example, if the AD7273/AD7274 is operated in a continuous sampling mode with a throughput rate of 500KSPS and a SCLK of 52MHz (V_{DD}= 3V), and the device is placed in the Power-Down mode between conversions, then the power consumption is calculated as follows. The power dissipation during normal operation is 13.5 mW (V_{DD}= 3V). If the power up time is one dummy cycle, i.e. 333ns, and the remaining conversion time is another cycle, i.e. 333ns, then the AD7273/AD7274 can be said to dissipate 13.5mW for 666ns during each conversion cycle.If the throughput rate is 500KSPS, the cycle time is 2µs and the average power dissipated during each cycle is (666/2000) x (13.5 mW)= 4.5mW.

Figure 15 shows the Power vs. Throughput Rate when using the Power-Down mode between conversions at 3V. The Power-Down mode is intended for use with throughput rates of approximately TBD MSPS and under as at higher sampling rates there is no power saving made by using the Power-Down mode.

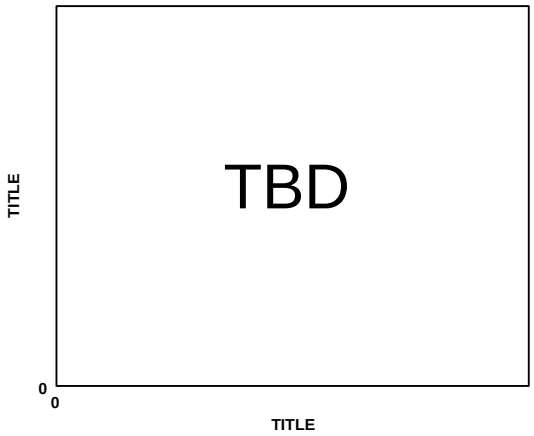


Figure 15. Power vs Throughput

SERIAL INTERFACE

Figures 16 and 17 show the detailed timing diagram for serial interfacing to the AD7274 and AD7273 respectively. The serial clock provides the conversion clock and also controls the transfer of information from the AD7273/AD7274 during conversion.

The $\overline{CS}$ signal initiates the data transfer and conversion process. The falling edge of $\overline{CS}$ puts the track and hold into hold mode, takes the bus out of three-state and the analog input is sampled at this point. The conversion is also initiated at this point.

For the AD7274 the conversion will require 14 SCLK cycles to complete. Once 13 SCLK falling edges have elapsed the track and hold will go back into track on the next SCLK rising edge as shown in Figure 16 at point B. If the rising edge of $\overline{CS}$ occurs before 14 SCLKs have elapsed then the conversion will be terminated and the SDATA line will go back into three-state. If 16 SCLKs are considered in the cycle, the last two bits will be zeros and SDATA will return to three-state on the 16th SCLK falling edge as shown in Figure 16.

For the AD7273 the conversion will require 12 SCLK cycles to complete. Once 11 SCLK falling edges have elapsed, the track and hold will go back into track on the next SCLK rising edge, as shown in Figure 17 at point B. If the rising edge of $\overline{CS}$ occurs before 12 SCLKs have elapsed then the conversion will be terminated and the SDATA line will go back into three-state. If 16 SCLKs are considered in the cycle, the AD7273 will clock out four trailing zeros for the last four bits and SDATA will return to three-state on the 16th SCLK falling edge, as shown in Figure 17.

If the user considers a 14 SCLKs cycle serial interface for the AD7273/AD7274, $\overline{CS}$ needs to be brought high after the 14th SCLK falling edge, the last two trailing zeros will be ignored and SDATA will go back into three-state. In this case, a 45 MHz serial clock would allow to achieve 3MSPS throughput rate.

$\overline{CS}$ going low clocks out the first leading zero to be read in by the microcontroller or DSP. The remaining data is then clocked out by subsequent SCLK falling edges beginning with the 2nd leading zero. Thus, the first falling clock edge on the serial clock has the first leading zero provided and also clocks out the second leading zero. The final bit in the data transfer is valid on the 16th falling edge, having being clocked out on the previous (15th) falling edge.

In applications with a slower SCLK, it is possible to read in data on each SCLK rising edge. In that case, the first falling edge of SCLK will clock out the second leading zero and it could be read in the first rising edge. However, the first leading zero that was clocked out when $\overline{CS}$ went low will be missed unless it was not read in the first falling edge. The 15th falling edge of SCLK will clock out the last bit and it could be read in the 15th rising SCLK edge.

If $\overline{CS}$ goes low just after one the SCLK falling edge has elapsed, $\overline{CS}$ will clock out the first leading zero as before and it may be read in the SCLK rising edge. The next SCLK falling edge will clock out the second leading zero and it could be read in the following rising edge.

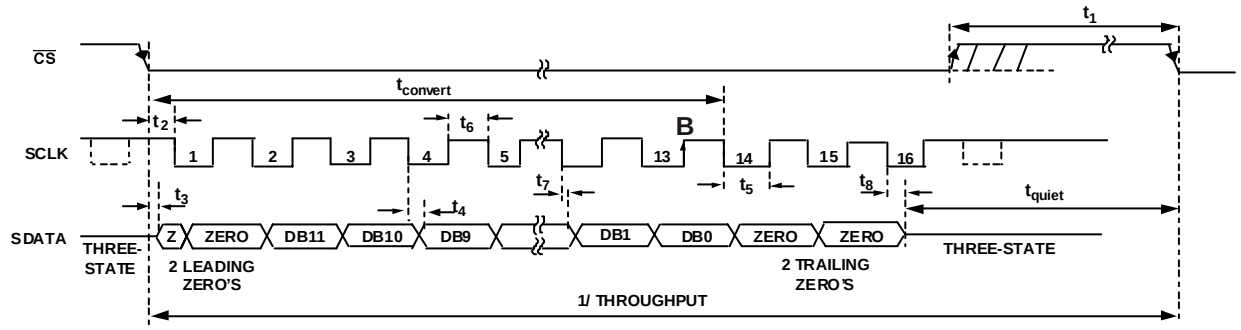


Figure 16. AD7274 Serial Interface Timing Diagram

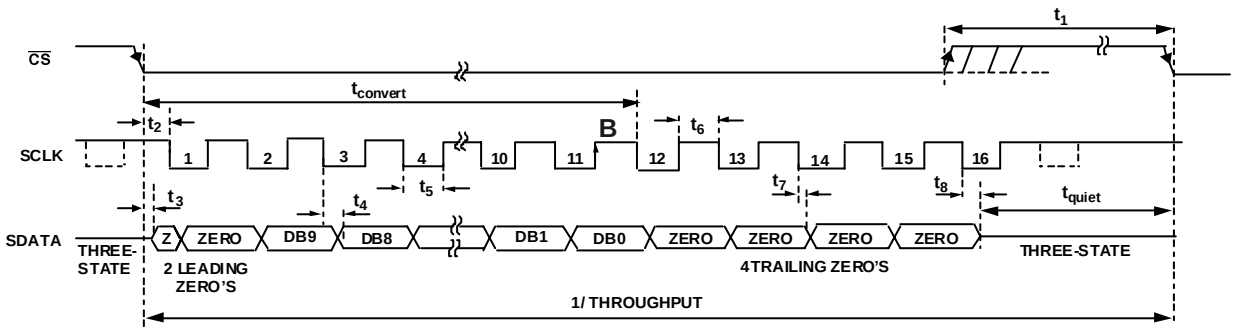
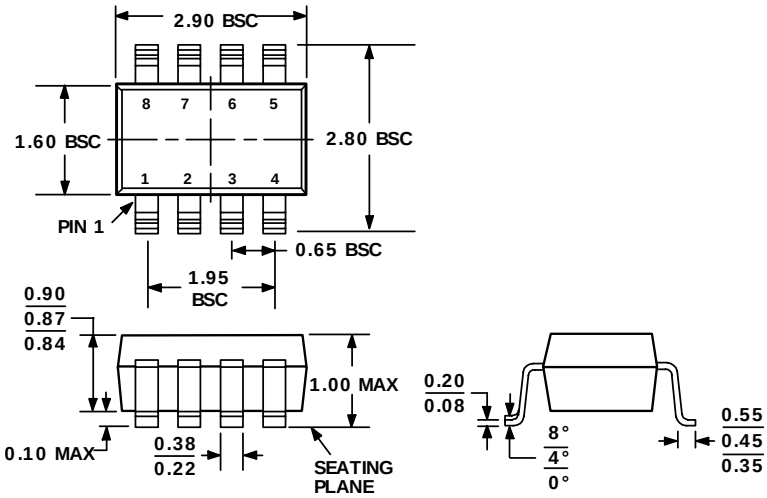


Figure 17. AD7273 Serial Interface Timing Diagram

OUTLINE DIMENSIONS

Dimensions shown in millimiters

8-Lead Thin Small Outline Transistor Package [TSOT]
(UJ- 8)



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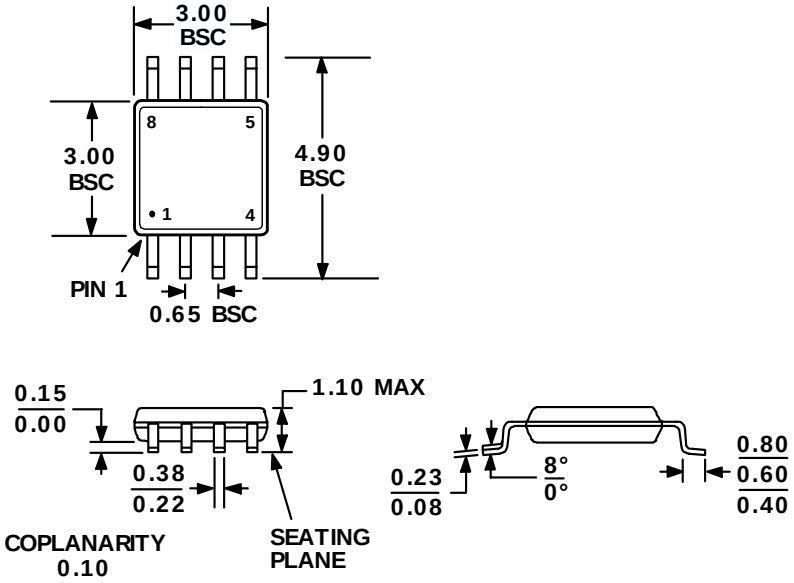
8-Lead Mini Small Outline Package [MSOP]
(RM - 8)



COMPLIANT TO JEDEC STANDARDS MO-187AA