SONY

CXD2422R

CCD Camera Timing Generator

Description

The CXD2422R generates the timing pulses required for driving and signal processing CCDs with 480,000 pixels (EIA, effective pixels) and CCDs with 570,000 pixels (CCIR, effective pixels).

Features

- EIA and CCIR compatible
- Compatible with component digital and composite digital recording format
- Compatible with field/frame accumulation modes

Applications

CCD cameras

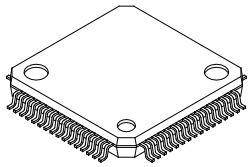
Structure

Silicon gate CMOS IC

Applicable CCD Image Sensors

ICX062/063AL

64 pin LQFP (Plastic)



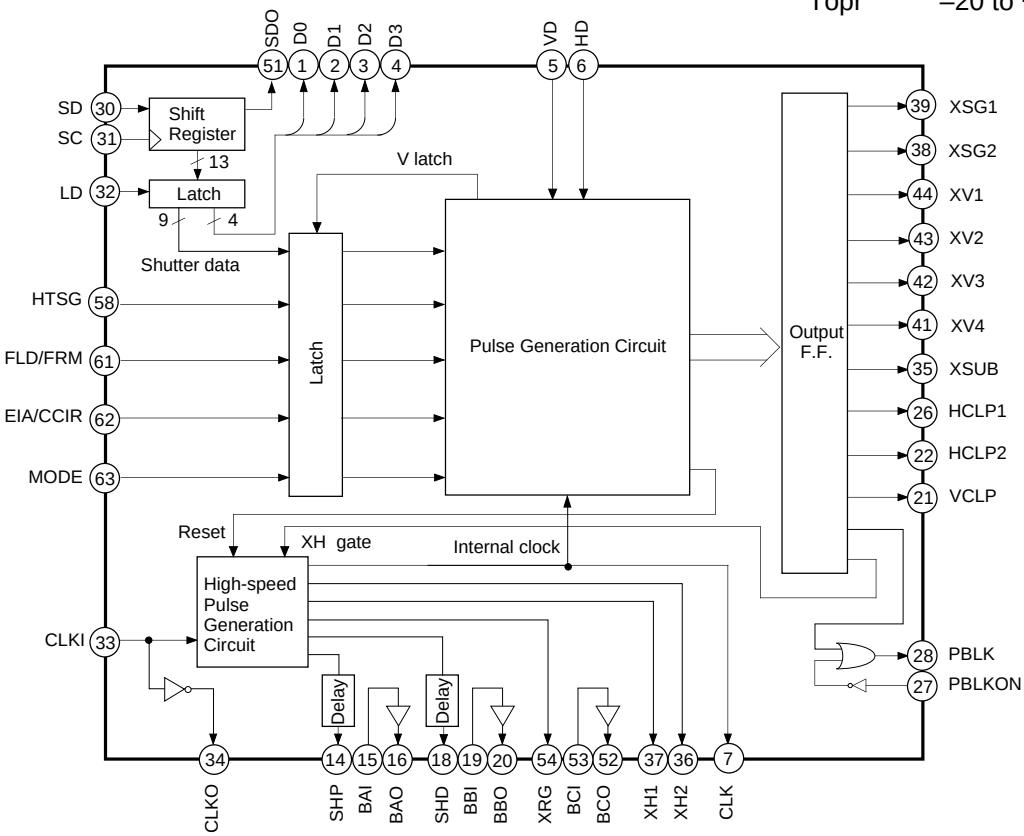
Absolute Maximum Ratings

• Supply voltage	V_{DD}	V_{SS} – 0.5 to +7.0	V
• Input voltage	V_I	V_{SS} – 0.5 to V_{DD} + 0.5	V
• Output voltage	V_O	V_{SS} – 0.5 to V_{DD} + 0.5	V
• Operating temperature			
	Topr	–20 to +75	°C
• Storage temperature			
	Tstg	–55 to +150	°C

Recommended Operating Conditions

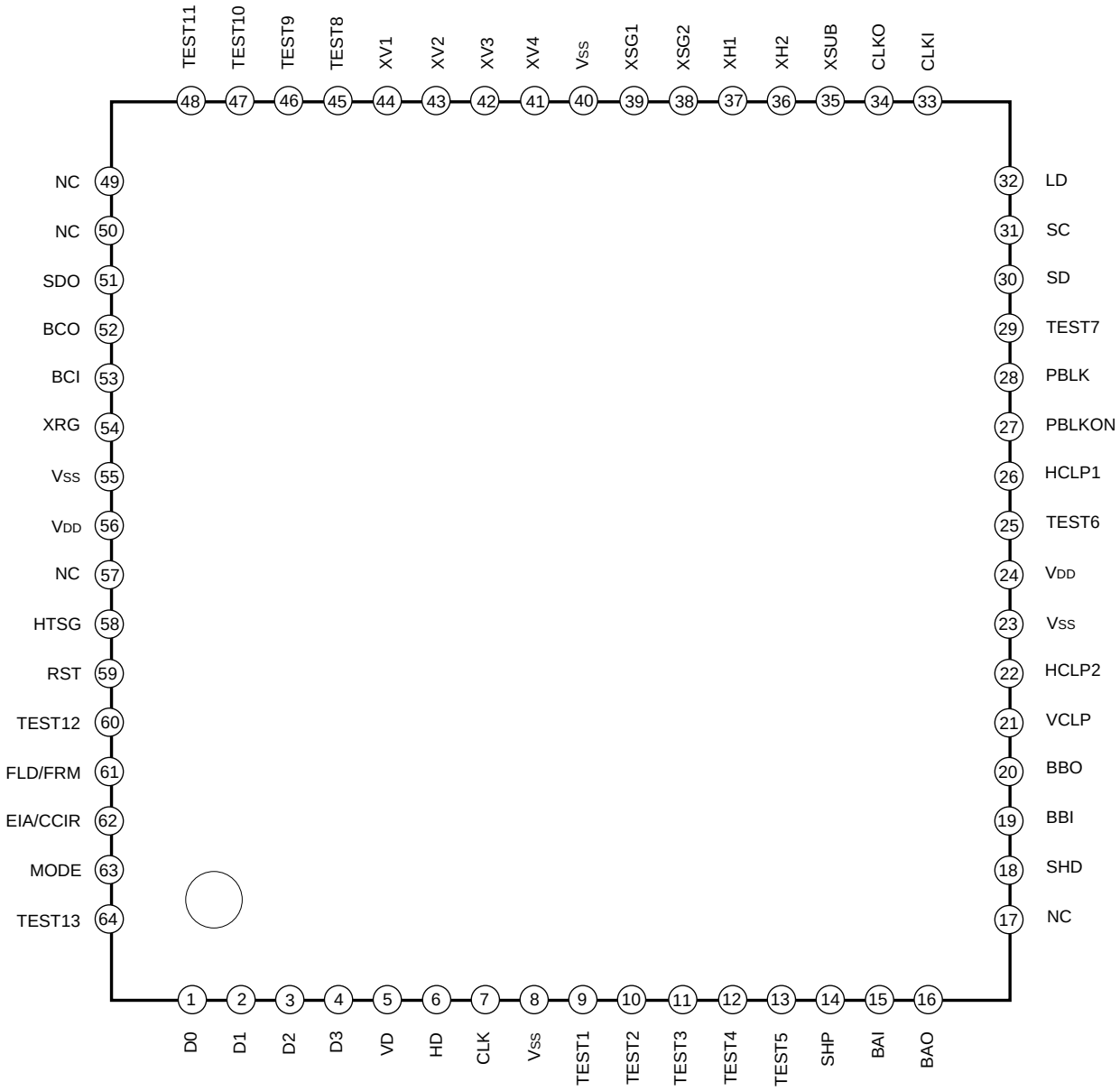
• Supply voltage	V_{DD}	4.5 to 5.5	V
• Operating temperature			
	Topr	–20 to +75	°C

Block Diagram



E94Y30-ST

Pin Configuration



Pin Description

Pin No.	Symbol	I/O	Description
1	D0	O	Extended I/O output.
2	D1	O	Extended I/O output.
3	D2	O	Extended I/O output.
4	D3	O	Extended I/O output.
5	VD	I	Vertical sync signal input. (With pull-up resistor)
6	HD	I	Horizontal sync signal input. (With pull-up resistor)
7	CLK	O	Two frequency divider output of Pin 33.
8	V_{SS}	—	
9	TEST1	I	Test input (normally Low). (With pull-down resistor)
10	TEST2	I	Test input (normally Low). (With pull-down resistor)
11	TEST3	I	Test input (normally Low). (With pull-down resistor)
12	TEST4	I	Test input (normally Low). (With pull-down resistor)
13	TEST5	I	Test input (normally Low). (With pull-down resistor)
14	SHP	O	CCD output precharge level sampling pulse output.
15	BAI	I	Buffer input (for phase adjustment of SHP). (With pull-up resistor)
16	BAO	O	Non-inversed output of BAI.
17	(NC)	—	
18	SHD	O	CCD output signal level sampling pulse output.
19	BBI	I	Buffer input (for phase adjustment of SHD). (With pull-up resistor)
20	BBO	O	Non-inversed output of BBI.
21	VCLP	O	Vertical clamp pulse output.
22	HCLP2	O	Horizontal (dummy bit block) clamp pulse output.
23	V_{SS}	—	
24	V_{DD}	—	
25	TEST6	I	Test input (normally High). (With pull-up resistor)
26	HCLP1	O	Horizontal (OPB block) clamp pulse output.
27	PBLKON	I	Output ON/OFF of PBLK. (High: ON) (With pull-up resistor).
28	PBLK	O	Preblanking pulse output.
29	TEST7	I	Test input (normally High). (With pull-up resistor)
30	SD	I	Serial data input for electronic shutter control. (With pull-up resistor)
31	SC	I	Clock input for electronic shutter control. (With pull-up resistor)
32	LD	I	Latch pulse input for electronic shutter control. (With pull-up resistor)
33	CLKI	I	Clock input.
34	CLKO	O	Inversed output of CLKI.
35	XSUB	O	Substrate pulse output for electronic shutter.
36	XH2	O	Clock output for horizontal register drive.
37	XH1	O	Clock output for horizontal register drive.

Pin No.	Symbol	I/O	Description
38	XSG2	O	Sensor charge readout pulse output.
39	XSG1	O	Sensor charge readout pulse output.
40	V_{SS}	—	
41	XV4	O	Clock output for vertical register drive.
42	XV3	O	Clock output for vertical register drive.
43	XV2	O	Clock output for vertical register drive.
44	XV1	O	Clock output for vertical register drive.
45	TEST8	O	Test output (normally open).
46	TEST9	O	Test output (normally open).
47	TEST10	O	Test output (normally open).
48	TEST11	O	Test output (normally open).
49	(NC)	—	
50	(NC)	—	
51	SDO	O	Serial data output for electronic shutter control.
52	BCO	O	Non-inversed output of BCI.
53	BCI	I	Buffer input (for phase adjustment of XRG). (With pull-up resistor)
54	XRG	O	Reset gate pulse output of output block.
55	V_{SS}	—	
56	V_{DD}	—	
57	(NC)	—	
58	HTSG	I	Readout pulse (XSG1, 2) ON/OFF. (High: OFF) (With pull-down resistor)
59	RST	I	Test input (normally High). (With pull-up resistor)
60	TEST12	I	Test input (normally Low). (With pull-up resistor)
61	FLD/FRM	I	High: Field accumulation mode, Low: Frame accumulation mode. (With pull-up resistor)
62	EIA/CCIR	I	High: EIA, Low: CCIR. (With pull-up resistor)
63	MODE	I	High: Component digital mode, Low: Composite digital mode. (With pull-up resistor)
64	TEST13	I	Test input (normally Low). (With pull-up resistor)

Note) TEST12 and TEST13 have a built-in pull-up resistor.
Be sure to fix them at Low.

Electrical Characteristics

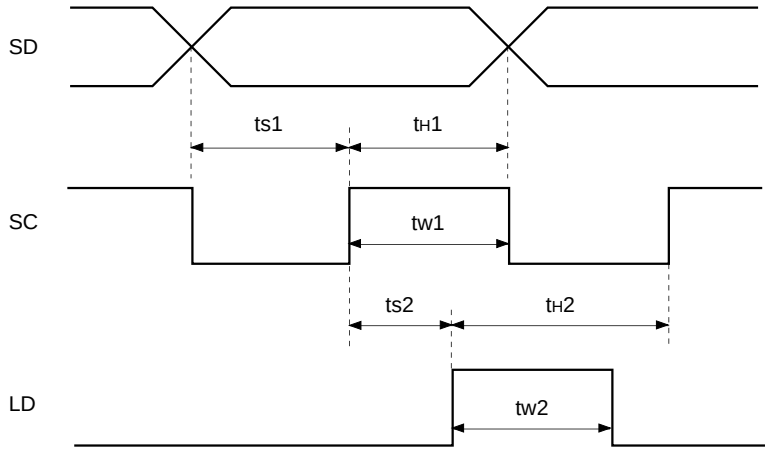
1) DC characteristics

(V_{DD} = 4.5 to 5.5V, Topr = –20 to +75°C)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Supply voltage	V_{DD}		4.5	5.0	5.5	V
Input/Output voltages	V_I, V_O		V_{SS}		V_{DD}	V
Input voltage	V_{IH}		0.7V_{DD}			V
	V_{IL}				0.3V_{DD}	V
Output voltage	V_{OH}	I_{OH} = –2mA	V_{DD} – 0.8			V
	V_{OL}	I_{OL} = 4mA			0.4	V
Pull-up/ Pull-down resistors	R_{PU}, R_{PD}	V_{IL} = 0V, V_{IH} = V_{DD}	40k	100k	250k	Ω

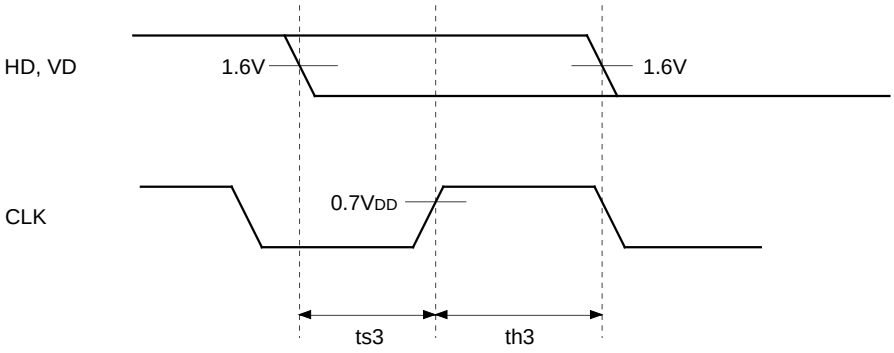
2) AC characteristics

2)-1. Pulses for electronic shutter control (SD, SC, LD)



Symbol	Item	Min.
ts1	SD set-up time, activated by the rising edge of SC	20ns
tH1	SD hold time, activated by the rising edge of SC	20ns
tw1	SC pulse width	20ns
ts2	SC set-up time, activated by the rising edge of LD	20ns
tH2	SC hold time, activated by the rising edge of LD	20ns
tw2	LD pulse width	20ns

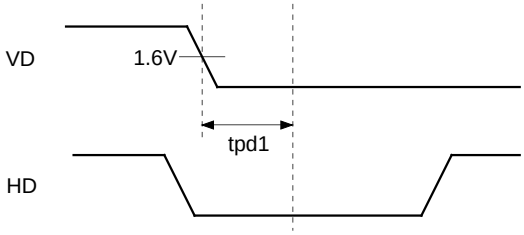
2)-2. HD/VD take-in characteristics



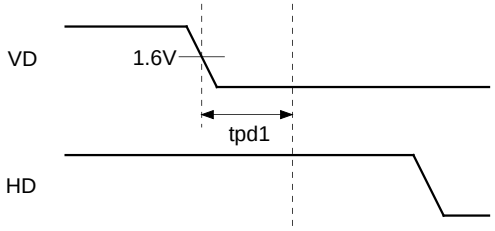
(V_{DD} = 4.5 to 5.5V, Topr = –20 to +75°C)

Symbol	Definition	Min.	Typ.	Max.	Unit
ts3	HD/VD set-up time, activated by CLK	4			ns
th3	HD/VD hold time, activated by CLK	0			ns

2)-3. Field discrimination characteristics



When the HD logic level is Low tpd1 after VD falls, the field is discriminated as an ODD (EVEN with CCIR) field.

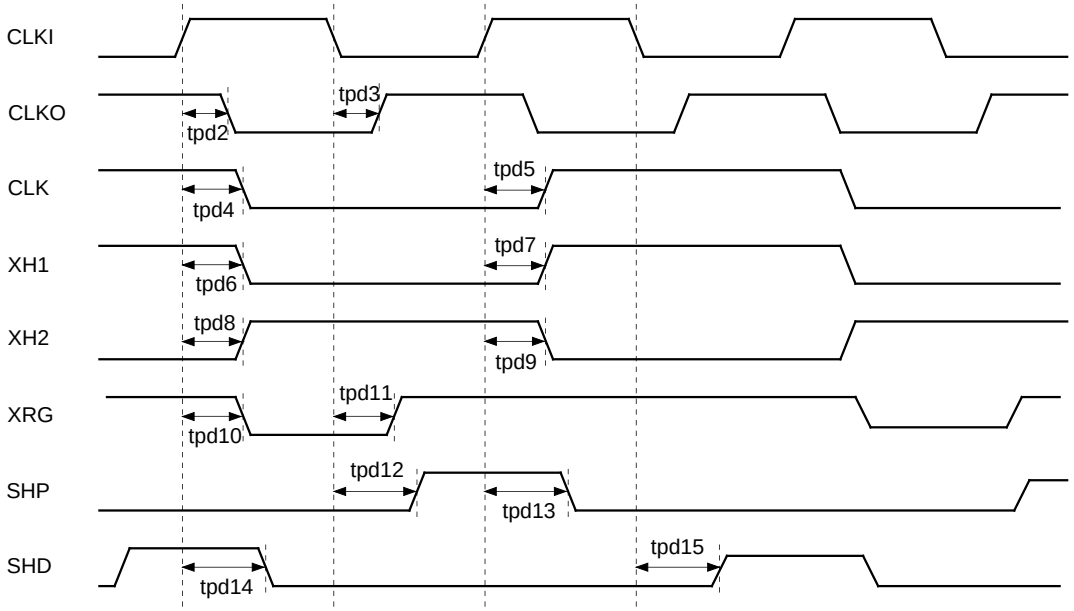


When the HD logic level is High tpd1 after VD falls, the field is discriminated as an EVEN (ODD with CCIR) field.

(V_{DD} = 4.5 to 5.5V, Topr = –20 to +75°C)

Symbol	Definition	Min.	Typ.	Max.	Unit
tpd1	Field discriminating clock phase, activated by the falling edge of VD	890			ns

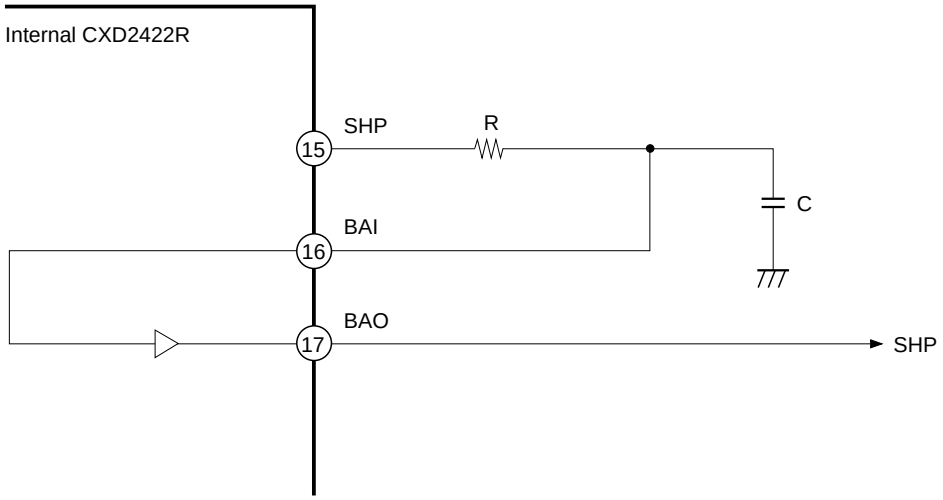
2)-4. CLKO, CLK, XH1, XH2, XRG, SHP, SHD phase characteristics



(V_{DD} = 4.5 to 5.5V, Topr = –20 to +75°C, load capacitance = 10pF)

Symbol	Definition	Min.	Typ.	Max.	Unit
tpd2	CLKO falling delay time against CLKI	3.5	6.2	12.1	ns
tpd3	CLKO rising delay time against CLKI	4.0	7.2	14.1	ns
tpd4	CLK2 falling delay time against CLKI	5.2	9.3	18.3	ns
tpd5	CLK2 rising delay time against CLKI	6.5	11.6	22.8	ns
tpd6	XH1 falling delay time against CLKI	5.2	8.8	17.2	ns
tpd7	XH1 rising delay time against CLKI	6.4	11.4	22.4	ns
tpd8	XH2 rising delay time against CLKI	5.7	10.2	20.3	ns
tpd9	XH2 falling delay time against CLKI	5.3	9.4	18.5	ns
tpd10	XRG falling delay time against CLKI	4.7	8.4	16.5	ns
tpd11	XRG rising delay time against CLKI	5.2	9.2	18.1	ns
tpd12	SHP rising delay time against CLKI	8.1	14.4	28.3	ns
tpd13	SHP falling delay time against CLKI	7.9	14.1	27.6	ns
tpd14	SHD falling delay time against CLKI	7.9	14.1	27.6	ns
tpd15	SHD rising delay time against CLKI	8.6	15.2	29.8	ns

Phases of SHP, SHD, and XRG pulses can be adjusted using on-chip buffers.



Delay times of SHP, SHD, and XRG can be adjusted with C and R.

Delay characteristics of on-chip buffers (V_{DD} = 4.5 to 5.5V, Topr = –20 to +75°C, load capacitance = 10pF)

Symbol	Definition	Min.	Typ.	Max.	Unit
tpd16	Rising delay time from BAI to BAO	4.0	7.1	13.9	ns
tpd17	Falling delay time from BAI to BAO	2.8	5.5	10.7	ns
tpd18	Rising delay time from BBI to BBO	4.0	7.0	13.8	ns
tpd19	Falling delay time from BBI to BBO	3.0	5.4	10.7	ns
tpd20	Rising delay time from BCI to BCO	4.3	7.6	15.0	ns
tpd21	Falling delay time from BCI to BCO	3.4	6.0	11.7	ns

3) I/O pin capacitances (V_{DD} = V_I = 0V, f = 1MHz)

Item	Symbol	Min.	Typ.	Max.	Unit
Input pin capacitance	C_{IN}			9	pF
Output pin capacitance	C_{OUT}			11	pF

Description of Operation

1) Mode setting

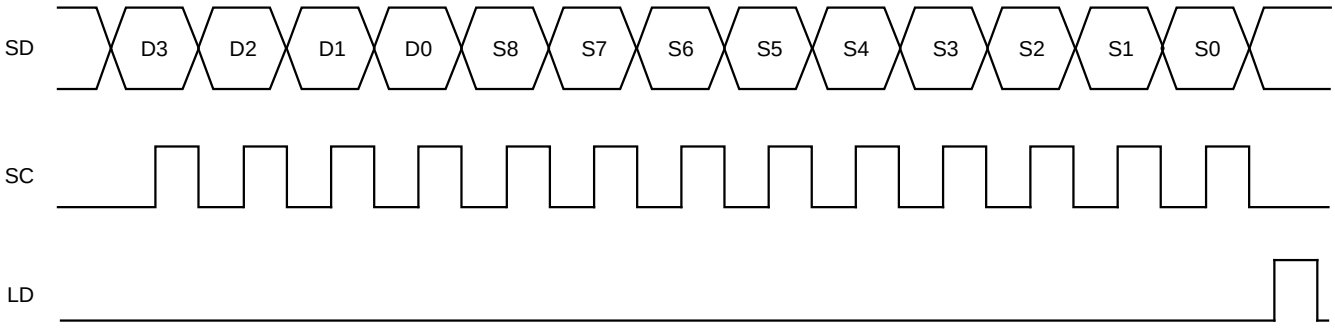
Symbol	Pin No.	Low	High
EIA/CCIR	62	CCIR	EIA
MODE	63	Composite digital mode Clock (CLKI) input EIA 35.79545MHz (2275fH = 10fsc) CCIR 35.46895MHz (2270+8/625fH = 8fsc)	Component digital mode Clock (CLKI) input EIA 36MHz (2288fH) CCIR 36MHz (2304fH)
FLD/FRM	61	Frame accumulation	Field accumulation
HTSG	58	XSG1 and XSG2 pulses are output.	XSG1 and XSG2 pulses are fixed at High. (Readout suspended)
PBLKON	27	PBLK is fixed at High.	PBLK pulse is output.

2) Inputting serial data

The accumulation time of the electronic shutter is controlled by external serial data.
Input pins (SD, SC, and LD) are used to input serial data.

SD: Serial data input
SC: Clock input
LD: Latch pulse input

The following is the serial data timing chart.

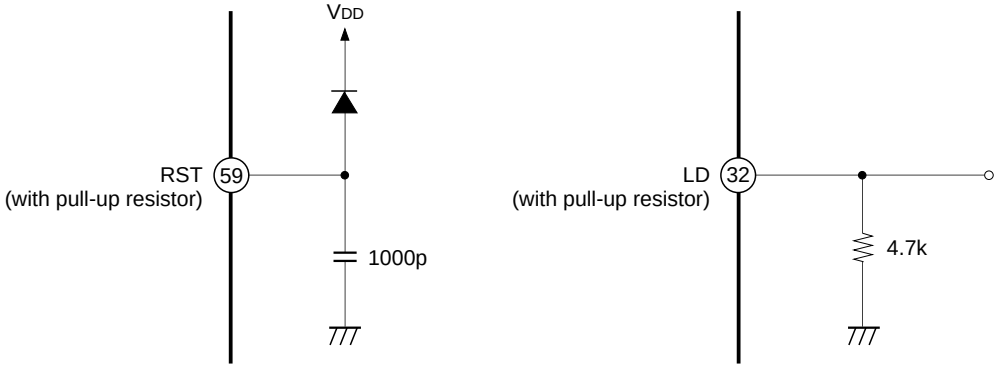


D3 to D0: Not related to the accumulation time of the electronic shutter. Data are output to D3 to D0 pins after converted into parallel data and being latched at LD.

S8 to S0: Sdata is set in 9-bit binary with S8 as MSB (High: 1, Low: 0). ON/OFF of the electronic shutter and the accumulation time are determined by Sdata.
The calculation on the next page is for the accumulation time in each mode.

The data for SD are input to the internal 13-bit shift register, and the data can be retrieved as serial data at SDO pin.

Note) The electronic shutter might operate from turning power on to inputting serial data. To prevent this operation, process RST and LD pins as shown in the following figures. Be careful, however, as serial data cannot be received before the voltage at RST rises.



Accumulation time of electronic shutter

EIA/ CCIR	Sdata	Accumulation time (s)
EIA	0 to 261	{(261 – Sdata)/15734} + 1/25678 (Component digital mode) {(261 – Sdata)/15734} + 1/25532 (Composite digital mode)
	262	Input prohibited
	263 to 511	Electronic shutter OFF
CCIR	0 to 311	{(311 – Sdata)/15625} + 1/25678 (Component digital mode) {(311 – Sdata)/15625} + 1/25299 (Composite digital mode)
	312	Input prohibited
	313 to 511	Electronic shutter OFF

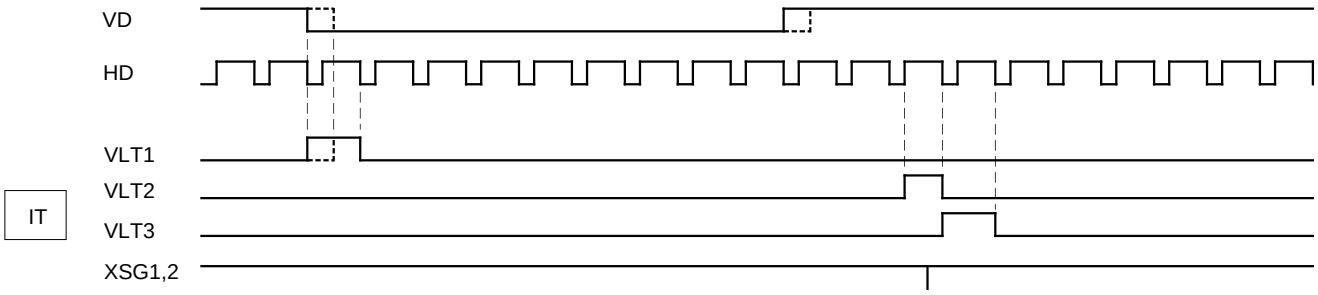
The Sdata values corresponding to representative shutter speeds are listed below.

Shutter speed	Sdata	
	EIA	CCIR
1/100	104 (068h)	155 (09Bh)
1/125	136 (088h)	187 (0BBh)
1/250	199 (0C7h)	249 (0F9h)
1/500	230 (0E6h)	280 (118h)
1/1000	246 (0F6h)	296 (128h)
1/2000	254 (0FEh)	304 (130h)

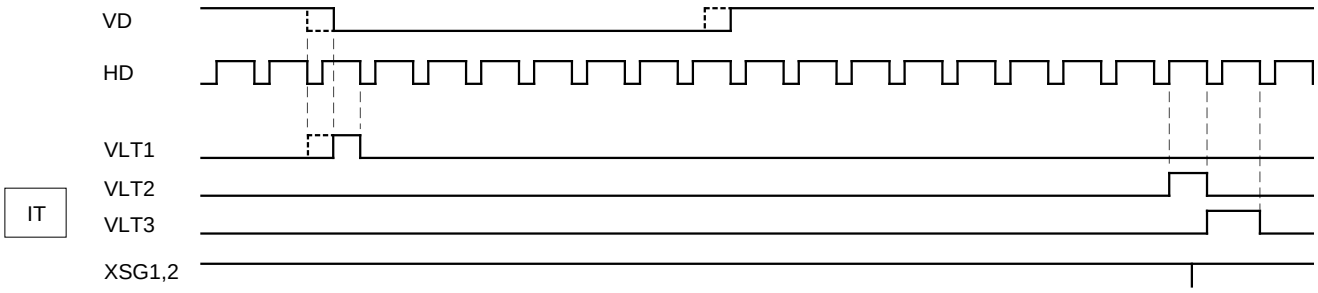
3) Latch pulse timing

Various mode switchings and shutter data are taken in by field. The latch pulse timing is as follows (The broken lines show timing in the EVEN FIELD.):

EIA

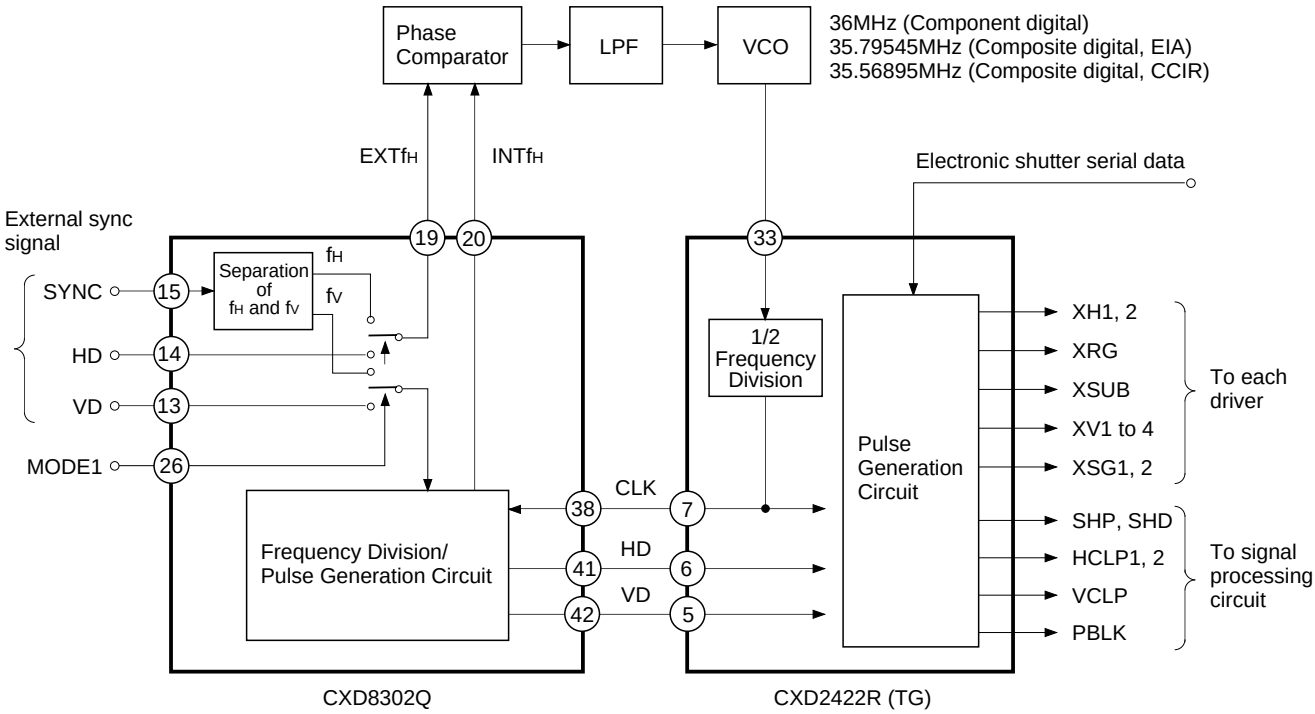


CCIR



Latch pulse	Latched data
VLT1	EIA/CCIR, MODE, HTSG
VLT2	Shutter data (S8 to S0)
VLT3	FLD/FRM

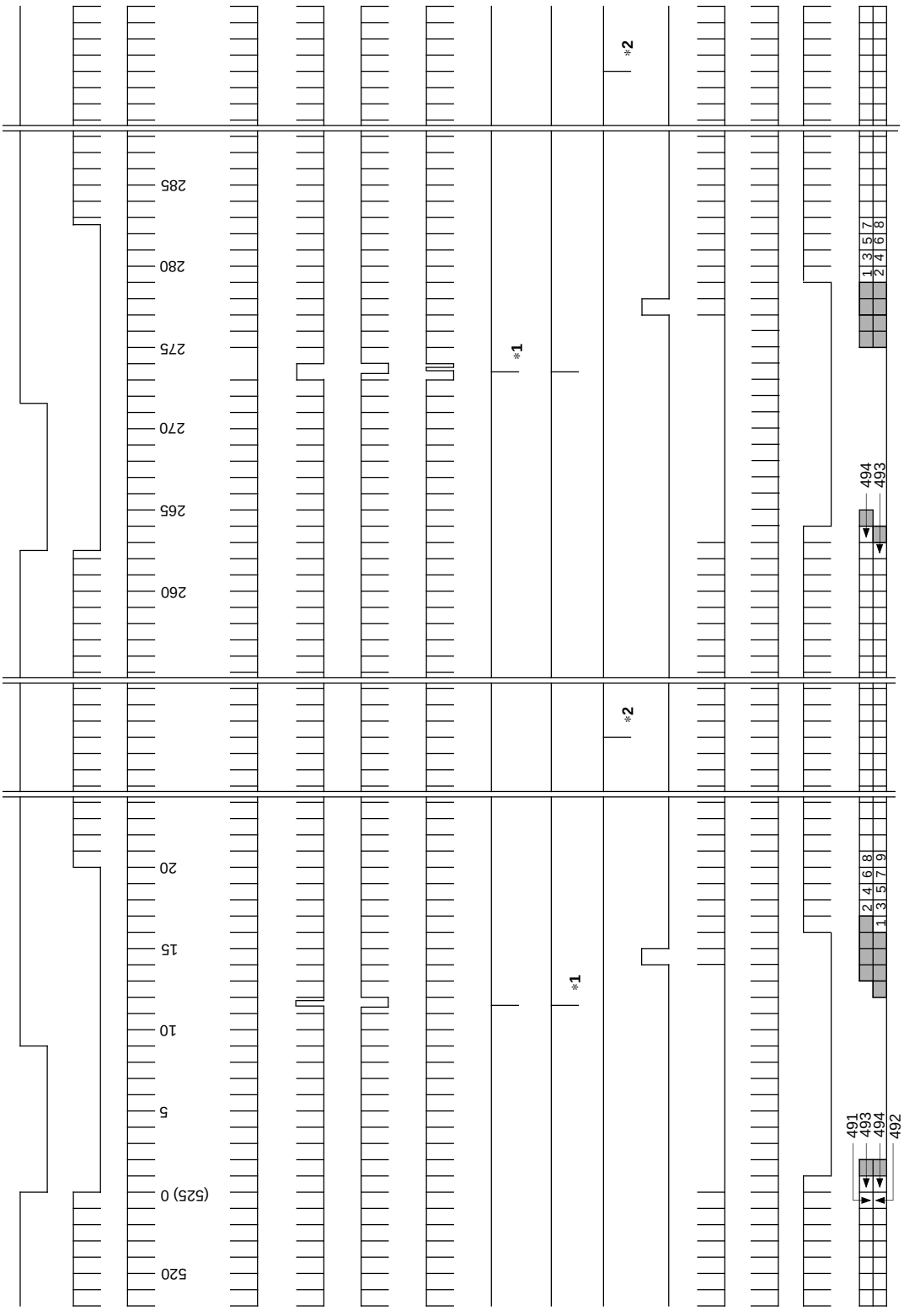
Example of System Configuration



Note) 1. Either SYNC or VD/HD is used as external sync signal. When SYNC is used (SYNC synchronous mode), fix MODE1 to High; when VD/HD is used (VD/HD Synchronous mode), fix MODE1 to Low.

2. Be sure to do phase comparison of the falling edge of EXTfH and INTfH for SYNC synchronous mode.

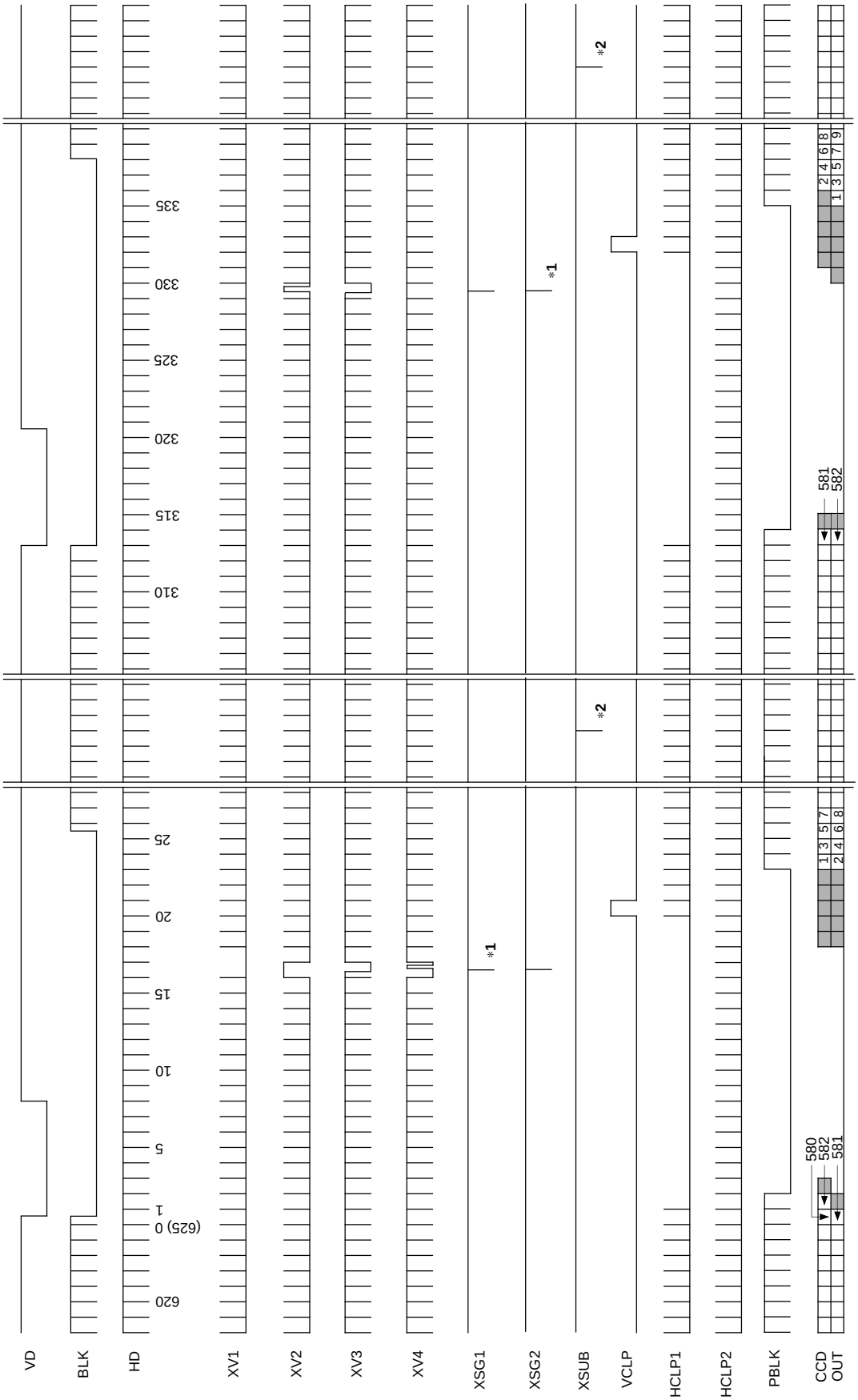
Timing Chart (1) EIA vertical direction



*1 These pulses are not output during frame accumulation.

*2 These pulses are output at the position determined by shutter data.

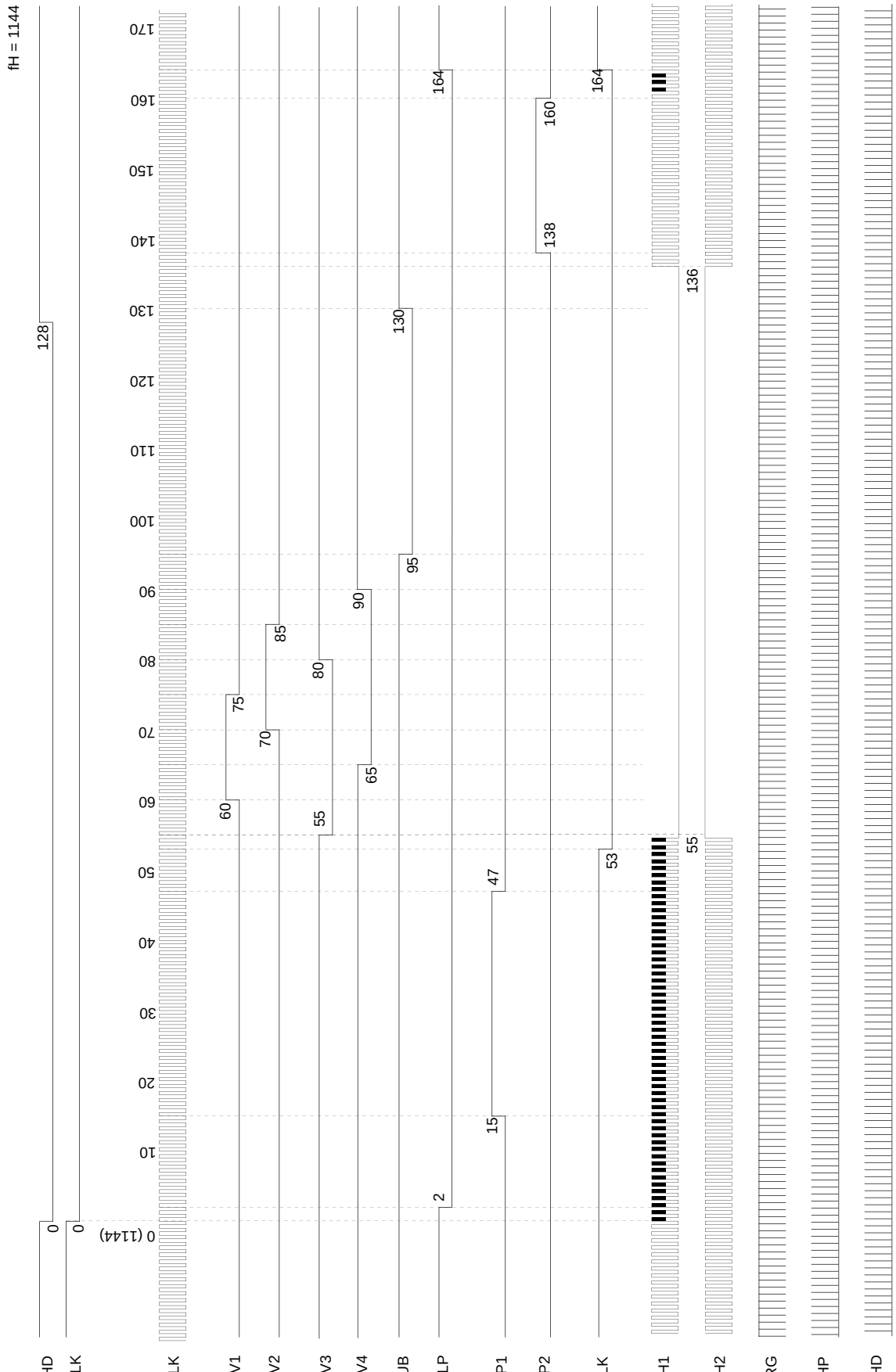
Timing Chart (2) CCIR vertical direction



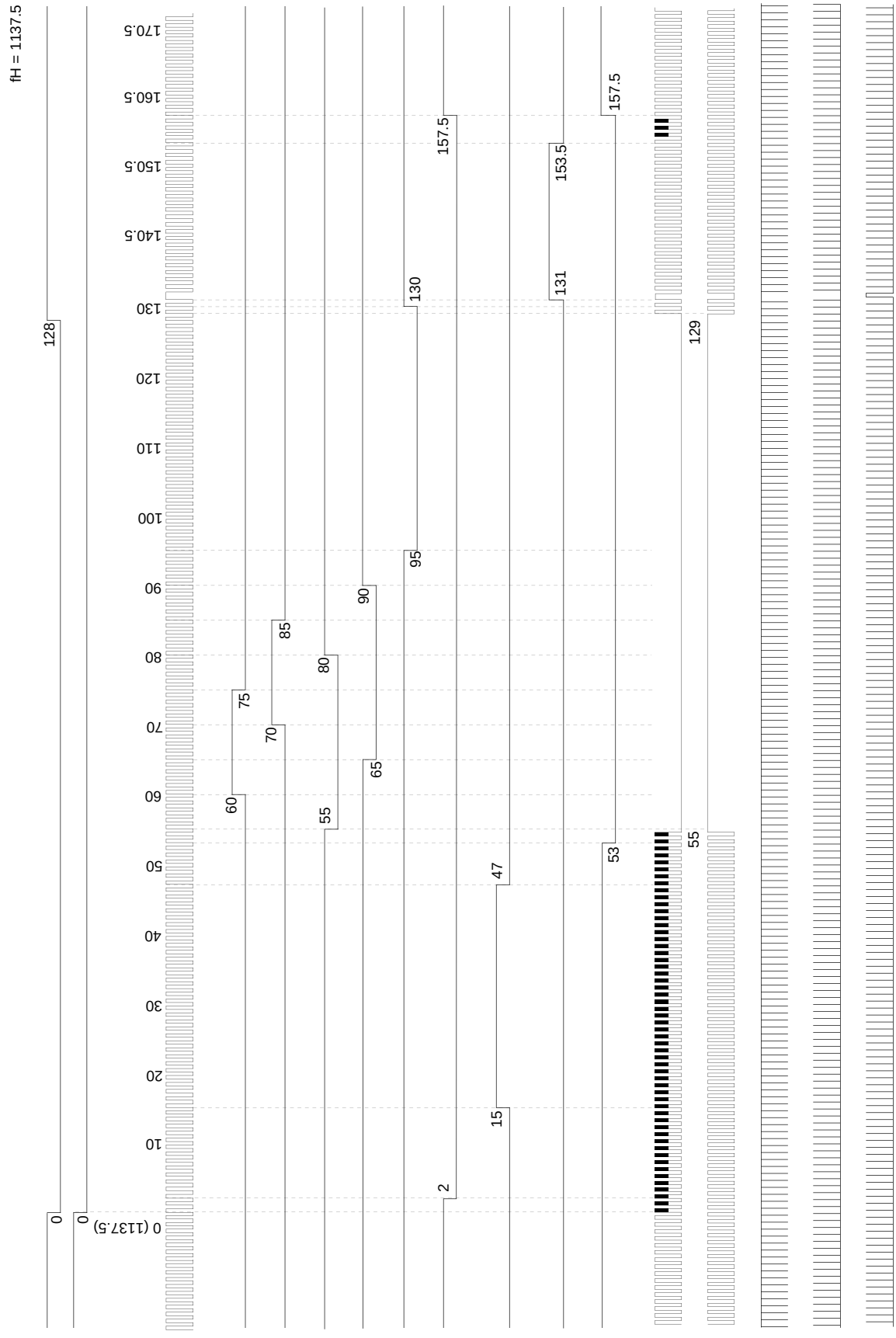
*1 These pulses are not output during frame accumulation.

*2 These pulses are output at the position determined by shutter data.

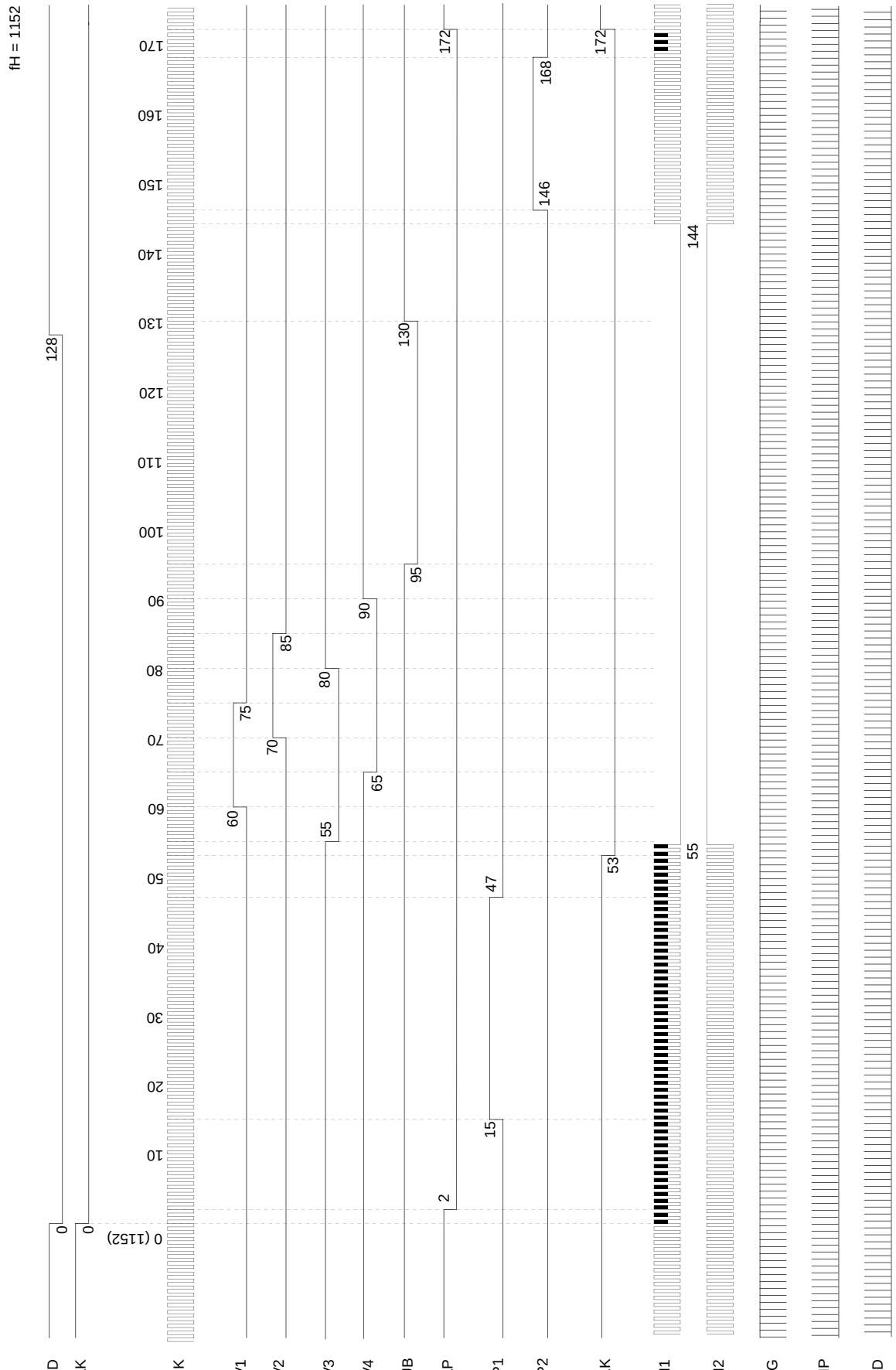
Timing Chart (3) EIA horizontal direction, Component digital mode



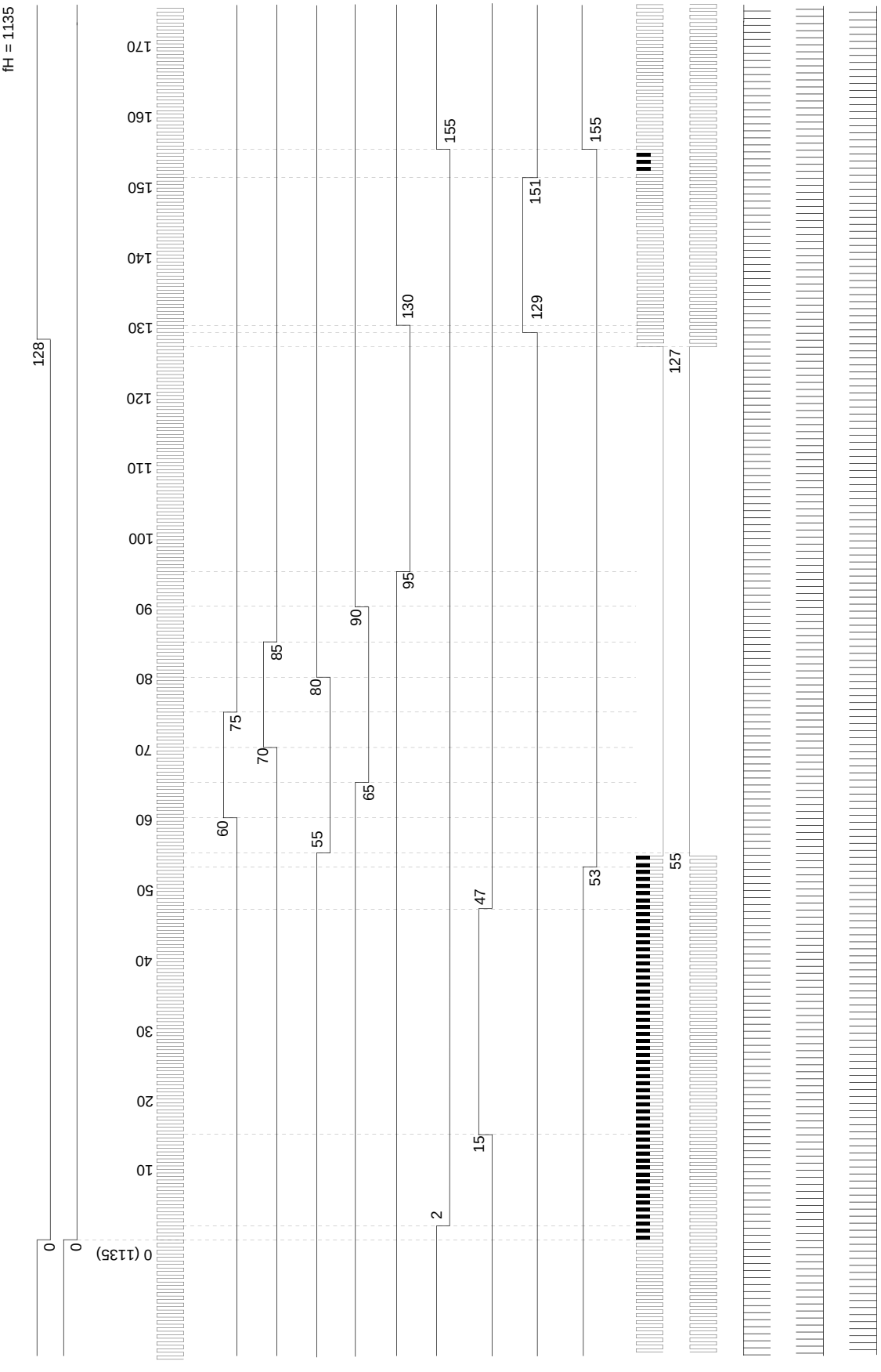
Timing Chart (4) EIA horizontal direction, Composite digital mode



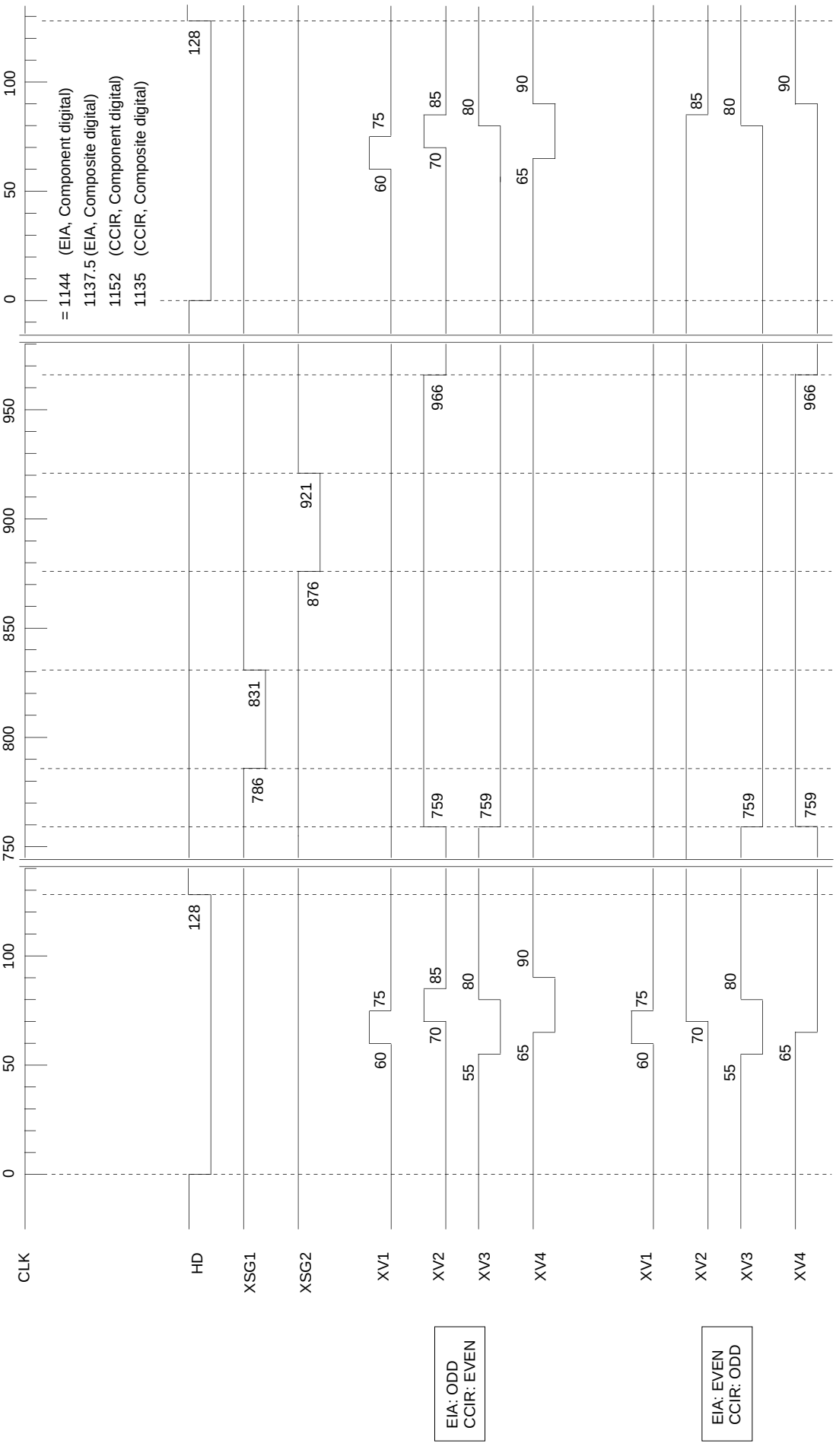
Timing Chart (5) CCIR horizontal direction, Component digital mode



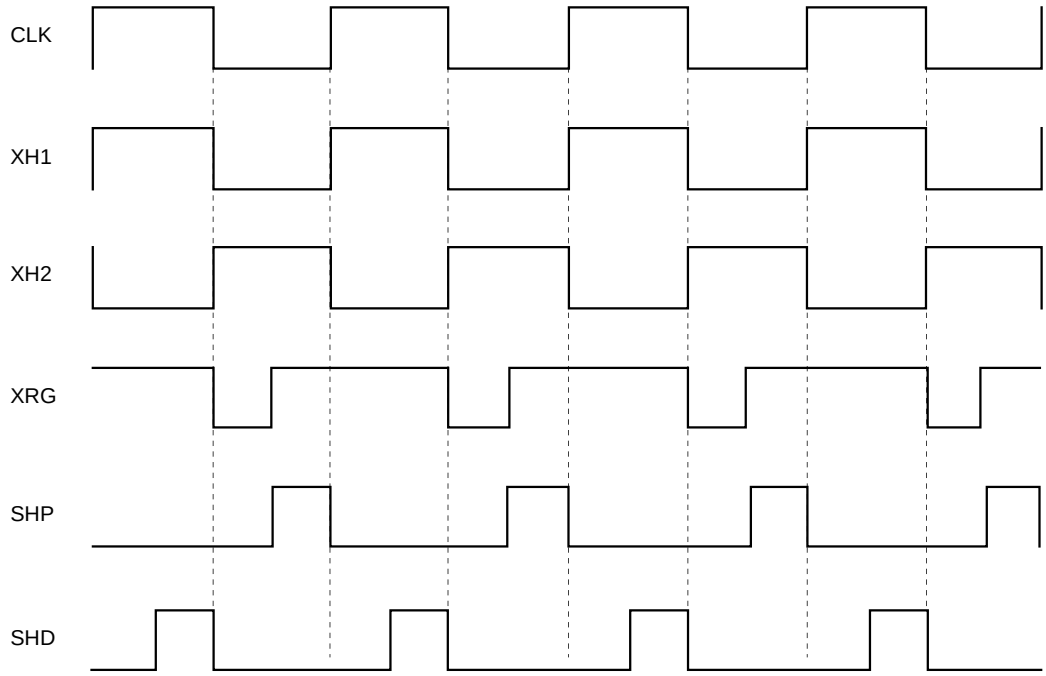
Timing Chart (6) CCIR horizontal direction, Composite digital mode



Timing Chart (7) Readout interval

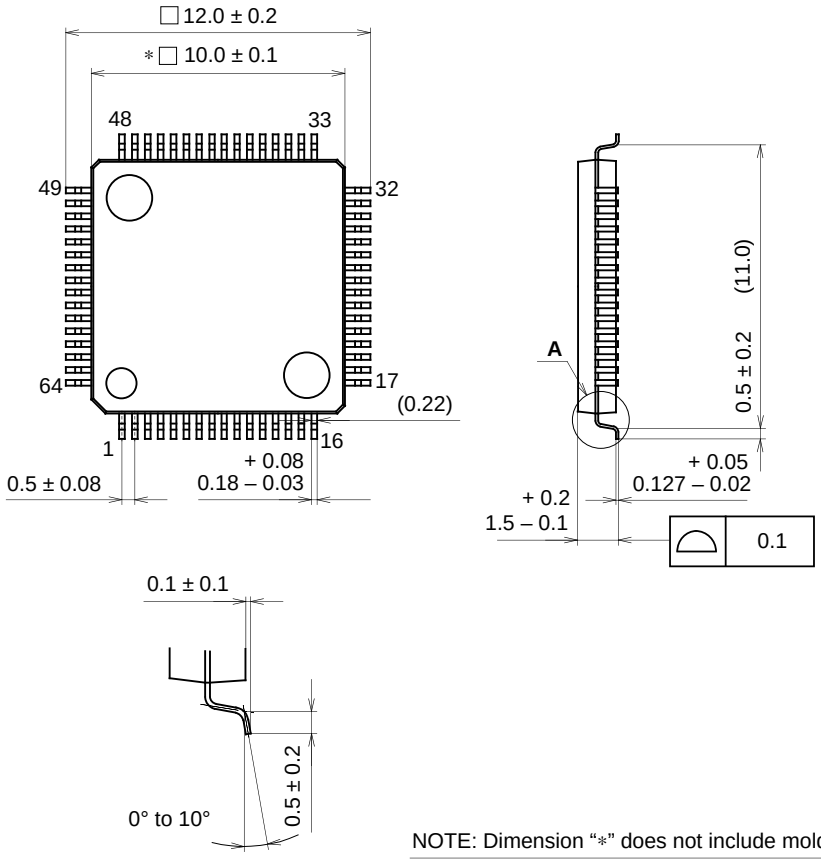


Timing Chart (8) High-speed pulse timing



Package Outline Unit: mm

64PIN LQFP (PLASTIC)



DETAIL **A**

NOTE: Dimension "∗" does not include mold protrusion.

SONY CODE	LQFP-64P-L01
EIAJ CODE	∗QFP064-P-1010-A
JEDEC CODE	————

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY / PHENOL RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42 ALLOY
PACKAGE WEIGHT	0.3g