

**SWITCHING
N-CHANNEL POWER MOS FET
INDUSTRIAL USE**

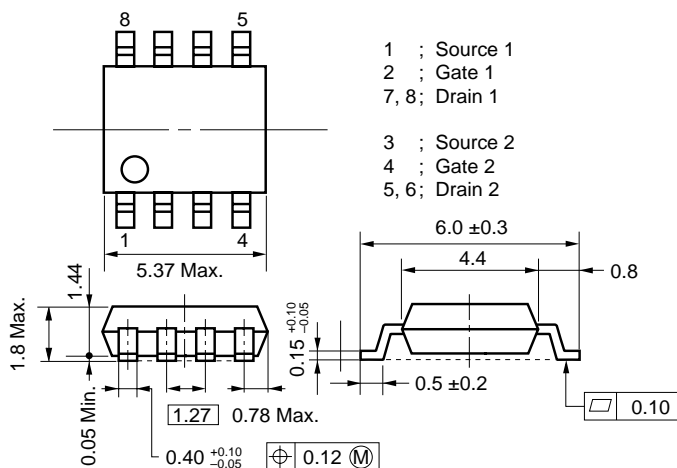
DESCRIPTION

This product is Dual N-channel MOS Field Effect Transistor designed for DC/DC converters and power management applications of notebook computers.

FEATURES

- Dual chip type
- Low on-resistance
 $R_{DS(on)1} = 32 \text{ m}\Omega \text{ MAX. (} V_{GS} = 10 \text{ V, } I_D = 3.5 \text{ A)}$
 $R_{DS(on)2} = 45 \text{ m}\Omega \text{ MAX. (} V_{GS} = 4.5 \text{ V, } I_D = 3.5 \text{ A)}$
- Low input capacitance $C_{iss} = 895 \text{ pF TYP.}$
- Built-in G-S protection diode
- Small and surface mount package (Power SOP8)

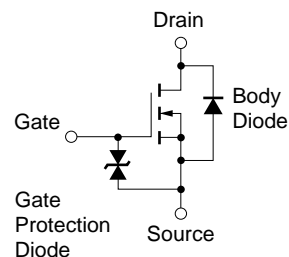
PACKAGE DRAWING (Unit : mm)



ORDERING INFORMATION

PART NUMBER	PACKAGE
μ PA1755G	Power SOP8

**EQUIVALENT CIRCUIT
(1/2 Circuit)**



ABSOLUTE MAXIMUM RATINGS ($T_A = 25 \text{ }^\circ\text{C}$, All terminals are connected.)

Drain to Source Voltage ($V_{GS} = 0$)	V_{DSS}	30	V
Gate to Source Voltage ($V_{DS} = 0$)	V_{GSS}	± 20	V
Drain Current (DC)	$I_{D(DC)}$	± 7.0	A
Drain Current (pulse) ^{Note1}	$I_{D(pulse)}$	± 28	A
Total Power Dissipation (1 unit) ^{Note2}	P_T	1.7	W
Total Power Dissipation (2 unit) ^{Note2}	P_T	2.0	W
Channel Temperature	T_{ch}	150	$^\circ\text{C}$
Storage Temperature	T_{stg}	-55 to + 150	$^\circ\text{C}$

- Notes**
1. $PW \leq 10 \mu\text{s}$, Duty cycle $\leq 1 \%$
 2. $T_A = 25 \text{ }^\circ\text{C}$, Mounted on ceramic substrate of $2000 \text{ mm}^2 \times 1.1 \text{ mm}$

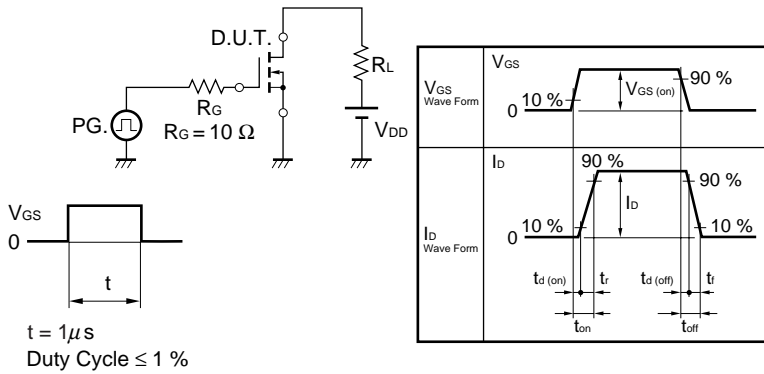
Remark The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

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 Not all devices/types available in every country. Please check with local NEC representative for availability and additional information.

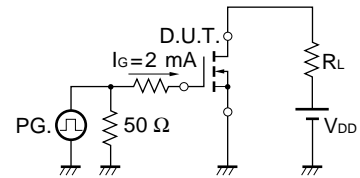
ELECTRICAL CHARACTERISTICS (T_A = 25 °C, All terminals are connected.)

CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Drain to Source On-state Resistance	R _{DS(on)1}	V _{GS} = 10 V, I _D = 3.5 A		22	32	mΩ
	R _{DS(on)2}	V _{GS} = 4.5 V, I _D = 3.5 A		32	45	mΩ
Gate to Source Cut-off Voltage	V _{GS(off)}	V _{DS} = 10 V, I _D = 1 mA	1.5	2.0	2.5	V
Forward Transfer Admittance	y _{fs}	V _{DS} = 10 V, I _D = 3.5 A	4.0	8.0		S
Drain Leakage Current	I _{DSS}	V _{DS} = 30 V, V _{GS} = 0			10	μA
Gate to Source Leakage Current	I _{GSS}	V _{GS} = ±20 V, V _{DS} = 0			±10	μA
Input Capacitance	C _{iss}	V _{DS} = 10 V		895		pF
Output Capacitance	C _{oss}	V _{GS} = 0		335		pF
Reverse Transfer Capacitance	C _{rss}	f = 1 MHz		150		pF
Turn-on Delay Time	t _{d(on)}	I _D = 3.5 A		16		ns
Rise Time	t _r	V _{GS(on)} = 10 V		130		ns
Turn-off Delay Time	t _{d(off)}	V _{DD} = 15 V		55		ns
Fall Time	t _f	R _G = 10 Ω		30		ns
Total Gate Charge	Q _G	I _D = 7.0 A		19		nC
Gate to Source Charge	Q _{GS}	V _{DD} = 24 V		2.2		nC
Gate to Drain Charge	Q _{GD}	V _{GS} = 10 V		5.4		nC
Body Diode forward Voltage	V _{F(S-D)}	I _F = 7.0 A, V _{GS} = 0		0.8		V
Reverse Recovery Time	t _{rr}	I _F = 7.0 A, V _{GS} = 0		45		ns
Reverse Recovery Charge	Q _{rr}	di/dt = 100 A/μs		62		nC

TEST CIRCUIT 1 SWITCHING TIME

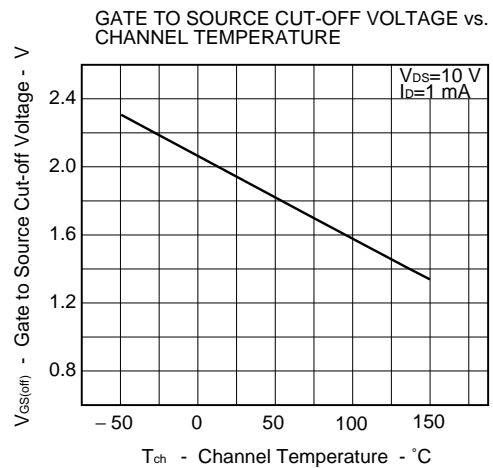
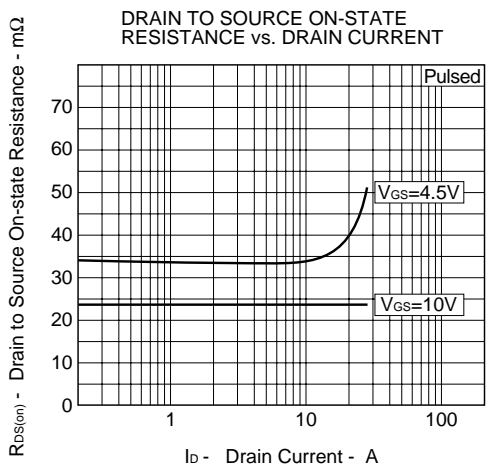
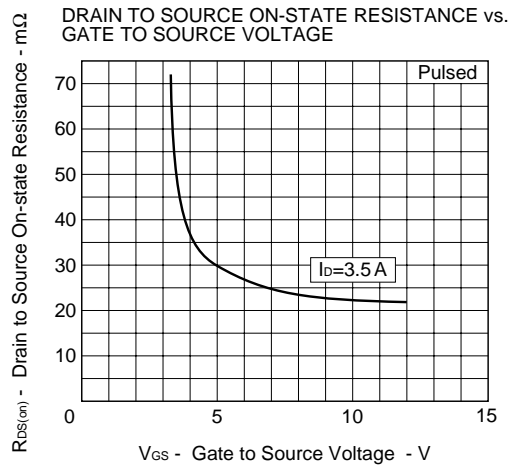
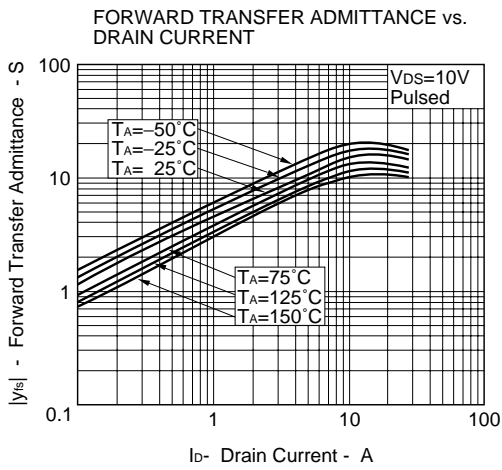
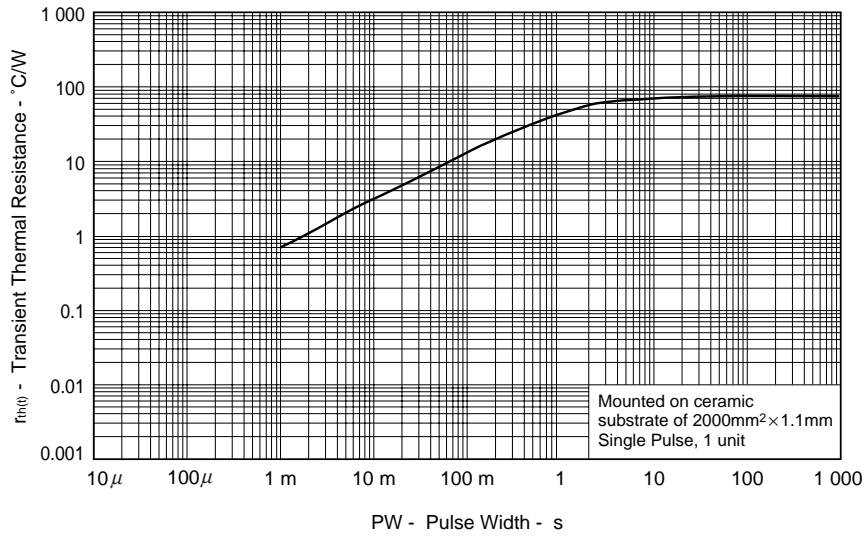


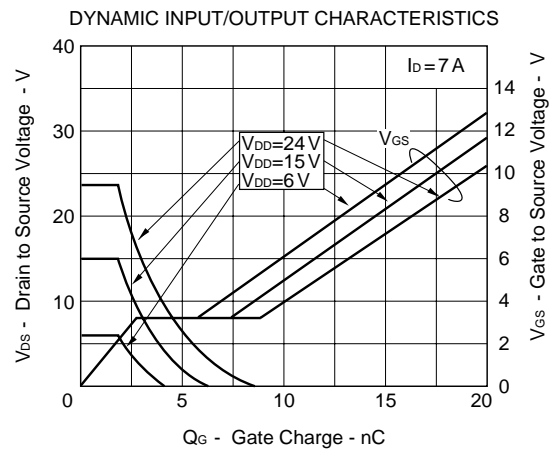
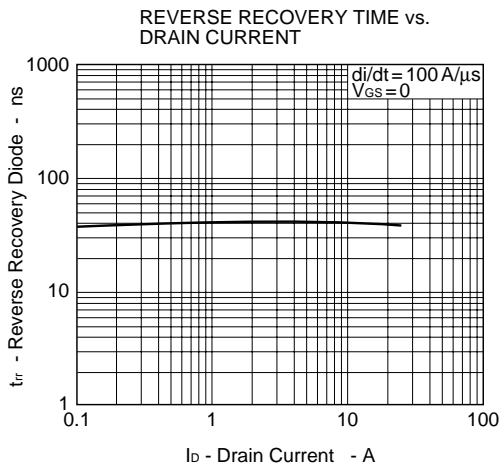
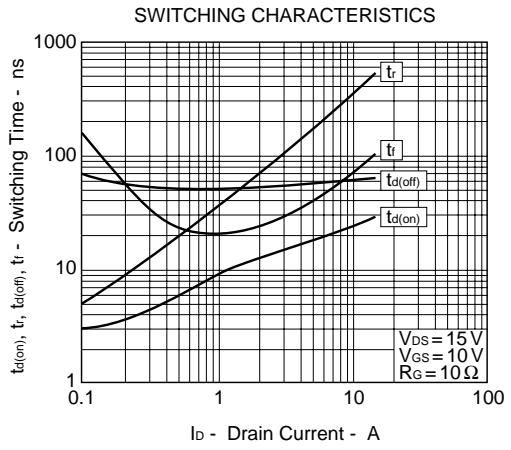
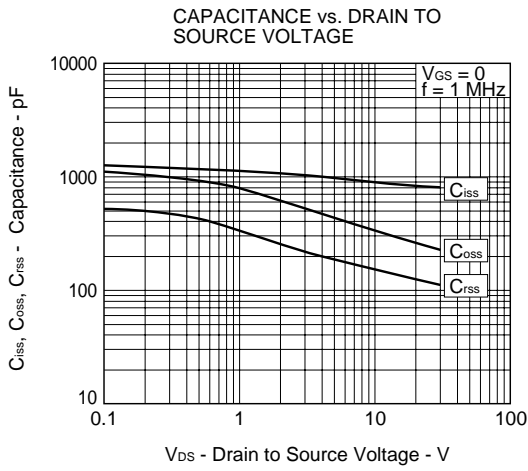
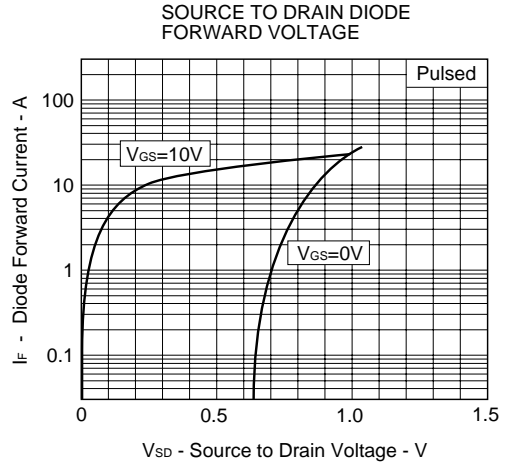
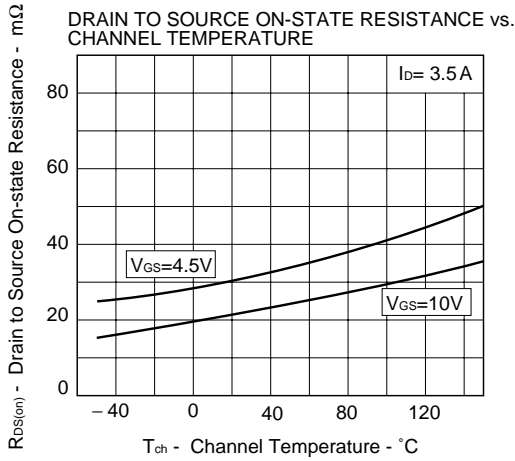
TEST CIRCUIT 2 GATE CHARGE

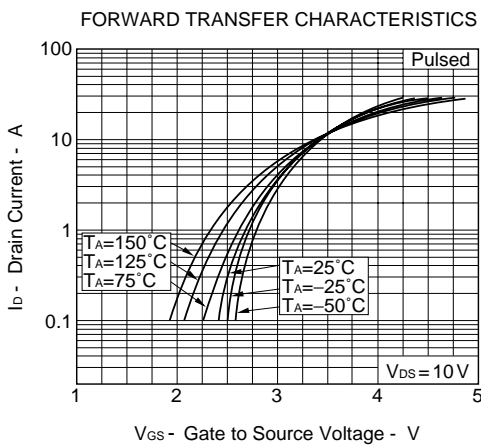
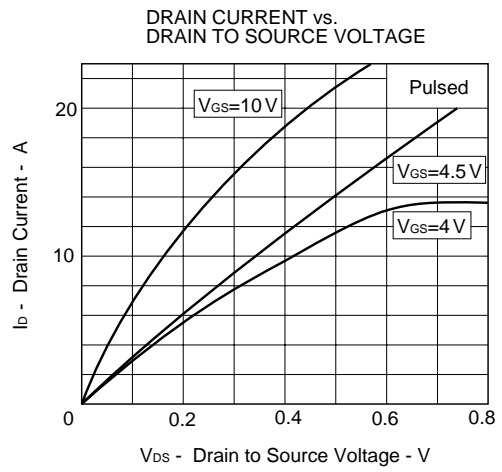
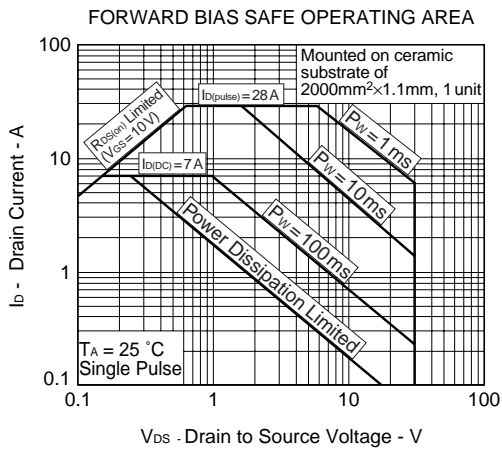
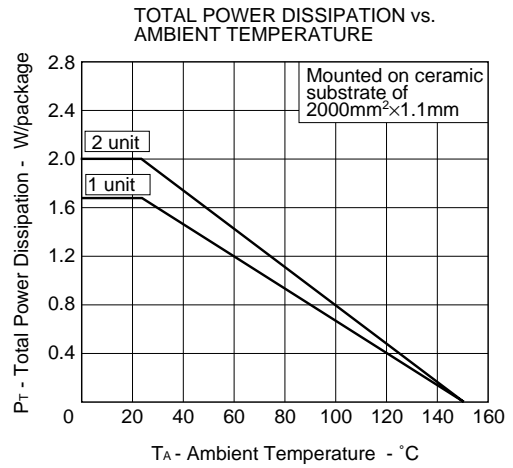
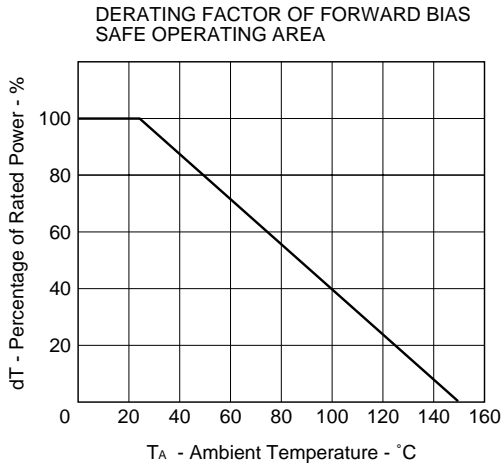


TYPICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$)

TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH







[MEMO]

[MEMO]

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