

4,194,304 WORD × 1 BIT DYNAMIC RAM

\* This is advanced information and specifications are subject to change without notice.

**DESCRIPTION**

The TC514102AP/AJ/ASJ/AZ is the new generation dynamic RAM organized 4,194,304 words by 1 bit. The TC514102AP/AJ/ASJ/AZ utilizes TOSHIBA's CMOS Silicon gate process technology as well as advanced circuit techniques to provide wide operating margins, both internally and to the system user. Multiplexed address inputs permit the TC514102AP/AJ/ASJ/AZ to be packaged in a standard 18 pin plastic DIP, 26/20 pin plastic SOJ (300/350mil) and 20 pin plastic ZIP. The package size provides high system bit densities and is compatible with widely available automated testing and insertion equipment. System oriented features include single power supply of 5V±10% tolerance, direct interfacing capability with high performance logic families such as Schottky TTL.

**FEATURES**

- 4,194,304 word by 1bit organization
- Fast access time and cycle time

		TC514102AP/AJ/ASJ/AZ - 60
t <sub>RAC</sub>	RAS Access Time	60ns
t <sub>AA</sub>	Column Address Access Time	30ns
t <sub>CAC</sub>	CS Access Time	20ns
t <sub>RC</sub>	Cycle Time	110ns
t <sub>SC</sub>	Static Column Mode Cycle Time	35ns

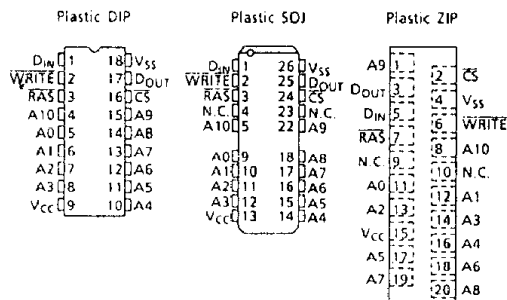
- Single power supply of 5V±10% with a built-in V<sub>BB</sub> generator

- Low Power  
660mW MAX. Operating (TC514102AP/AJ/ASJ/AZ-60)  
5.5mW MAX. Standby
- Output unlatched at cycle end allows two-dimensional chip selection
- Common I/O capability
- Read-Modify-Write, CS before RAS refresh, RAS-only refresh, Hidden refresh, Static Column Mode and Test Mode capability
- All inputs and outputs TTL compatible
- 1,024 refresh cycles/16ms
- Package TC514102AP : DIP18-P-300E  
TC514102AJ : SOJ26-P-350  
TC514102ASJ : SOJ26-P-300A  
TC514102AZ : ZIP20-P-400A

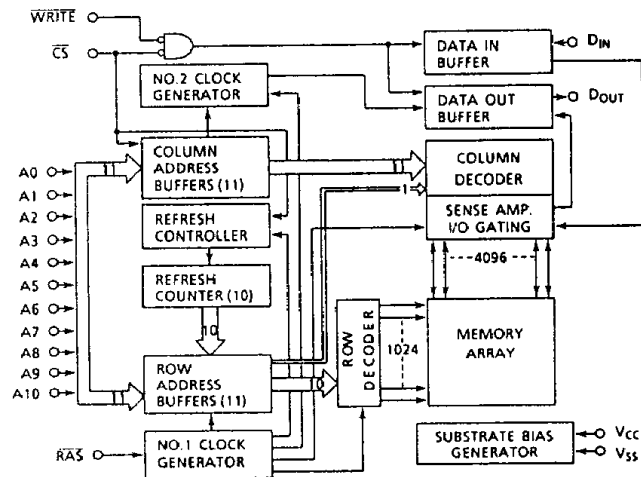
**PIN NAMES**

A0~A10	Address Inputs	WRITE	Read/Write Input
RAS	Row Address Strobe	V <sub>CC</sub>	Power (+ 5V)
D <sub>IN</sub>	Data In	V <sub>SS</sub>	Ground
D <sub>OUT</sub>	Data Out	N.C.	No Connection
CS	Chip Select Input		

**PIN CONNECTION (TOP VIEW)**



**BLOCK DIAGRAM**



# TC514102AP/AJ/ASJ/AZ-60

## ABSOLUTE MAXIMUM RATINGS

ITEM	SYMBOL	RATING	UNITS	NOTES
Input Voltage	$V_{IN}$	-1~7	V	1
Output Voltage	$V_{OUT}$	-1~7	V	1
Power Supply Voltage	$V_{CC}$	-1~7	V	1
Operating Temperature	$T_{OPR}$	0~70	°C	1
Storage Temperature	$T_{STG}$	-55~150	°C	1
Soldering Temperature · Time	$T_{SOLDER}$	260 · 10	°C · sec	1
Power Dissipation	$P_D$	700	mW	1
Short Circuit Output Current	$I_{OUT}$	50	mA	1

## RECOMMENDED DC OPERATING CONDITIONS (Ta = 0~70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	NOTES
$V_{CC}$	Supply Voltage	4.5	5.0	5.5	V	2
$V_{IH}$	Input High Voltage	2.4	-	6.5	V	2
$V_{IL}$	Input Low Voltage	-1.0	-	0.8	V	2

## DC ELECTRICAL CHARACTERISTICS ( $V_{CC} = 5V \pm 10\%$ , $T_a = 0 \sim 70^\circ C$ )

SYMBOL	PARAMETER	MIN.	MAX.	UNITS	NOTES	
$I_{CC1}$	OPERATING CURRENT Average Power Supply Operating Current ( $\overline{RAS}$ , $\overline{CS}$ , Address Cycling: $t_{RC} = t_{RC} \text{ MIN.}$ )	TC514102AP/AJ/ASJ/AZ-60	-	120	mA	3, 4 5
$I_{CC2}$	STANDBY CURRENT Power Supply Standby Current ( $\overline{RAS} = \overline{CS} = V_{IH}$ )		-	2	mA	
$I_{CC3}$	$\overline{RAS}$ ONLY REFRESH CURRENT Average Power Supply Current, $\overline{RAS}$ Only Mode ( $\overline{RAS}$ Cycling, $\overline{CS} = V_{IH}$ : $t_{RC} = t_{RC} \text{ MIN.}$ )	TC514102AP/AJ/ASJ/AZ-60	-	120	mA	3, 5
$I_{CC4}$	STATIC COLUMN MODE CURRENT Average Power Supply Current, Static Column Mode ( $\overline{RAS} = \overline{CS} = V_{IL}$ , Address Cycling: $t_{SC} = t_{SC} \text{ MIN.}$ )	TC514102AP/AJ/ASJ/AZ-60	-	85	mA	3, 4 5
$I_{CC5}$	STANDBY CURRENT Power Supply Standby Current ( $\overline{RAS} = \overline{CS} = V_{CC} - 0.2V$ )		-	1	mA	
$I_{CC6}$	$\overline{CS}$ BEFORE $\overline{RAS}$ REFRESH CURRENT Average Power Supply Current, $\overline{CS}$ Before $\overline{RAS}$ Mode ( $\overline{RAS}$ , $\overline{CS}$ Cycling: $t_{RC} = t_{RC} \text{ MIN.}$ )	TC514102AP/AJ/ASJ/AZ-60	-	120	mA	3, 5
$I_{I(L)}$	INPUT LEAKAGE CURRENT Input Leakage Current, any input ( $0V \leq V_{IH} \leq 6.5V$ , All Other Pins Not Under Test = $0V$ )		- 10	10	$\mu A$	
$I_{O(L)}$	OUTPUT LEAKAGE CURRENT ( $D_{OUT}$ is disabled, $0V \leq V_{OUT} \leq +5.5V$ )		- 10	10	$\mu A$	
$V_{OH}$	OUTPUT LEVEL Output "H" Level Voltage ( $I_{OUT} = -5mA$ )		2.4	-	V	
$V_{OL}$	OUTPUT LEVEL Output "L" Level Voltage ( $I_{OUT} = 4.2mA$ )		-	0.4	V	

# TC514102AP/AJ/ASJ/AZ-60

## ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

( $V_{CC} = 5V \pm 10\%$ ,  $T_a = 0 \sim 70^\circ\text{C}$ )(Notes 6, 7, 8)

SYMBOL	PARAMETER	TC514102AP/AJ/ASJ/AZ-60		UNIT	NOTES
		MIN.	MAX.		
$t_{RC}$	Random Read or Write Cycle Time	110	-	ns	
$t_{RMW}$	Read-Modify-Write Cycle Time	135	-	ns	
$t_{SC}$	Static Column Mode Cycle Time	35	-	ns	
$t_{SRMW}$	Static Column Mode Read-Modify-Write Cycle Time	60	-	ns	
$t_{RAC}$	Access Time from $\overline{RAS}$	-	60	ns	9, 14 15
$t_{CAC}$	Access Time from $\overline{CS}$	-	20	ns	9, 14
$t_{AA}$	Access Time from Column Address	-	30	ns	9, 15
$t_{ALW}$	Access Time from Last Write	-	55	ns	9, 16
$t_{CLZ}$	$\overline{CS}$ to Output in Low-Z	0	-	ns	9
$t_{OFF}$	Output Buffer Turn-Off Delay	0	20	ns	10
$t_{AOH}$	Output Data Hold Time from Column Address	5	-	ns	
$t_{OW}$	Output Data Enable Time from $\overline{WRITE}$	-	20	ns	
$t_{WOH}$	Output Data Hold Time from $\overline{WRITE}$	0	-	ns	
$t_T$	Transition Time (Rise and Fall)	3	50	ns	8
$t_{RP}$	$\overline{RAS}$ Precharge Time	40	-	ns	
$t_{RAS}$	$\overline{RAS}$ Pulse Width	60	10,000	ns	
$t_{RASC}$	$\overline{RAS}$ Pulse Width (Static Column Mode)	60	200,000	ns	
$t_{RSH}$	$\overline{CS}$ to $\overline{RAS}$ Hold Time	20	-	ns	
$t_{CSH}$	$\overline{RAS}$ to $\overline{CS}$ Hold Time	60	-	ns	
$t_{CS}$	$\overline{CS}$ Pulse Width	20	10,000	ns	
$t_{CSC}$	$\overline{CS}$ Pulse Width (Static Column Mode)	20	200,000	ns	
$t_{RCD}$	$\overline{RAS}$ to $\overline{CS}$ Delay Time	20	40	ns	14
$t_{RAD}$	$\overline{RAS}$ to Column Address Delay Time	15	30	ns	15
$t_{CRP}$	$\overline{CS}$ to $\overline{RAS}$ Precharge Time	5	-	ns	
$t_{CP}$	$\overline{CS}$ Precharge Time (Static Column Mode)	10	-	ns	
$t_{ASR}$	Row Address Set-Up Time	0	-	ns	
$t_{RAH}$	Row Address Hold Time	10	-	ns	
$t_{ASC}$	Column Address Set-Up Time	0	-	ns	
$t_{CAH}$	Column Address Hold Time	15	-	ns	

## ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS (Continued)

SYMBOL	PARAMETER	TC514102AP/AJ/ASJ/AZ-60		UNITS	NOTES
		MIN.	MAX.		
$t_{AR}$	Column Address Hold Time referenced to $\overline{RAS}$ (READ CYCLE)	70	-	ns	
$t_{RAL}$	Column Address to $\overline{RAS}$ Lead Time	30	-	ns	
$t_{AH}$	Column Address Hold Time referenced to $\overline{RAS}$ Rise	5	-	ns	17
$t_{CWL}$	Write Command to $\overline{CS}$ Lead Time	20	-	ns	
$t_{LWAD}$	Last Write to Column Address Delay Time	20	25	ns	16
$t_{AHLW}$	Last Write to Column Address Hold Time	55	-	ns	
$t_{RCS}$	Read Command Set-up Time referenced to $\overline{CS}$	0	-	ns	
$t_{RCH}$	Read Command Hold Time referenced to $\overline{CS}$	0	-	ns	11
$t_{RRH}$	Read Command Hold Time referenced to $\overline{RAS}$	0	-	ns	11
$t_{WCH}$	Write Command Hold Time	10	-	ns	13
$t_{WCP}$	Write Command Pulse Width	10	-	ns	
$t_{WCI}$	Write Command Inactive Time	10	-	ns	
$t_{RWL}$	Write Command to $\overline{RAS}$ Lead Time	20	-	ns	
$t_{DS}$	Data-In Set-Up Time	0	-	ns	12
$t_{DH}$	Data-In Hold Time	15	-	ns	12
$t_{REF}$	Refresh Period	-	16	ms	
$t_{WCS}$	Write Command Set-UP Time	0	-	ns	13
$t_{CWD}$	$\overline{CS}$ to $\overline{WRITE}$ Delay Time (READ-MODIFY-WRITE CYCLE)	20	-	ns	13
$t_{RWD}$	$\overline{RAS}$ to $\overline{WRITE}$ Delay Time (READ-MODIFY-WRITE CYCLE)	60	-	ns	13
$t_{AWD}$	Column Address to $\overline{WRITE}$ Delay Time	30	-	ns	13
$t_{CSR}$	$\overline{CS}$ Set-Up Time ( $\overline{CS}$ before $\overline{RAS}$ )	5	-	ns	
$t_{CHR}$	$\overline{CS}$ Hold Time ( $\overline{CS}$ before $\overline{RAS}$ )	15	-	ns	
$t_{RPC}$	$\overline{RAS}$ Precharge to $\overline{CS}$ Active Time	0	-	ns	
$t_{CPT}$	$\overline{CS}$ Precharge Time ( $\overline{CS}$ before $\overline{RAS}$ Counter Test)	30	-	ns	

# TC514102AP/AJ/ASJ/AZ-60

## ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS (Continued)

SYMBOL	PARAMETER	TC514102AP/AJ/ASJ/AZ-60		UNIT	NOTES
		MIN.	MAX.		
t <sub>WTS</sub>	Write Command Set-Up Time	10	–	ns	
t <sub>WTH</sub>	Write Command Hold Time	10	–	ns	
t <sub>WRP</sub>	WRITE to RAS Precharge Time	10	–	ns	
t <sub>WRH</sub>	WRITE to RAS Hold Time	10	–	ns	

# TC514102AP/AJ/ASJ/AZ-60

## ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATION CONDITIONS IN THE TEST MODE ( $V_{CC} = 5V \pm 10\%$ , $T_a = 0 \sim 70^\circ\text{C}$ ) (Note6, 7, 8)

SYMBOL	PARAMETER	TC514102AP/AJ/ASJ/AZ-60		UNIT	NOTES
		MIN.	MAX.		
$t_{RC}$	Random Read or Write Cycle Time	115	-	ns	
$t_{SC}$	Static Column Mode Cycle Time	40	-	ns	
$t_{RAC}$	Access Time from $\overline{RAS}$	-	65	ns	9,14 15
$t_{CAC}$	Access Time from $\overline{CS}$	-	25	ns	9,14
$t_{AA}$	Access Time from Column Address	-	35	ns	9,15
$t_{RAS}$	$\overline{RAS}$ Pulse Width	65	10,000	ns	
$t_{RASC}$	$\overline{RAS}$ Pulse Width (Static Column Mode)	75	20,000	ns	
$t_{RSH}$	$\overline{RAS}$ Hold Time	25	-	ns	
$t_{CSH}$	$\overline{CS}$ Hold Time	65	-	ns	
$t_{CS}$	$\overline{CS}$ Pulse Width	25	10,000	ns	
$t_{CSC}$	$\overline{CS}$ Pulse Width (Static Column Mode)	25	20,000	ns	
$t_{RAL}$	Column Address to $\overline{RAS}$ Lead Time	35	-	ns	

## CAPACITANCE ( $V_{CC} = 5V \pm 10\%$ , $f = 1\text{MHz}$ , $T_a = 0 \sim 70^\circ\text{C}$ )

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
$C_{I1}$	Input Capacitance (A0~A10, D <sub>IN</sub> )	-	5	pF
$C_{I2}$	Input Capacitance ( $\overline{RAS}$ , $\overline{CS}$ , $\overline{WRITE}$ )	-	7	pF
$C_O$	Output Capacitance (D <sub>OUT</sub> )	-	7	pF

# TC514102AP/AJ/ASJ/AZ-60

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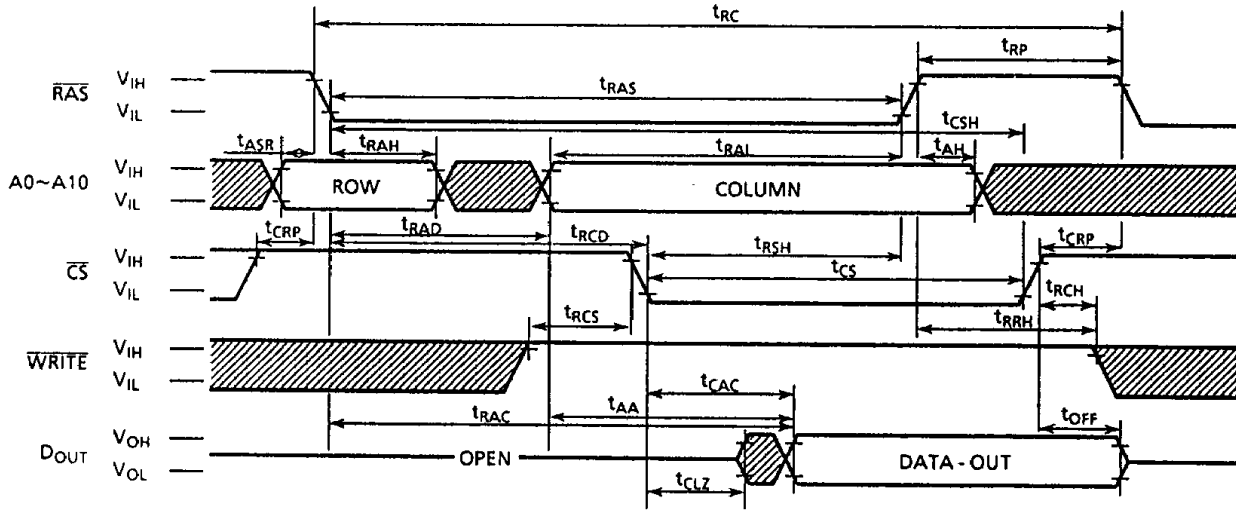
## NOTES:

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.
2. All voltages are referenced to  $V_{SS}$ .
3.  $I_{CC1}$ ,  $I_{CC3}$ ,  $I_{CC4}$ ,  $I_{CC6}$  depend on cycle rate.
4.  $I_{CC1}$ ,  $I_{CC4}$  depend on output loading. Specified values are obtained with the output open.
5. Column address can be changed once or less While  $\overline{RAS}=V_{IL}$ .
6. An initial pause of 200 $\mu$ s is required after power-up followed by any 8  $\overline{RAS}$  only refresh cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8  $\overline{CS}$  Before  $\overline{RAS}$  refresh cycles instead of 8  $\overline{RAS}$  only refresh cycles are required.
7. AC measurements assume  $t_T=5$ ns.
8.  $V_{IH}$  (min.) and  $V_{IL}$  (max.) are reference levels for measuring timing of input signals. Also, transition times are measured between  $V_{IH}$  and  $V_{IL}$ .
9. Measured with a load equivalent to 2 TTL loads and 100pF.
10.  $t_{OFF}$  (max.) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
11. Either  $t_{RCH}$  or  $t_{RRH}$  must be satisfied for a read cycle.
12. These parameters are referenced to  $\overline{CS}$  leading edge in early write cycles and to  $\overline{WRITE}$  leading edge in read-write cycles.
13.  $t_{WCS}$ ,  $t_{RWD}$ ,  $t_{CWD}$ , and  $t_{AWD}$  are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If  $t_{WCS} \geq t_{WCS}(\text{min.})$ , the cycle is an early write cycle and data out pin will remain open circuit (high impedance) throughout the entire cycle; If  $t_{RWD} \geq t_{RWD}(\text{min.})$ ,  $t_{CWD} \geq t_{CWD}(\text{min.})$ , and  $t_{AWD} \geq t_{AWD}(\text{min.})$ , the cycle is a read-write cycle and the data out will contain data read from the selected cell: If neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
14. Operation within the  $t_{RCD}(\text{min.})$  limit insures that  $t_{RAC}(\text{max.})$  can be met.  $t_{RCD}(\text{max.})$  is specified as a reference point only: If  $t_{RCD}$  is greater than the specified  $t_{RCD}(\text{max.})$  limit, then access time is controlled by  $t_{CAC}$ .
15. Operation within the  $t_{RAD}(\text{max.})$  limit insures that  $t_{RAC}(\text{max.})$  can be met.  $t_{RAD}(\text{max.})$  is specified as a reference point only: If  $t_{RAD}$  is greater than the specified  $t_{RAD}(\text{max.})$  limit, then access time is controlled exclusively by  $t_{AA}$ .
16. Operation within the  $t_{LWAD}(\text{max.})$  limit insures that  $t_{ALW}(\text{max.})$  can be met.  $t_{LWAD}(\text{max.})$  is specified as a reference point only: If  $t_{LWAD}$  is greater than the specified  $t_{LWAD}(\text{max.})$  limit, then access time is controlled exclusively by  $t_{AA}$ .
17.  $t_{AH}$  is the condition to latch column address when  $\overline{RAS}$  has risen up.

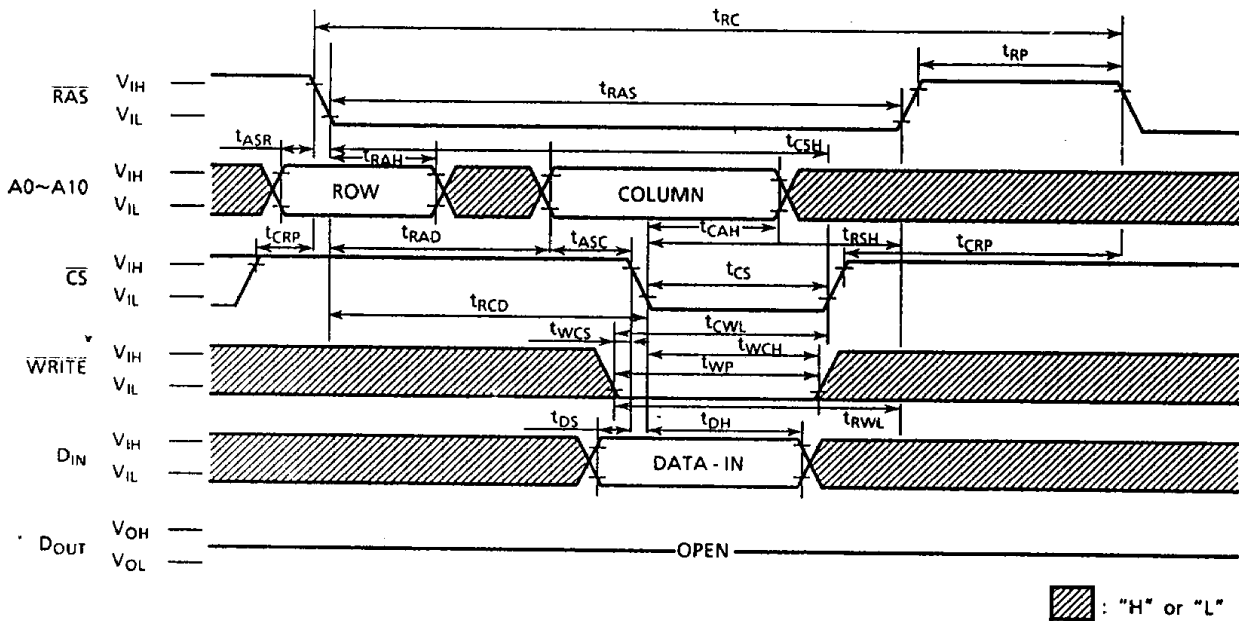


TIMING WAVEFORMS

READ CYCLE



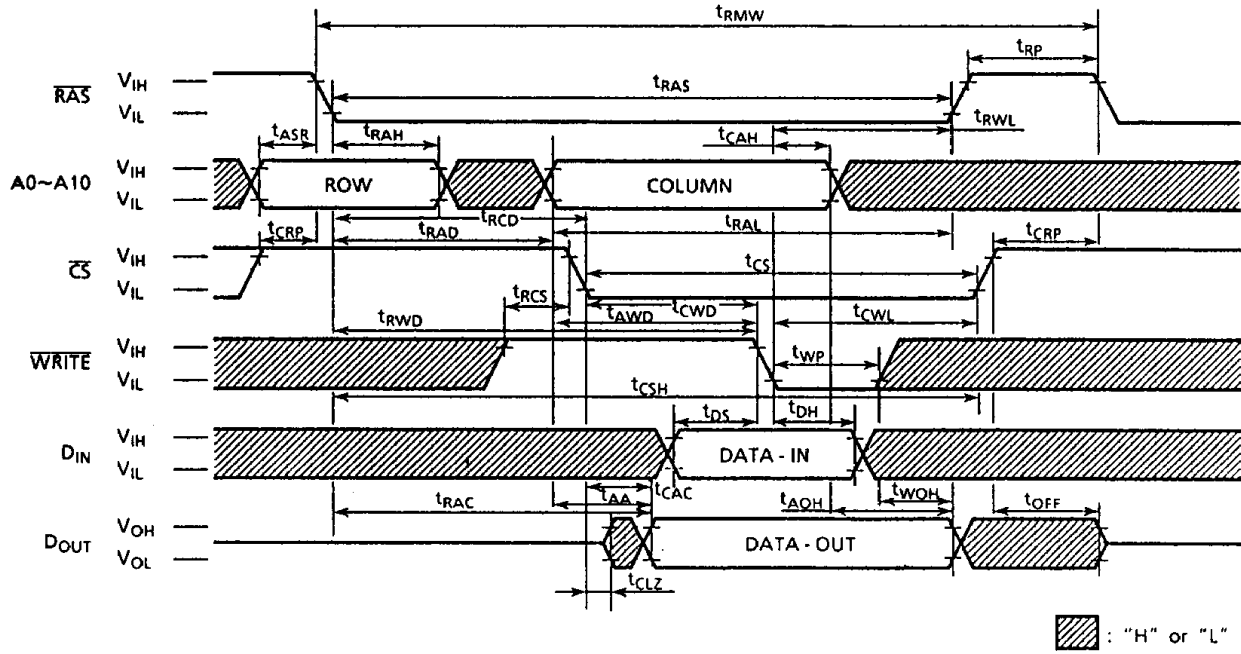
WRITE CYCLE (EARLY WRITE)



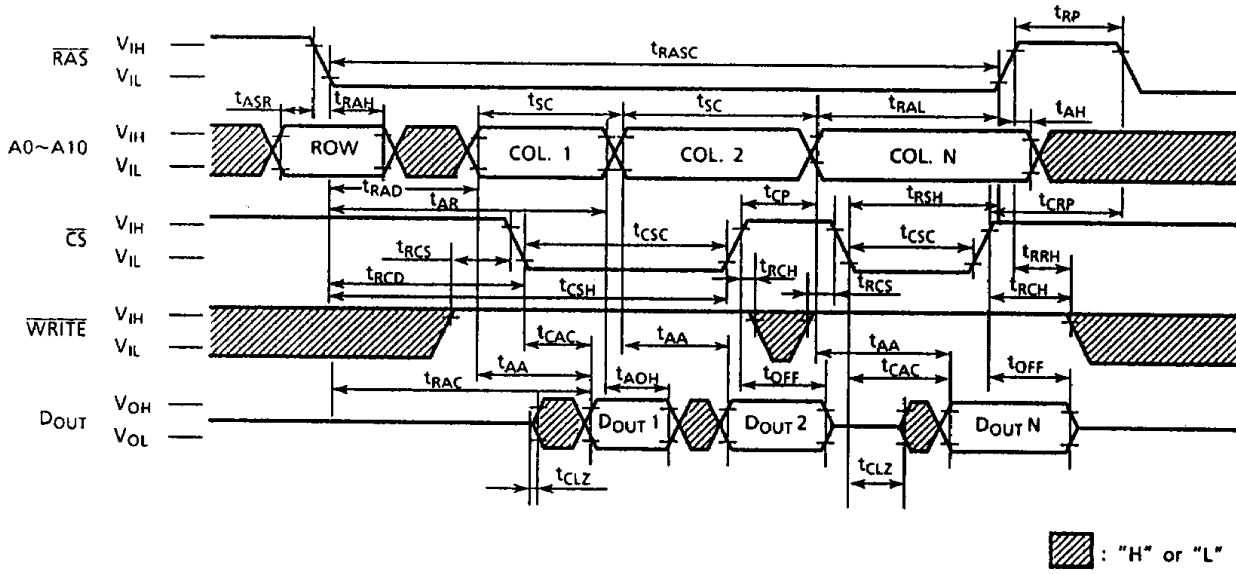
▨ : "H" or "L"

# TC514102AP/AJ/ASJ/AZ-60

## READ - MODIFY - WRITE CYCLE



STATIC COLUMN MODE READ CYCLE

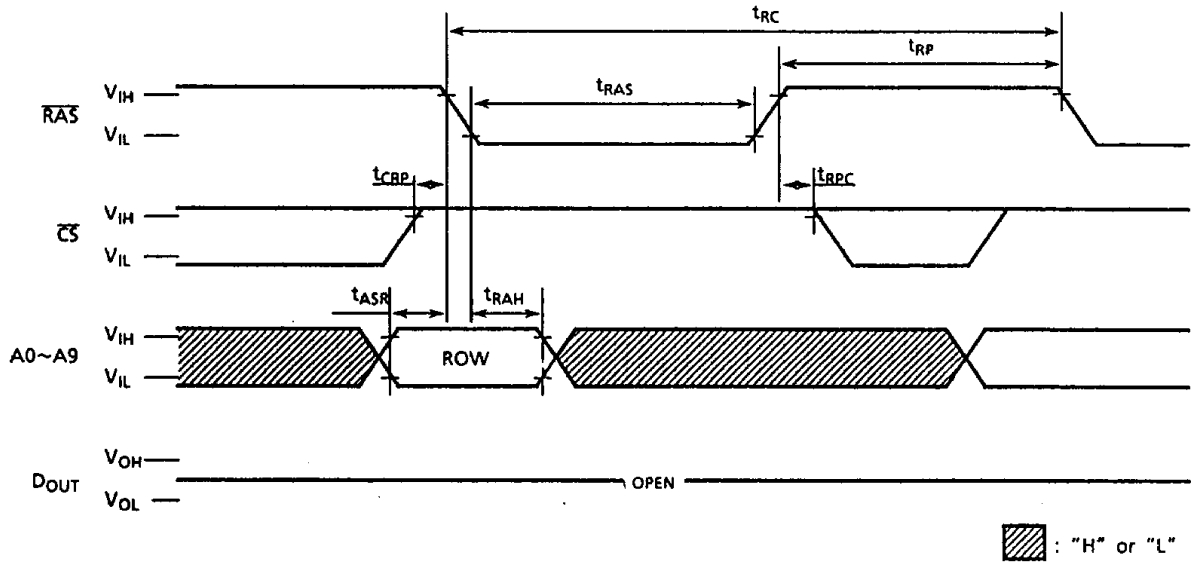






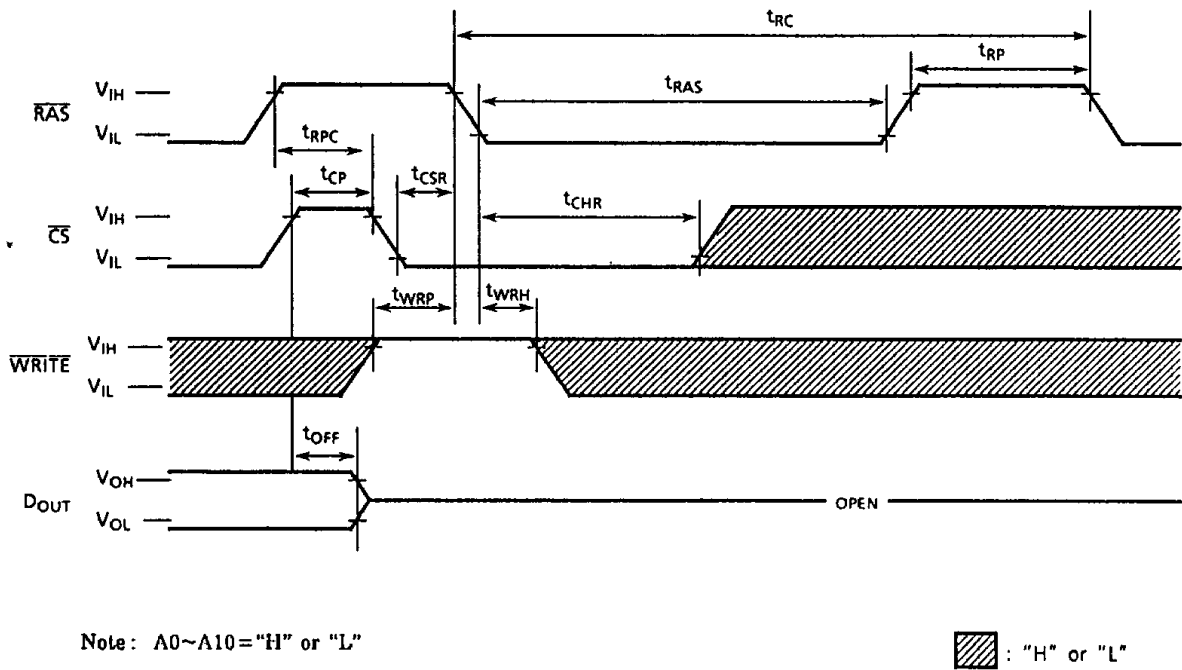
# TC514102AP/AJ/ASJ/AZ-60

## RAS ONLY REFRESH CYCLE



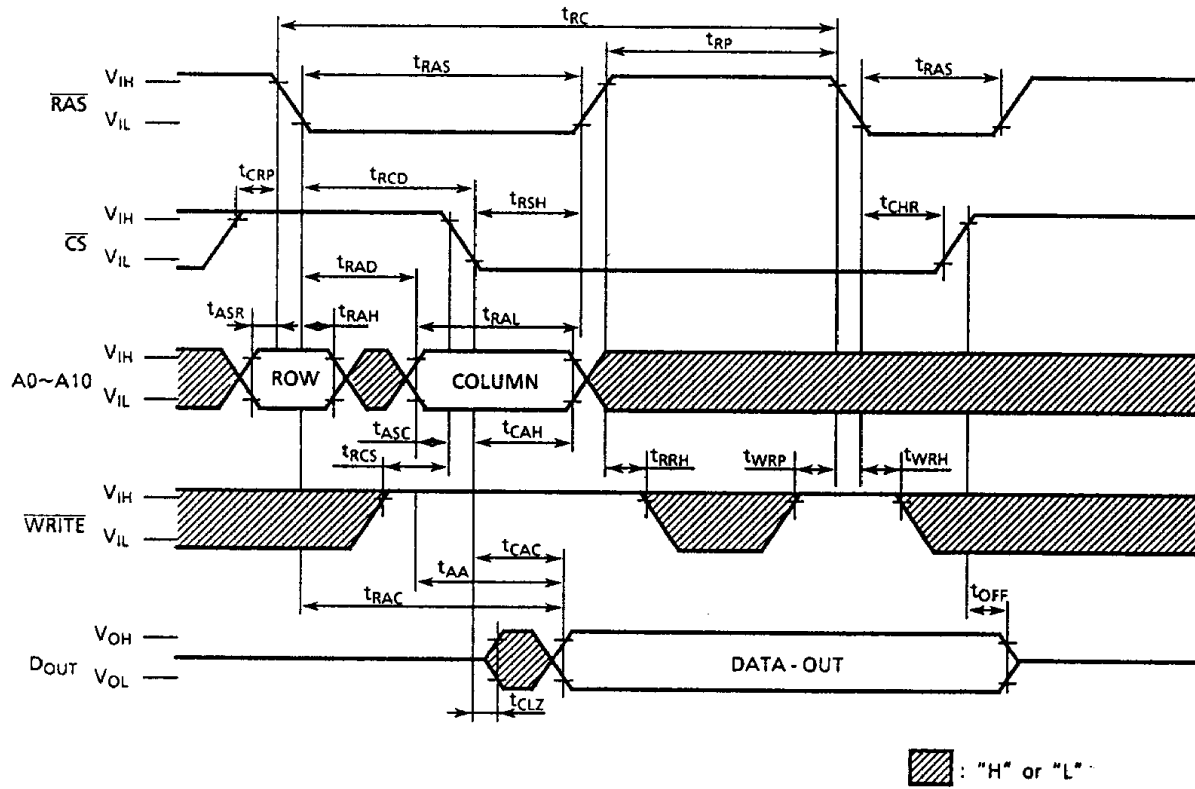
Note: WRITE, A10 = "H" or "L"

## CS BEFORE RAS REFRESH CYCLE



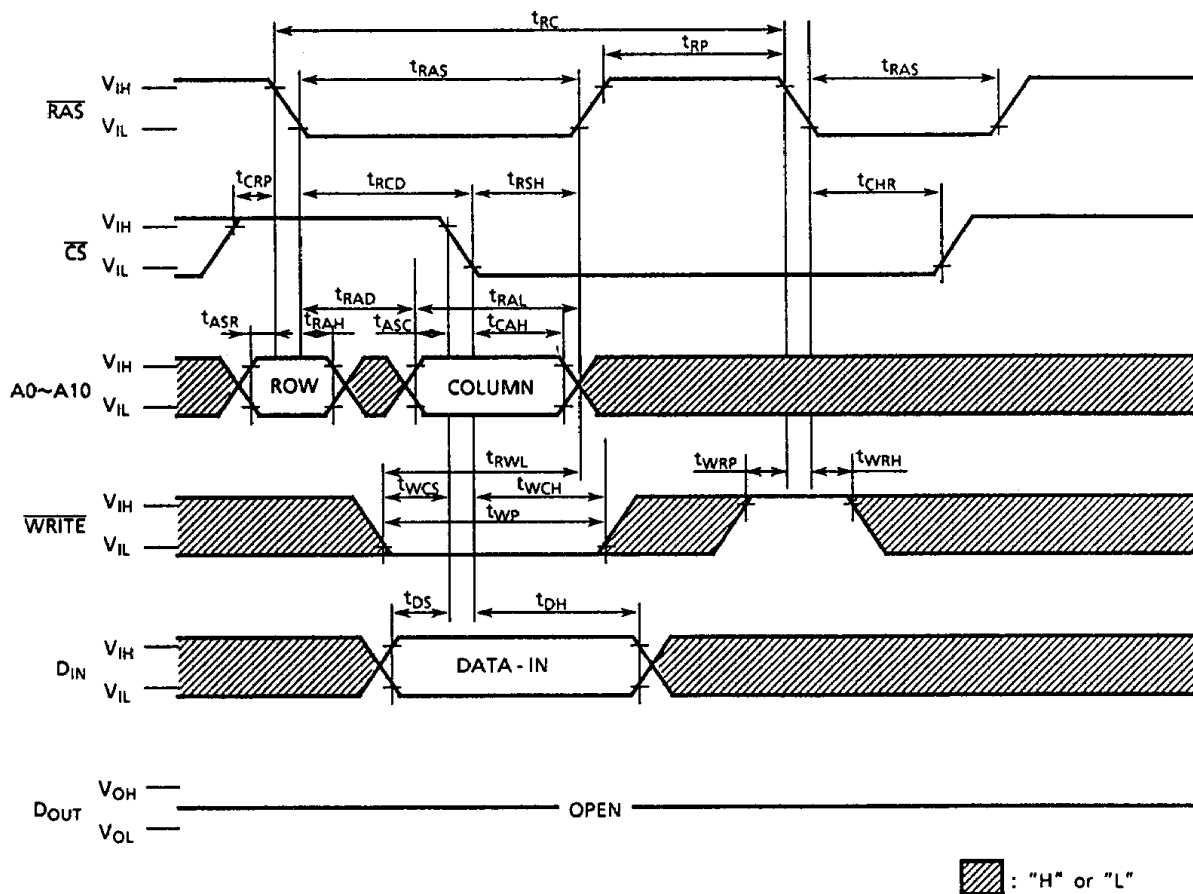
Note: A0~A10 = "H" or "L"

HIDDEN REFRESH CYCLE (READ)



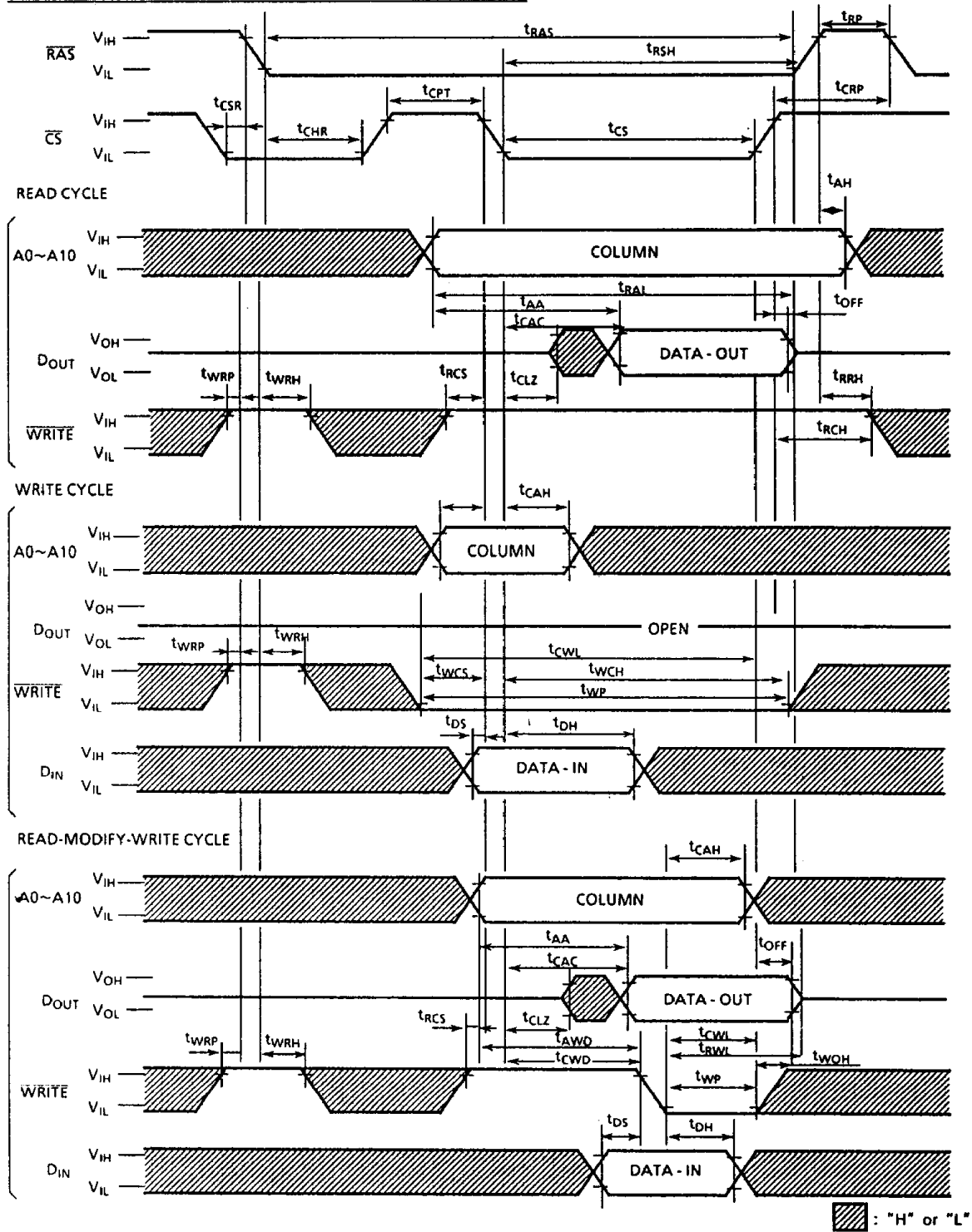
# TC514102AP/AJ/ASJ/AZ-60

## HIDDEN REFRESH CYCLE (WRITE)



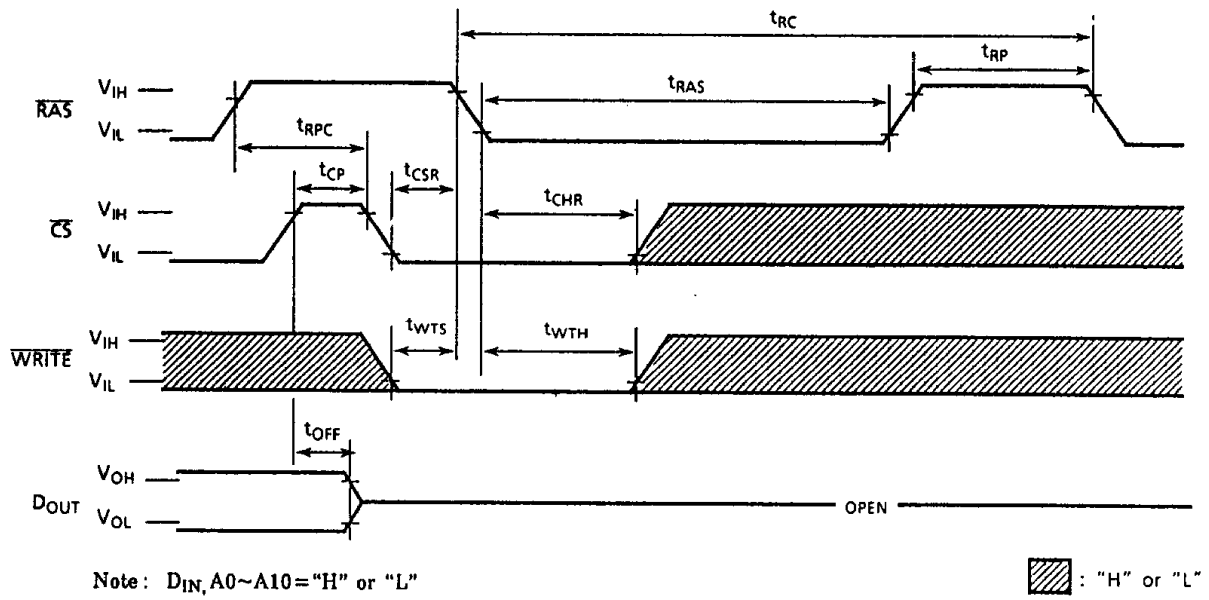


CS BEFORE RAS REFRESH COUNTER TEST CYCLE



# TC514102AP/AJ/ASJ/AZ-60

## WRITE, CS BEFORE RAS REFRESH CYCLE



## TEST MODE

The TC514102AP/AJ/ASJ/AZ is The RAM organized 4,194,304 words by 1 bit, it is internally organized 524,288 words by 8 bits. In "Test Mode", data are written into 8 sectors in parallel and retrieved the same way. A10R, A10C and A0C are not used. If, upon reading, all bits are equal (all "1"s or "0"s), the data output pin indicates a "1" shows the block diagram of TC514102AP/AJ/ASJ/AZ. In "Test Mode", the 4M DRAM can be tested as if it were a 512K DRAM.

" $\overline{\text{WRITE}}$ ,  $\overline{\text{CS}}$  Before  $\overline{\text{RAS}}$  Refresh Cycle" puts the device "Test Mode". And " $\overline{\text{CS}}$  Before  $\overline{\text{RAS}}$  Refresh Cycle" or " $\overline{\text{RAS}}$  Only Refresh Cycle" puts it back into "Normal Mode". In the Test Mode, " $\overline{\text{WRITE}}$ ,  $\overline{\text{CS}}$  Before  $\overline{\text{RAS}}$  Refresh Cycle" performs the refresh operation with the internal refresh address counter. The "Test Mode" function reduces test times (1/8 in case of N test pattern).

# TC514102AP/AJ/ASJ/AZ-60

## BLOCK DIAGRAM IN THE TEST MODE

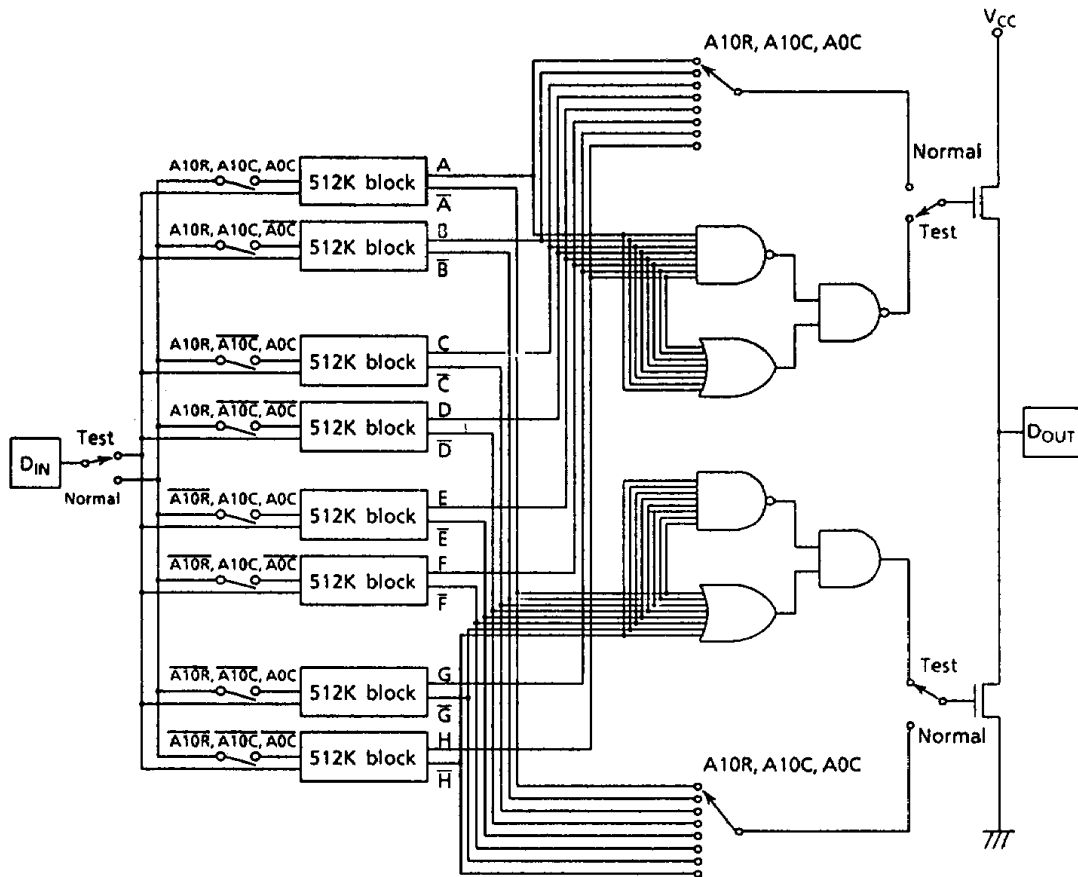


Fig. 1