MN6474A

D/A Converter for Digital Audio Equipment

■ Overview

The MN6474A is a CMOS digital-to-analog converter with a built-in 16-bit digital filter for pulse code modulation (PCM) digital audio equipment.

It uses noise shaping technology to convert a digital signal into a PWM signal.

It contains a 4-fold oversampling digital filter that permits simplification of the low pass filter after the D/A converter, thus greatly reducing the power consumption of the entire D/A conversion system.

The chip provides both regular and inverted phase outputs for both channels.

The chip contributes to cost and size reductions for CD players and other digital audio equipment.

■ Features

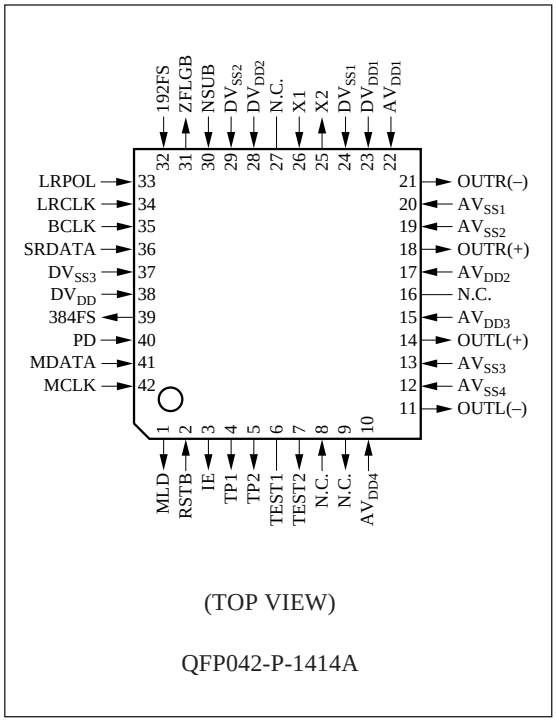
- Built-in 4-fold oversampling digital filter

  (ripple of only ±0.0072 dB within the supported band and attenuation of 62.7 dB within the cutoff band)
- Internal resolution of 18 bits
- Two's complement input (I^2S input code also supported)
- Built-in overflow limiter
- No zero cross distortion
- Sample-and-hold circuit is unnecessary
- Output pin for detecting zero input
- Single 5V power supply

■ Applications

- CD players and other digital audio equipment

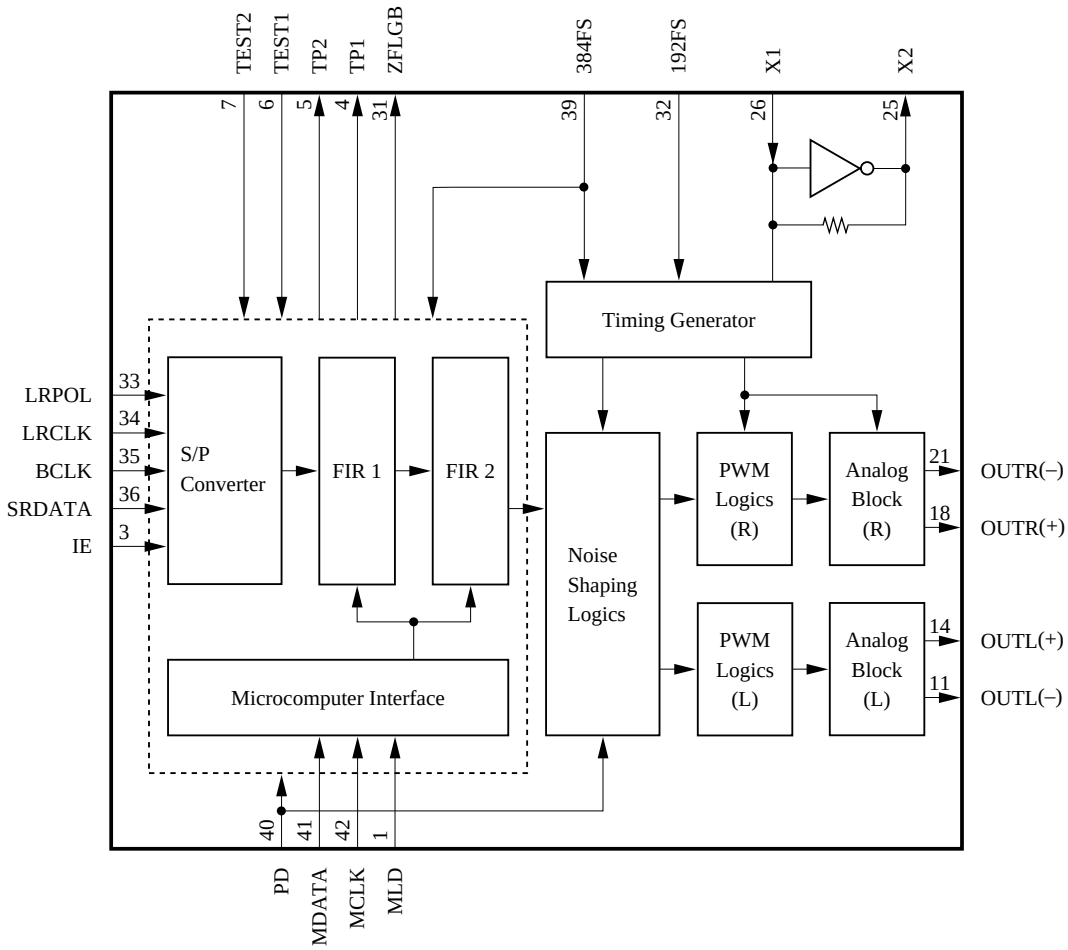
■ Pin Assignment



(TOP VIEW)

QFP042-P-1414A

■ Block Diagram



■ Pin Descriptions

Pin No.	Symbol	Function Description
1	MLD	Microcomputer command load input ("L" level to load)
2	RSTB	Reset pin (active "L"). Always pull this pin low after applying the power.
3	IE	Input format selection pin. "H" level; I^2S format "L" level; signal processing LSI format.
4	TP1	Digital filter test output pin 1. Leave this pin open.
5	TP2	Digital filter test output pin 2. Leave this pin open.
6	TEST1	Digital filter test input pin 1. Keep this pin at "L" level.
7	TEST2	Digital filter test input pin 2. Keep this pin at "L" level.
8	N.C.	No connection Leave these pins open.
9	N.C.	No connection Leave these pins open.
10	AV_{DD4}	Power supply pin 4 for analog circuits. (+5V)
11	OUTL(–)	Left channel inverted phase PWM output pin.
12	AV_{SS4}	Ground pin 4 for analog circuits.
13	AV_{SS3}	Ground pin 3 for analog circuits.
14	OUTL(+)	Left channel normal phase PWM output pin.
15	AV_{DD3}	Power supply pin 3 for analog circuits. (+5V)
16	N.C.	No connection Leave this pin open.
17	AV_{DD2}	Power supply pin 2 for analog circuits. (+5V)
18	OUTR(+)	Right channel through phase PWM output pin.
19	AV_{SS2}	Ground pin 2 for analog circuits.
20	AV_{SS1}	Ground pin 1 for analog circuits.
21	OUTR(–)	Right channel inverted phase PWM output pin.
22	AV_{DD1}	Power supply pin 1 for analog circuits. (+5V)
23	DV_{DD1}	Power supply pin 1 for digital circuits. (+5V) (Power supply for oscillator circuit)
24	DV_{SS1}	Ground pin 1 for digital circuits. (Ground for oscillator circuit)
25	X2	Crystal oscillator pin.
26	X1	Crystal oscillator pin. (External clock input pin)
27	N.C.	No connection Leave this pin open.
28	DV_{DD2}	Power supply pin 2 for analog circuits. (+5V)
29	DV_{SS2}	Ground pin 2 for digital circuits.
30	NSUB	Connect to $D\text{-}V_{DD}$. (Silicon substrate potential fixing pin)
31	ZFLGB	Output pin for detecting zero input.
32	192FS	$192f_s$(=9.216 MHz)output pin. Max. load capacity: 30 pF.
33	LRPOL	LRCLK polarity selection pin. "H" level; selects the left channel "L" level; the right channel.
34	LRCLK	LRCLK pin. When the LRPOL pin is at "H" level, "H" level in this pin indicates left channel data input; "L" level indicates right channel data input. When the LRPOL pin is at "L" level, "L" level in this pin indicates left channel data input; "H" level input indicates right channel data input.
35	BCLK	Serial input bit clock
36	SRDATA	Serial input data (digital) input pin.
37	DV_{SS3}	Ground pin 3 for digital circuits.

■ Pin Descriptions (continued)

Pin No.	Symbol	Function Description
38	DV_{DD}	Power supply pin for digital circuits. (Silicon substrate potential fixing pin.) (+5V)
39	384FS	$384f_s$ (=18.432 MHz) output pin. Max. load capacitance: 30 pF.
40	PD	Power down pin. (active "H")
41	MDATA	Microcomputer command data input pin.
42	MCLK	Clock input pin for microcomputer command.

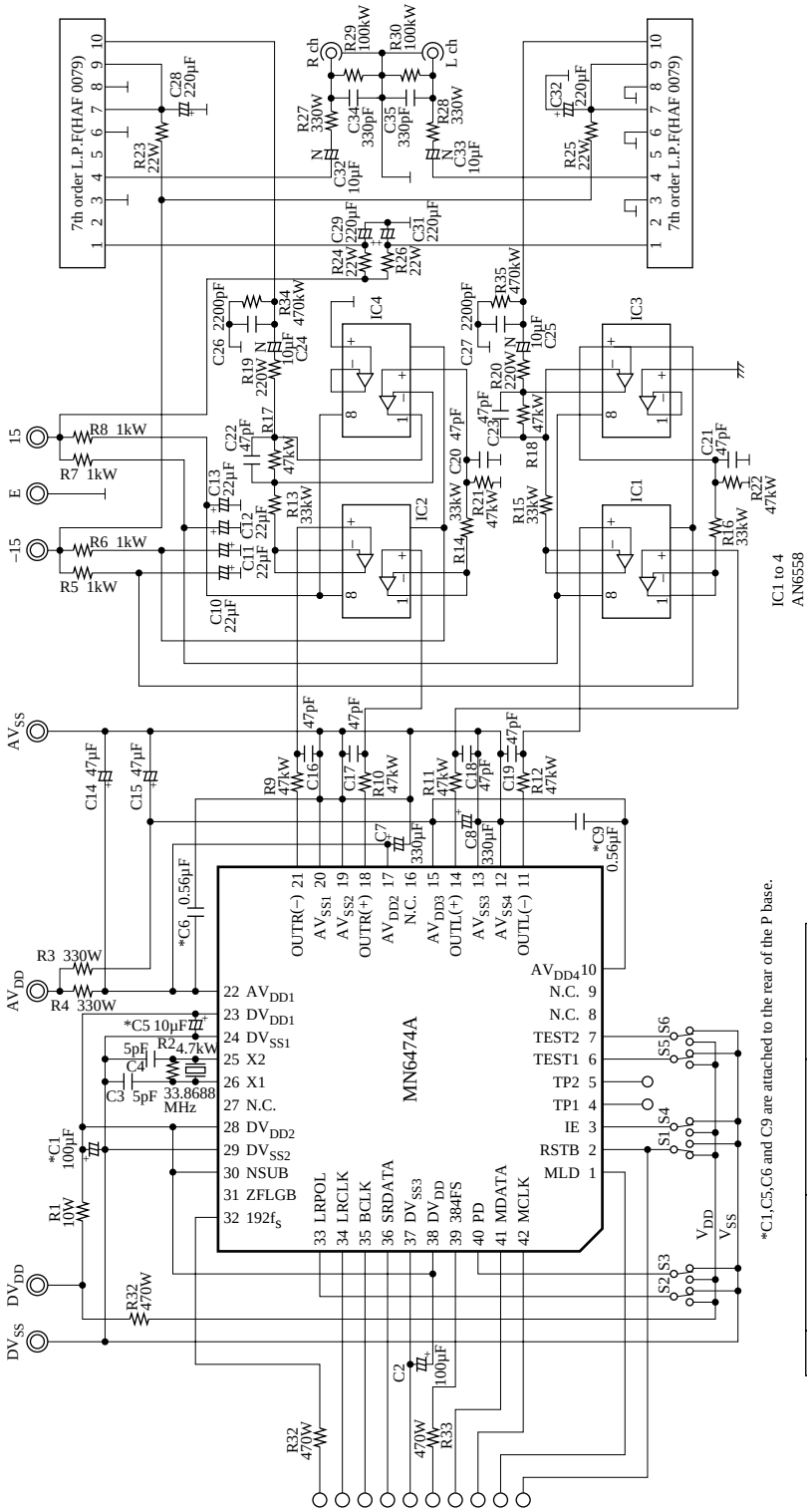
■ Conversion Characteristics

DV_{DD}=5.0V, DV_{SS}=0V, AV_{DD}=5.0V, AV_{SS}=0V, f=33.8688MHz, Ta=25˚C

Parameter	Symbol	Test Conditions	min	typ	max	Unit
Analog characteristics						
Signal-to-noise ratio	S/N	EIAJ (1kHz)	95	106		dB
Dynamic range	D.R.	EIAJ (1kHz)	90	98		dB
Total harmonic distortion	THD+N	EIAJ (1kHz)		0.003	0.005	%
Crosstalk		EIAJ (1kHz)	90	98		dB
Output level *1		1kHz F.S.	1.4	1.7		V_{rms}

Note*1: These analog characteristics are for circuits equivalent to the suggested application circuit.

■ Application Circuit Example



	PD(S3)	RSTB(S1)	IE(S4)
"L"	–	Reset	Signal processing LSI format
"H"	Power down mode	–	I^2S format

■ Package Dmensions (Unit: mm)

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