HA13614FH

Combo (Spindle & VCM) Driver

HITACHI

ADE-207-246D (Z)
Preliminary
5th Edition
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Description

This COMBO driver for HDD application consists of sensorless spindle driver and BTL type VCM driver.

"PWM soft switching function" for low power dissipation and less commutation acoustic noise at the same time is implemented by using the IPIC* process.

Note: Intelligent Power IC

Features

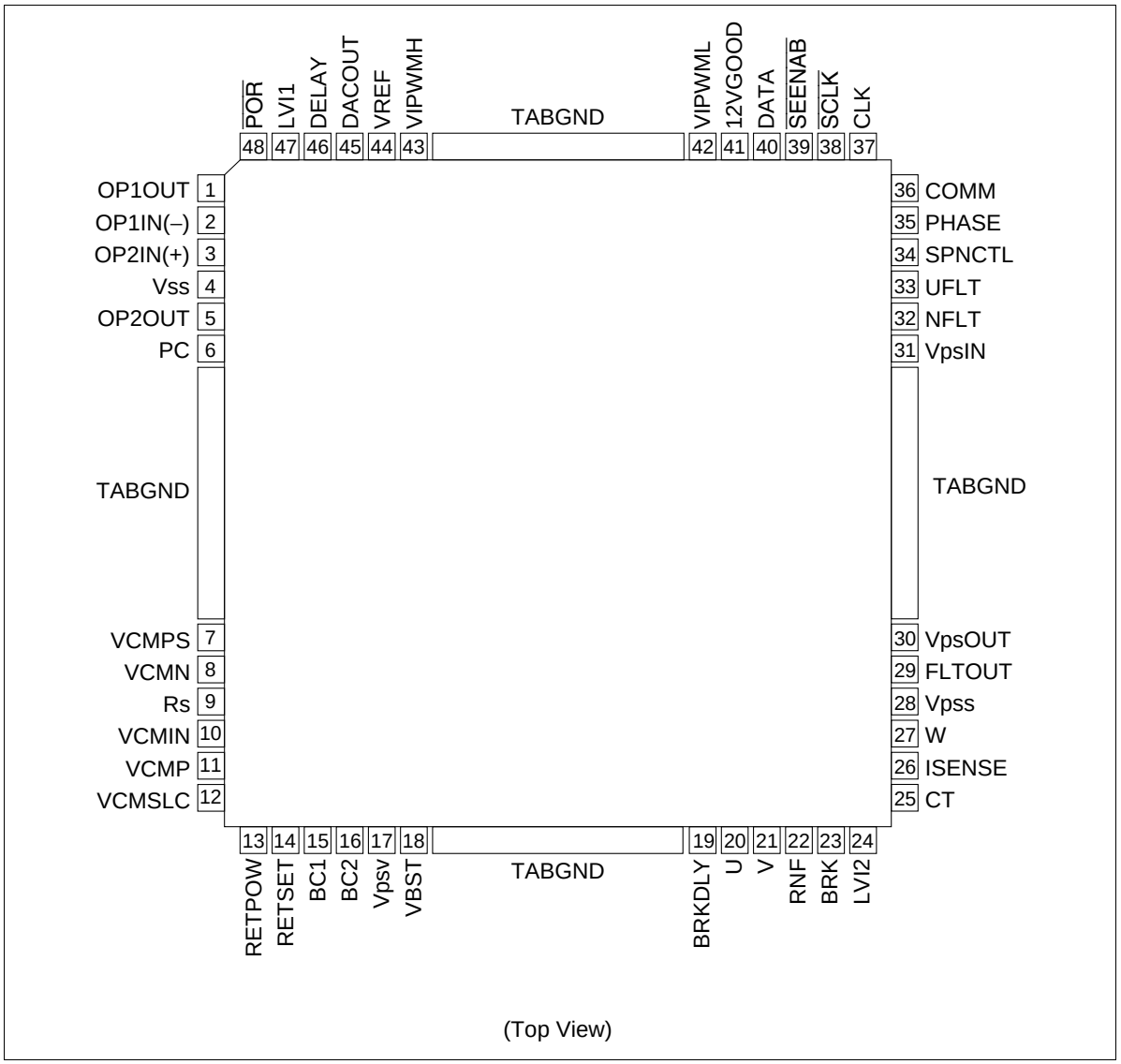
- PWM soft switching drive
- Small surface mount package: FP-48T
- Low thermal resistance: 30°C/W with 4 layer multi glass-epoxy board
- Low output on resistance
  - — Spindle 1.2 Ω Typ
  - — VCM 1.4 Ω Typ
- TTL compatible input level (with 3.3 V logic interface)
- High precision reference voltage output (for 3.3 V power supply)

Functions

- 16 bit serial port
- 2.0 A Max/3-phase spindle motor driver with PWM soft switch function
- 1.5 A Max BTL VCM driver with low crossover distortion
- PWMDAC for VCM drive current control
- Power off brake function for spindle motor
- Auto retract with constant output voltage
- Booster
- Internal Protector (OTSD, LVI)
- Precision power monitor
- OP amplifier

Hitachi semiconductor

Pin Arrangement



(Top View)

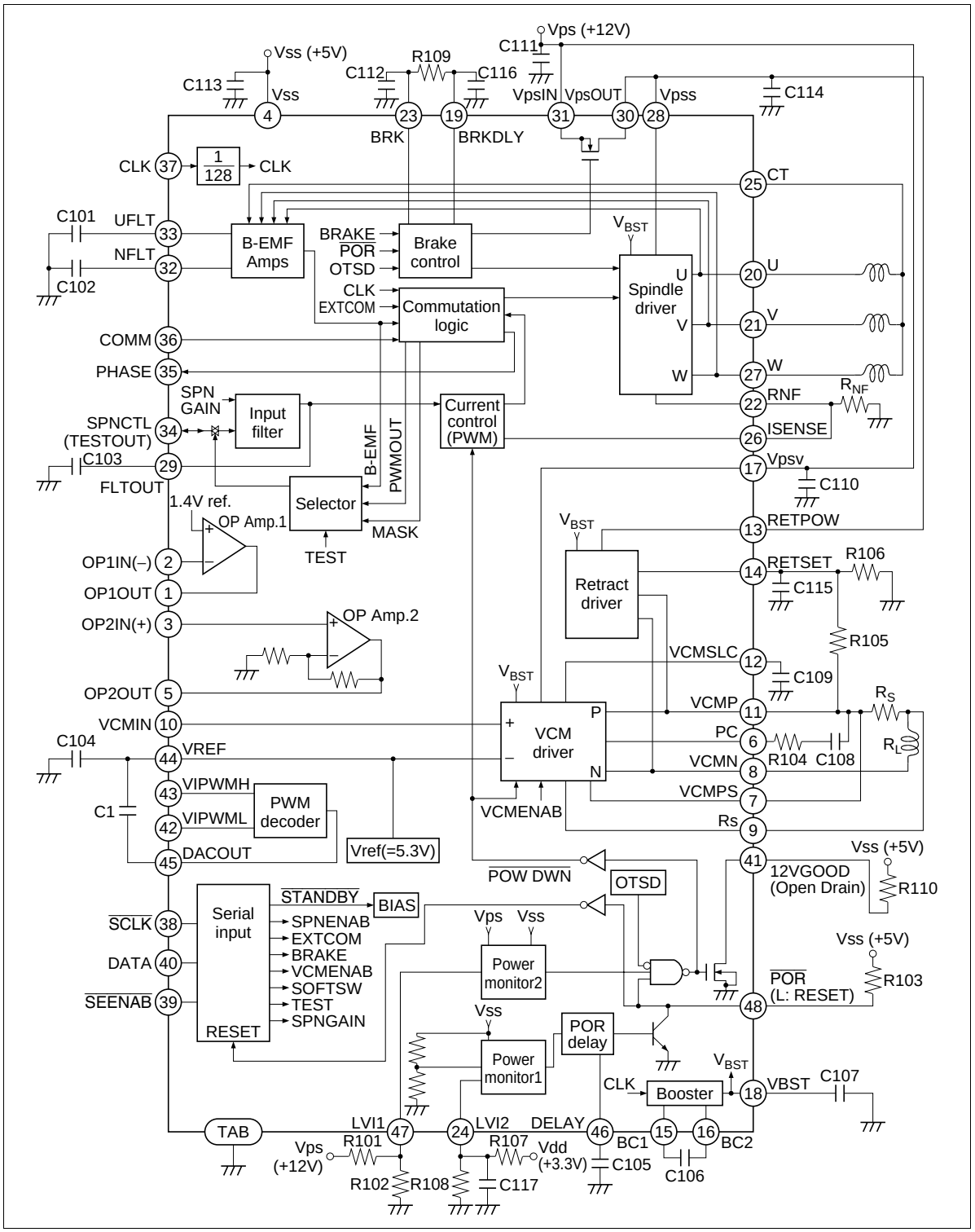
Pin Description

Pin No.	Pin Name	Function
1	OP1OUT	Output of OP amp. 1
2	OP1IN(–)	Inverted input of OP amp. 1
3	OP2IN(+)	Non-inverted input of OP amp. 2
4	Vss	Power supply for +5 V
5	OP2OUT	Output of OP amp. 2
6	PC	External time costant connection terminal for phase compensation of VCM driver
7	VCMPS	Current sensing terminal for VCM driver
8	VCMN	Output of VCM driver (Inverted output of VCMP)
9	Rs	Current sensing terminal for VCM driver (differential input for VCMPS)
10	VCMIN	Input of VCM driver (differential input for VREF)
11	VCMP	Output of VCM driver (inverted output of VCMN)
12	VCMSLC	External capacitor connection terminal for stabilizing internal reference voltage of VCM driver
13	RETPOW	Power supply terminal of retract driver
14	RETSET	Output voltage set up terminal of retract driver
15	BC1	External capacitor connection terminal for pumping of booster
16	BC2	
17	Vpsv	+12 V power supply for VCM driver
18	VBST	Output of booster circuit
19	BRKDLY	Time constance set up terminal of delayed brake
20	U	U-phase output of spindle motor driver
21	V	V-phase output of spindle motor driver
22	RNF	Current sensing terminal for spindle motor driver
23	BRK	External capacitor connection terminal for power off brake
24	LVI2	Resistor connection terminal for set up the threshold of +3.3 V power monitor
25	CT	Center tap connection terminal for spindle motor
26	ISENSE	Input of PWM comparator
27	W	W-phase output of spindle motor driver
28	Vpss	+12 V power supply for spindle motor driver
29	FLTOUT	PWMDAC output for current control of spindle motor driver
30	VpsOUT	Output of power supply switch
31	VpsIN	Input of power supply switch (+12 V)
32	NFLT	Output of pre-filter for B-EMF sensing (capacitor connection terminal)
33	UFLT	

Pin Description (cont)

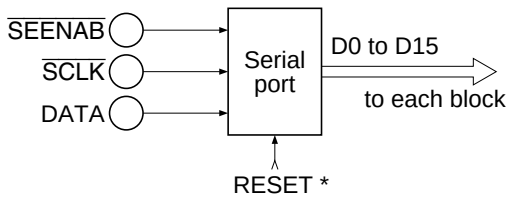
Pin No.	Pin Name	Function
34	SPNCTL	PWMDAC input for current control of spindle motor driver
35	PHASE	Toggle signal output for zero-crossing timing of B-EMF
36	COMM	Commutation signal input for spindle motor driver during synchronous driving
37	CLK	Master clock input of commutation logic circuit
38	$\overline{\text{SCLK}}$	Clock input of serial port for data strobe
39	$\overline{\text{SEENAB}}$	Enable signal input of serial port
40	DATA	Data signal input of serial port
41	12VGOOD	Output of power monitor for +12 V power supply (open drain)
42	VIPWML	PWMDAC input for current control of VCM driver
43	VIPWMH	
44	VREF	Output of internal reference voltage
45	DACOUT	PWMDAC output for current control of VCM driver
46	DELAY	Capacitor connection terminal for set up the power on reset time
47	LVI1	Resistor connection terminal for set up the threshold of +12 V power monitor
48	$\overline{\text{POR}}$	Output of power on reset signal
TAB	GND	Ground of this IC

Block Diagram



Serial Port

Construction



Note: When $\overline{POR}$ = Low, internal RESET signal becomes High and when RESET = High, all bit of serial port are set up default value as shown in table 2.

Figure 1 Construction of Serial Port

Table 1 Truth Table of Internal RESET Signal

Input	Output	Note
$\overline{POR}$	RESET	
Low	High	1
Open	Low	1

Note: 1. When +5 V or +3.3 V power supply goes to Low, then $\overline{POR}$ = Low.
$\overline{POR}$ output is able to construct the wired logic with external signal.

Input Data

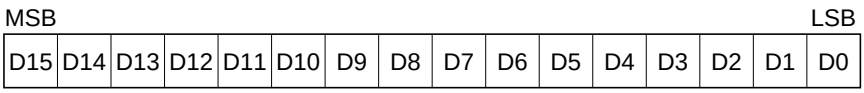


Figure 2 Input Data

The serial port is required the 16 bits data (D0 to D15). When the data length is less than 16 bits, the internal register will not be up dated. And when the data length is more than 16 bits, this register will take later 16 bits and ignore the faster bit.

Bit Assingnment

Table 2 Bit Assingnment of Serial Port

Bit	Symbol	1 (= High)	0 (= Low)	Default	Note
D0	$\overline{\text{STANDBY}}$	Active	Stand by	0	1
D1	VCMENAB	VCM enable	VCM disable	0	1
D2	SPNENAB	Spindle enable	Spindle disable	0	1
D3	BRAKE	Brake enable	Brake disable	0	1
D4	SENSEN	B-EMF sense enable	B-EMF sense disable	0	2
D5	VARCNT	Variable count	Normal count	0	2
D6	EXTCOM	External commutation	Internal commutation	0	2
D7	SRCTL1	High slew rate	Low slew rate	0	3
D8	SRCTL2	Commutation time select (See table 4)		0	4
D9	SRCTL3			0	4
D10	OFFTIME1	Off time select of PWM drive (See table 5)		0	5
D11	OFFTIME2			0	5
D12	SPNGAIN	High gain	Low gain	0	6
D13	RETRACT	Retract	Not retract	0	1
D14	TEST1	For testing		0	7
D15	TEST2			0	7

Note:
1. The priority of operation for each bit is as shown in table 3.
2. This bit is using for start up of spindle motor. Please refer to the application note explained about start up of spindle motor.
3. The slew rate during every commutation of spindle motor is selectable by using this bit. Please select the suitable value of this bit for your motor.
4. This bit is used for setting up the commutation time (refer to figure 9) of spindle motor as shown in table 4.
5. This bit is used for setting up the off time at PWM driving of spindle motor as shown in table 5.
6. The gain of current control for spindle motor is selectable by using this bit. Please select the suitable value of this bit for your motor.
7. This bit will be used in fabrication test. Please set up D15 = “0” normally.
   SPNCTL terminal (pin 35) is using for output terminal in the case of “1” for testing. Then please do not input signal into pin 35 from outside.

Table 3 Truth Table

Input							Driver Output			
OTSD	12VGOOD *1	$\overline{\text{STANDBY}}$	SPNENAB	BRAKE	RETRACT	VCMENAB	Spindle Driver	VCM Driver	Retract Driver	Power Switch
Enable	Low	×*2	×	×	×	×	Braking	Cut off	On	Cut off
Disable	Low	×	×	×	×	×	Braking	Cut off	On	Cut off
Disable	High	Low	×	×	×	×	Braking	Cut off	Cut off	Cut off
Disable	High	High	0	0	0	0	Cut off	Cut off	Cut off	On
Disable	High	High	0	1	0	0	Braking	Cut off	Cut off	On
Disable	High	High	1	×	0	0	On	Cut off	Cut off	On
Disable	High	High	0	0	0	1	Cut off	On	Cut off	On
Disable	High	High	0	1	0	1	Braking	On	Cut off	On
Disable	High	High	1	×	0	1	On	On	Cut off	On
Disable	High	High	0	0	1	×	Cut off	Cut off	On	On
Disable	High	High	0	1	1	×	Braking	Cut off	On	On
Disable	High	High	1	×	1	×	On	Cut off	On	On

Note: 1. The 12VGOOD terminal is open drain output type. The 12VGOOD signal output is determined by the power monitor output for 12 V power supply, $\overline{\text{POR}}$ output and OTSD signal as shown in the table below.

12 V Supply	$\overline{\text{POR}}$	OTSD	12VGOOD
Cut off	×	×	Low
×	Low	×	Low
×	×	Enable	Low
Normal	High	Disable	High

2. The symbol "×" means "Don't care".

Table 4 Commutation Time

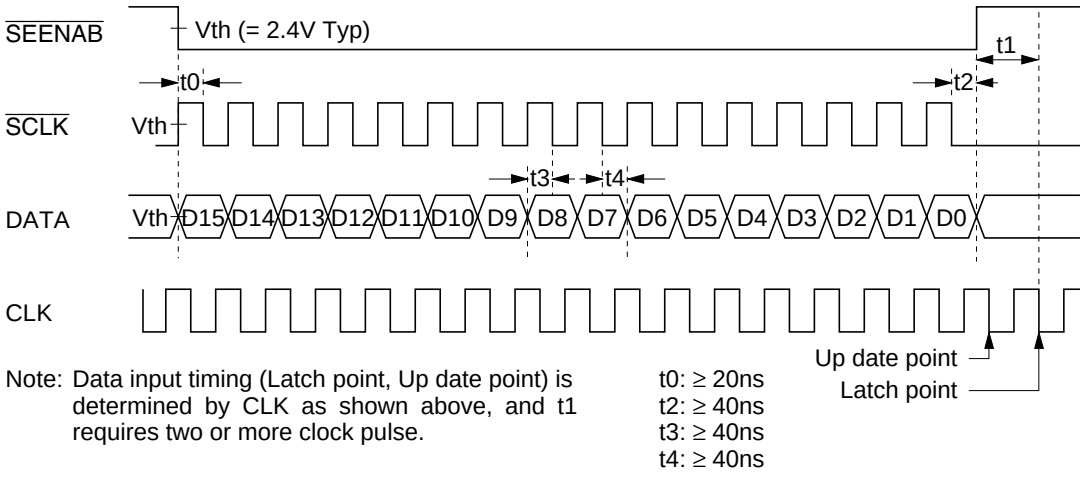
SRCTL2	SRCTL3	Commutation Time (s)
0	0	24 × (128 / fclk)
0	1	16 × (128 / fclk)
1	0	12 × (128 / fclk)
1	1	No slew rate control

Note: The "fclk" is the frequency on pin "CLK". (Recommendation: 20 MHz)

Table 5 OFF Time at PWM Drive

OFFTIME1	OFFTIME2	OFF Time (s)
0	0	1 × (32 / fclk) + (4 / fclk)
0	1	2 × (32 / fclk) + (4 / fclk)
1	0	3 × (32 / fclk) + (4 / fclk)
1	1	4 × (32 / fclk) + (4 / fclk)

Data Input Timing



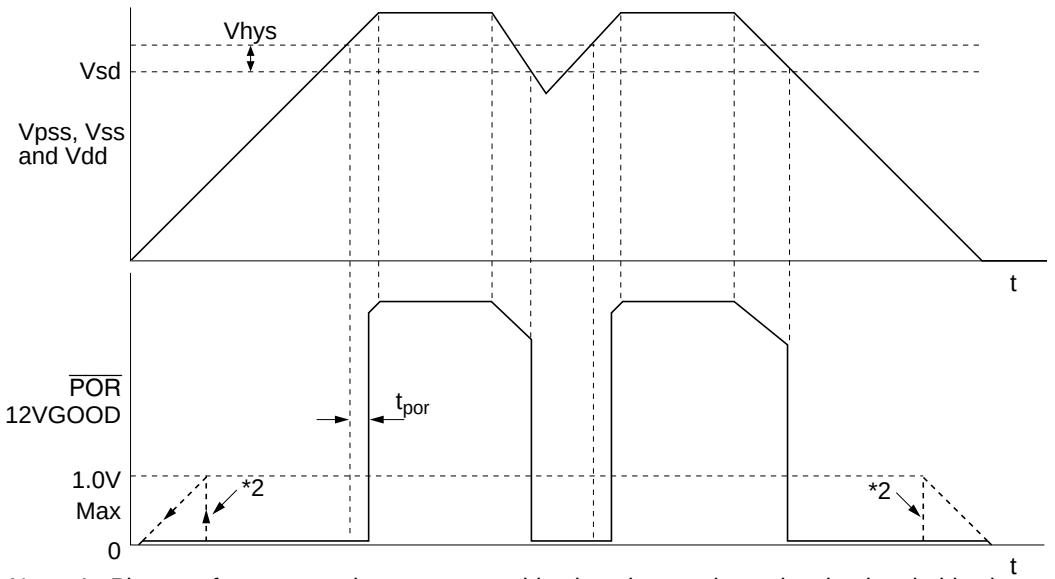
Note: Data input timing (Latch point, Up date point) is determined by CLK as shown above, and t1 requires two or more clock pulse.

t0: ≥ 20ns
t2: ≥ 40ns
t3: ≥ 40ns
t4: ≥ 40ns

Figure 3 Input Timing of Serial Port

Timing Chart

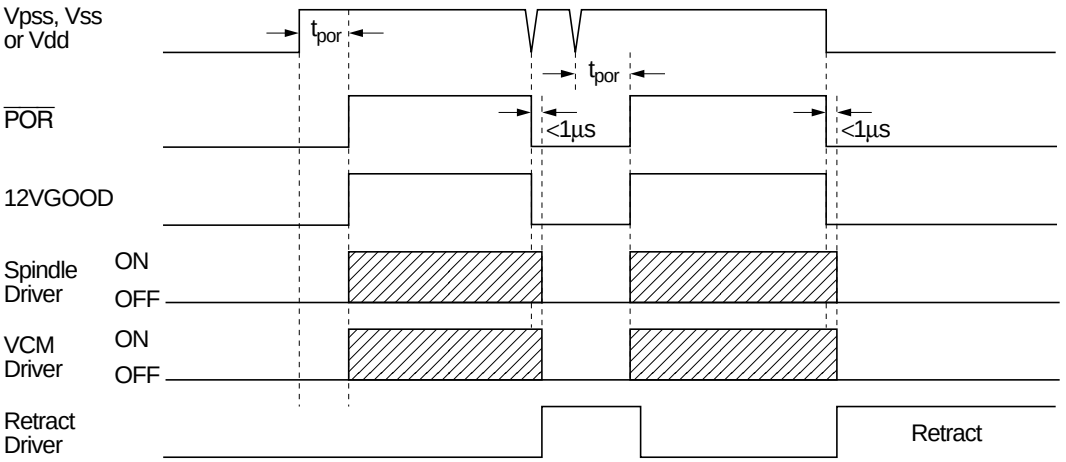
Power on Reset (1)



Note: 1. Please refer to external components table about how to determine the threshold voltage Vsd and delay time t_{por}.
2. Operation for Vss.

Figure 4 Operation of the Power Monitor (1)

Power on Reset (2)



Note: This retract driver requires the electrical power from B-EMF of spindle motor.

Figure 5 Operation of the Power Monitor (2)

Power on Reset (3)

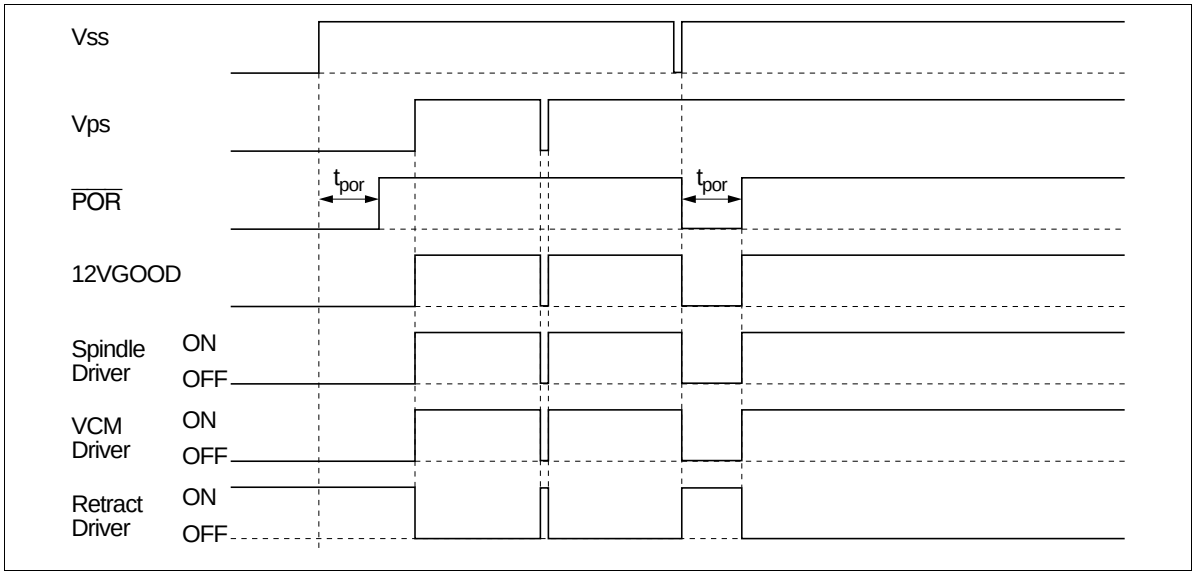
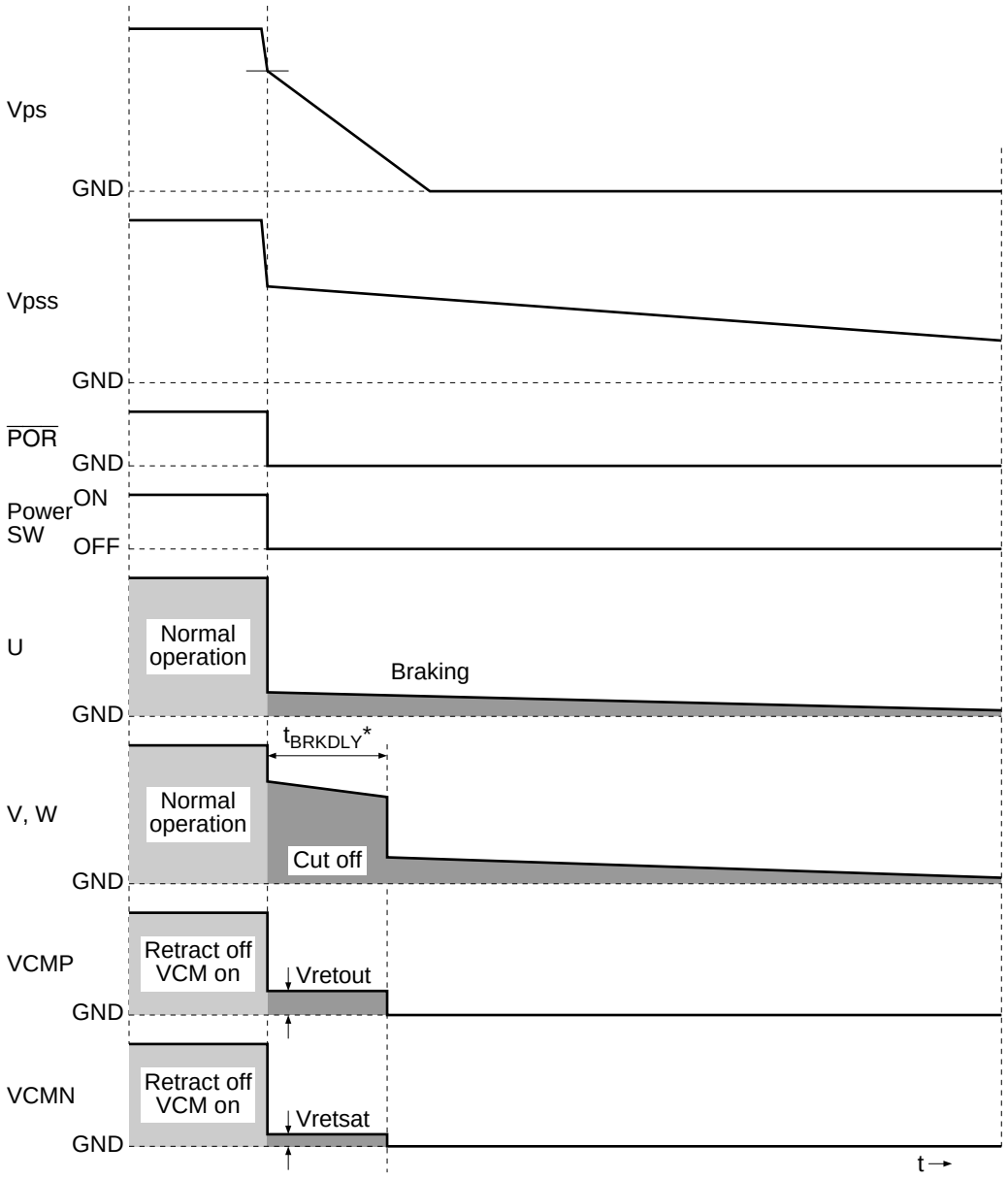


Figure 6 Operation of the Power Monitor (3)

Power Off Retract & Brake

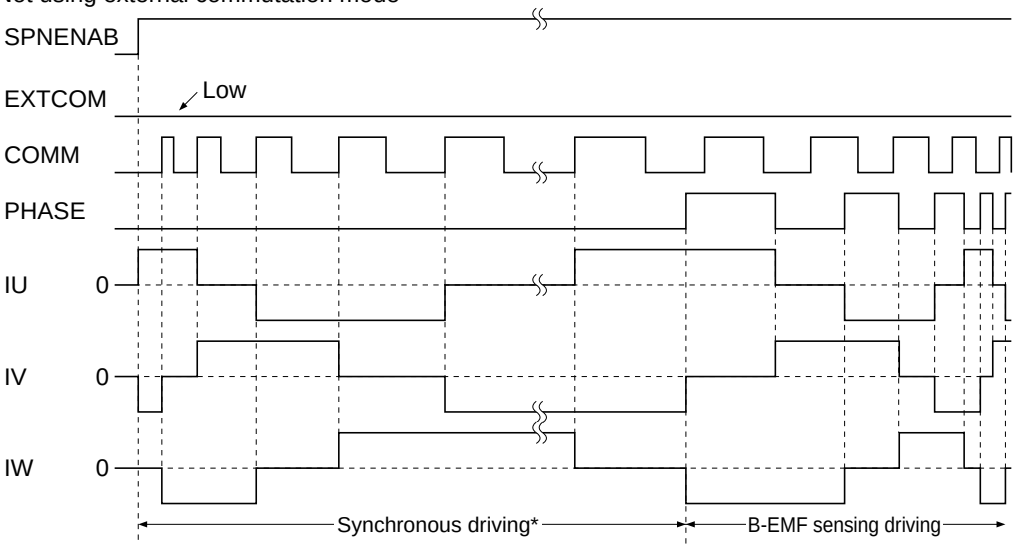


Note: Please see the External Component table about setting delay time t_{BRKDLY}.

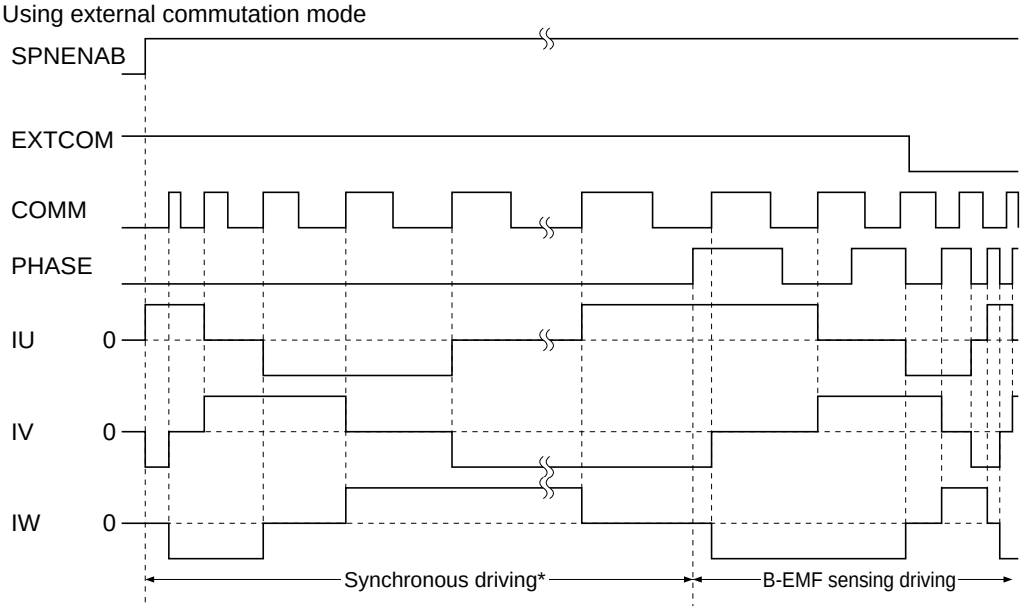
Figure 7 Operation of Power Off Retract & Brake

Start-up of the Spindle motor

• Not using external commutation mode



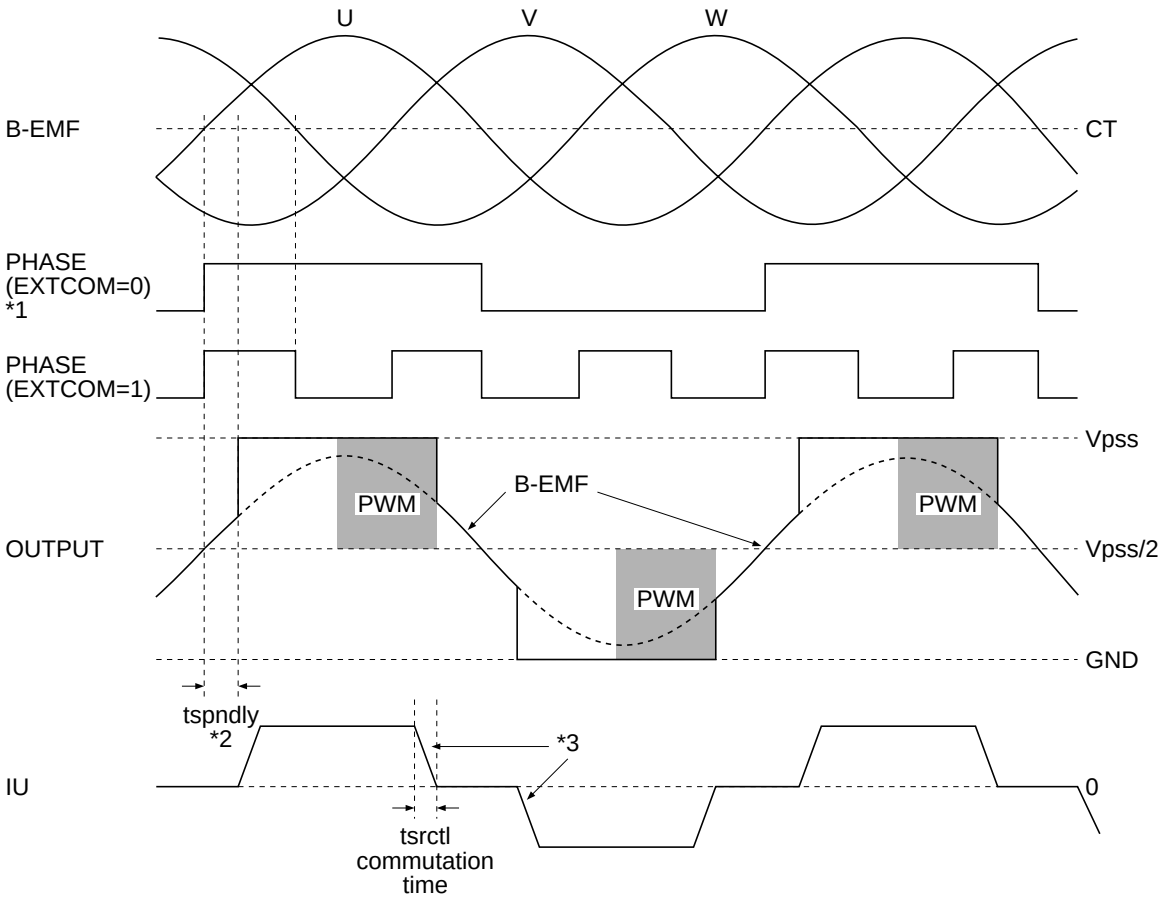
• Using external commutation mode



Note: "Synchronous driving" is defined as the period after changing SPNENAB = L to H until the first positive edge of the PHASE signal.

Figure 8 Start-up of the Spindle Motor

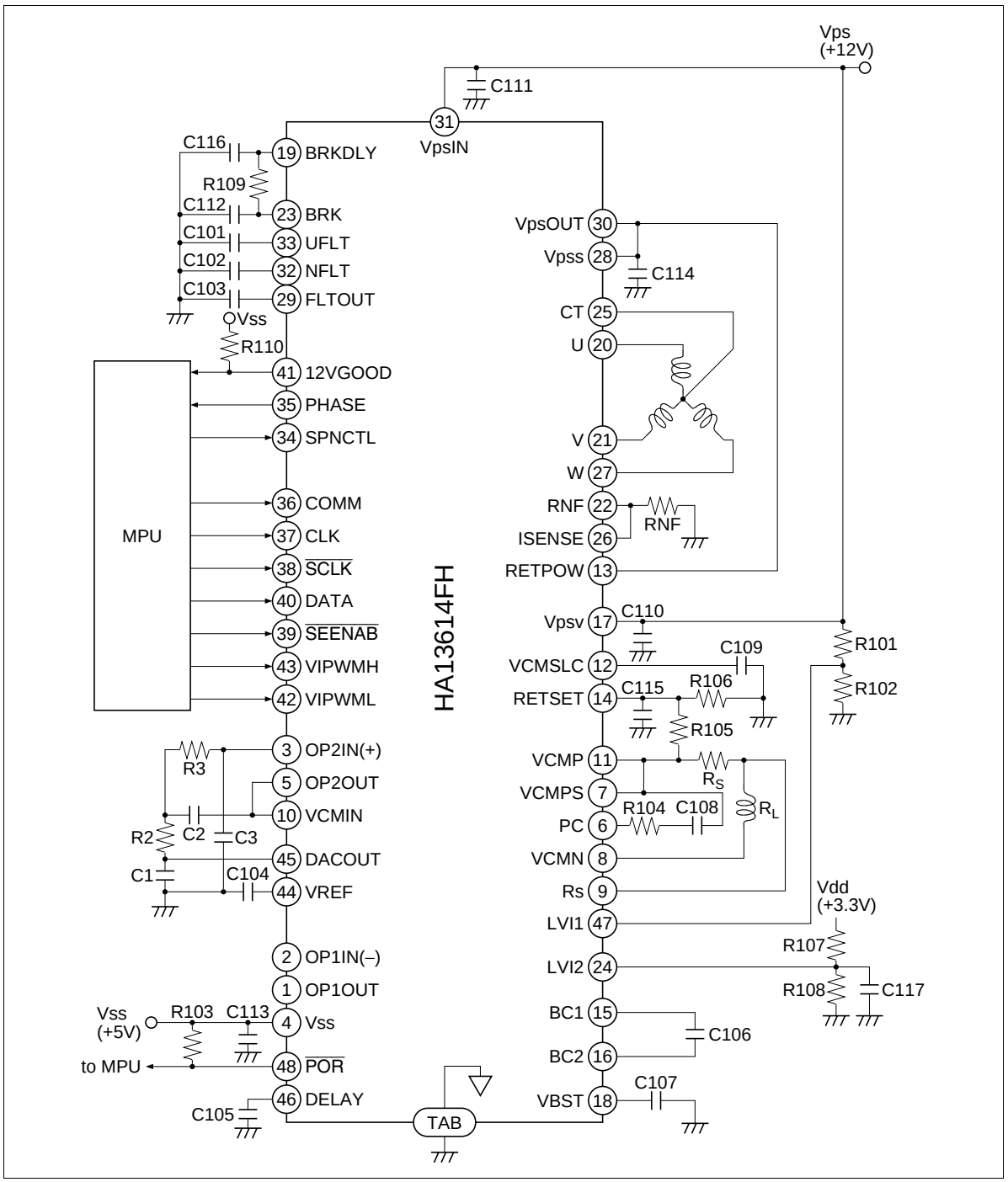
Commutation Timing of the Spindle motor



Note: 1. In the case of external commutation mode (EXTCOM=1), the signal PHASE will toggle at every B-EMF zero-crossing, and selected the internal commutation mode (EXTCOM=0), the PHASE will have the same period as B-EMF of the spindle motor.
2. This is delay time by pre-LPF of the B-EMF amplifier. This delay time can be adjust by the value of external filter capacitor C101, C102. To get the maximum driving efficiency of the spindle motor, these capacitor value should be chosen as equation (17) in the “External components” section.
3. The slew rate of every commutation timing is controllable by changing the SRCTL1, SRCTL2 and SRCTL3 in the serial port.

Figure 9 Commutation Timing of the Spindle motor

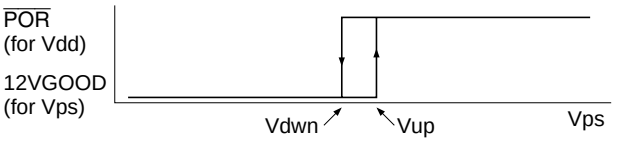
Application



External Components

Parts No.	Recommendation Value	Purpose	Note
R101	—	Set up threshold of power monitor for Vps	1
R102	—		
R103	≥ 5.6 kΩ	Pull up for POR terminal	
R104	—	Gain dumping for VCM driver	5
R105	—	Set up output voltage of retract driver for pin VCMP	6
R106	—		
R107	—	Set up threshold of power monitor for Vdd	1
R108	—		
R109	—	Set up time constance of delayed brake	12
R110	≥ 5.6 kΩ	Pull up for 12VGOOD terminal	
R2	—	Filter constant of LPF	3
R3	—		
Rnf	0.33 Ω	Current sensing for spindle motor	7
R_S	0.47 Ω	Current sensing for VCM	4
C101, C102	—	Pre-filter of B-EMF amplifier	10
C103	—	Filter of PWMDAC for current control of spindle motor	9
C104	0.1 μF	Filter of internal reference output	
C105	0.1 μF	Set up delay time of $\overline{\text{POR}}$ signal	8
C106	0.22 μF	Boost up of power supply	
C107	2.2 μF	Stabilizing boost up voltage	
C108	—	Gain dumping for VCM driver	5
C109	0. 1 μF	Stabilizing reference voltage of VCM driver	
C110	0.1 μF	By passing of power supply	
C111	0.1 μF		
C112	—	Keeping brake function	12
C113	0.1 μF	By passing of power supply	
C114	0.1 μF		
C115	—	Stabilizing output voltage of retract driver for pin VCMP	11
C116	—	Set up time constance of delayed brake	12
C117	0.1 μF	Stabilizing LVI2 terminal	
C1	—	Filter constant of LPF	3
C2	—		
C3	—		

Notes: 1. The operation threshold voltage of Vps or Vdd is determined by resistor R101, R102 or R107, R108 as follows.



• for Vps

Recovery voltage $Vup(Vps) = (Vsd1 + Vhys3) \cdot \left(1 + \frac{R101}{R102}\right)$ [V] (1)

Cut off voltage $Vdwn(Vps) = Vsd1 \cdot \left(1 + \frac{R101}{R102}\right)$ [V] (2)

where, Vsd1 : Operating voltage of the power monitor [V] (refer to Electrical Charasteristics)
Vhys3 : Hysteresis voltage of the power monitor [V] (refer to Electrical Charasteristics)

• for Vdd

Recovery voltage $Vup(Vdd) = (Vsd1 + Vhys4) \cdot \left(1 + \frac{R107}{R108}\right)$ [V] (1)'

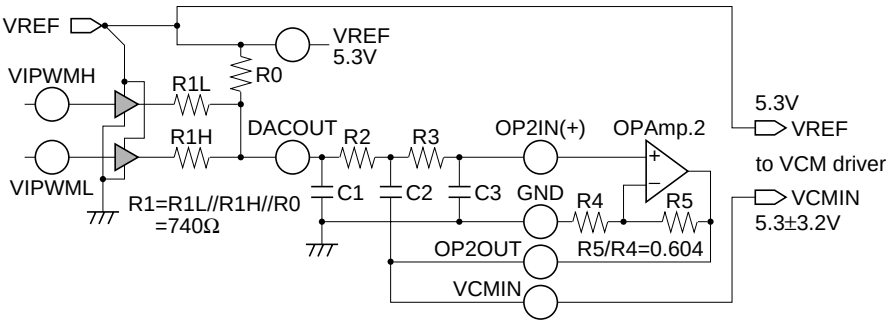
Cut off voltage $Vdwn(Vdd) = Vsd1 \cdot \left(1 + \frac{R107}{R108}\right)$ [V] (2)'

where, Vhys4 : Hysteresis voltage of the power monitor [V] (refer to Electrical Charasteristics)

2. The relation between PWMDAC input VIPWMH, VIPWML for VCM driver current control and VCM driver input (VCMIN – VREF) is determined by following equation. (refer to below figure)

$$VCMIN - VREF = \frac{6.4}{6500} \cdot (64 \cdot DPWMH + DPWML) - 3.2 \quad (3)$$

where, VREF : Internal reference voltage [V] (refer to Electrical Charasteristics)
DPWMH : Duty of input signal on terminal VIPWMH [%]
DPWML : Duty of input signal on terminal VIPWML [%]



3. The 3rd order LPF at next stage of PWMDAC is characterized by internal OP amp. and capacitor C1, C2, C3 and resistor R2, R3. These components value are determined by following equations.

$$C1 = \frac{1}{2 \cdot \pi \cdot fc \cdot R1} \quad [F] \quad (4)$$

$$C3 = 220 \cdot 10^{-12} \quad [F] \tag{5}$$

$$C2 = \frac{1}{2} \cdot \frac{4 \cdot k + 1 - \sqrt{8 \cdot k + 1}}{k^2} \cdot C3 \quad [F] \tag{6}$$

$$R2 = \frac{k}{\sqrt{4 \cdot k + 1 - \sqrt{8 \cdot k + 1}}} \cdot \frac{\sqrt{2}}{2 \cdot \pi \cdot fc \cdot C3} \quad [\Omega] \tag{7}$$

$$R3 = R2 \quad [\Omega] \tag{8}$$

$$k = \frac{R5}{R4} = 0.604 \tag{9}$$

where, fc : Cut off frequency of 3rd order LPF [Hz]
R1 : Output resistance of PWMDAC [Ω] (refer to Electrical Characteristics)

4. The driving current of VCM Ivcm is determined by following equation.

$$Ivcm = \frac{Vvcmin - VREF}{R_S} \cdot Gvcm \quad [A] \tag{10}$$

where, Vvcmin : Input voltage on terminal VCMIN (pin 10) [V]
Gvcm : Transfer function of VCM driver [dB] (refer to Electrical Characteristics)

5. Capacitor C108 and resistor R104 are useful to dump the gain peaking of VCM driver. These components also determine the gain band width of VCM driver BW1 which should be chosen less than 10 kHz, as follows.

$$R104 = \frac{12\pi \cdot BW1 \cdot Lvcm}{R_S} \quad [k\Omega] \tag{11}$$

$$C108 = \frac{Lvcm}{R_S + R_L} \cdot \frac{1}{R104} \quad [F] \tag{12}$$

where, R_L : Coil resistance of VCM [Ω]
Lvcm : Coil inductance of VCM [H]

6. Retract current Iret is determined by following equation.

$$Iret = \frac{0.7 \times \left(1 + \frac{R105}{R106}\right) - Vretsat}{R_S + R_L} \quad [A] \tag{13}$$

Vretsat : Output saturation voltage of retract driver [V]
(refer to Electrical Characteristics)

7. The relation between duty of input signal on terminal SPCNTL (pin 34) and output current of spindle motor driver Ispn is as follows.

$$Ispn = \frac{Vref - Voff1}{Rnf} \cdot duty \quad [A] \tag{14}$$

Vref : Reference voltage of current control amplifier [V]
Vref = Vref2 (@SPNGAIN = 1)
Vref = Vref3 (@SPNGAIN = 0)
Voff1 : Offset voltage of current control amplifier [V]
(refer to Electrical Characteristics)

8. The delay time of the power monitor for start up is as follows.

$$tpor = 140 \cdot C105 \quad [ms] \tag{15}$$

9. The cut off frequency fcpwm of the filter for current control input of the spindle motor is as follows.

$$fcpwm = \frac{1}{2\pi \times 20k \cdot C103} \quad [Hz] \tag{16}$$

10. To get the maximum driving efficiency for spindle motor, the capacitor C101, C102 should be chosen as following equation.

$$C101 = 0.8 \cdot C102 \tag{17-1}$$

$$C102 = \frac{\tan(\pi/6)}{2\pi \cdot 13k} \cdot \frac{1}{fbemf} \quad [F] \tag{17-2}$$

fbemf : Back EMF frequency at standard rotation speed of the spindle motor [Hz]

where, please set the value of C101, C102 so that C101 < C102 can be kept including the accuracy of the absolute value to assure the stability of motor starting and speed lock state.

11. To stabilize output voltage od retract driver, the capacitor C115 should be chosen as following equation. Please chose same values for C115.

$$C115 = \frac{3 \cdot 10^{-6}}{2\pi \cdot (R105 \,//\, R106)} \quad [F] \tag{18}$$

12. Time t_{BRKDLY} of the delayed brake of V, W phase for retract is determined by resistor R109 and capacitor C112, C116 as following equation.

$$t_{BRKDLY} = -\frac{C116 \cdot R109}{1 + \frac{C116}{C112}} \cdot \ln\left[1 - \frac{Vthb}{V_{BRK0}} \cdot \left(1 + \frac{C116}{C112}\right)\right] \quad [s] \tag{19}$$

where, Vthb : Threshold voltage that output MOS transistor of spindle motor driver is operated.

$V_{BRK0} = Vpss - 0.7$ [V]

Vpss : +12 V power supply for spindle motor driver

and, please select capacitor C112 and C116 that the ratio of C112/C116 is more than 3 times, because the last voltage of BRK and BRKDLY terminals falls if the value of C116 is big for C112, and effect of brake goes down.

Absolute Maximum Ratings

Item	Symbol	Rating	Unit	Note
Power supply	Vss	6.0	V	1
	Vpss	15	V	2
	Vpsv	15	V	2
Spindle current	Ispn	2.0	A	3
VCM current	Ivcm	1.5	A	3
Input voltage	Vin	–0.33 to Vss +1.0	V	4
Power dissipation	P_T	5.0	W	5
Junction temperature	Tj	150	℃	6
Storage temperature	Tstg	–55 to +125	℃	

Notes: 1. Operating voltage range is 4.25 V to 5.5 V. If power supply voltage exceed this operating range in actual application, the reliability of this IC can not be guaranteed.
2. Operating voltage range is 10.2 V to 13.8 V.
3. ASO (Area of Safety Operation) of each output transistor is shown in figure 10.
Operating locus must be within the ASO.
4. Applied to CLK, COMM, SPNCTL, VIPWMH, VIPWML, $\overline{\text{SCLK}}$, DATA and $\overline{\text{SEENAB}}$.
5. Thermal resistance θj-a ≤ 30°C/W (Using 4 layer glass epoxy board)
6. Operating junction temperature range is 0°C to +125°C.

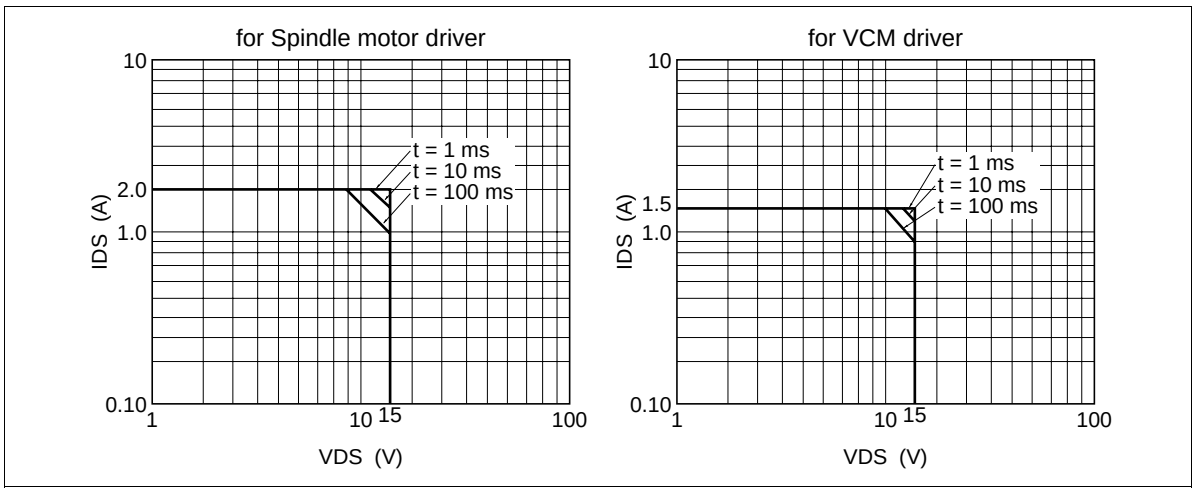


Figure 10 ASO of Output Transistor

Electrical Characteristics (Ta = 25°C, Vss = 5 V, Vpss = Vpsv = 12 V)

Item		Symbol	Min	Typ	Max	Unit	Test Conditions	Applicable Pins	Note
Supply current		Iss0	—	2.0	3.4	mA	Stand by, fclk=20MHz	Vss	
		Iss1	—	3.2	4.2	mA	fclk=20MHz		
		Ips0	—	1.6	2.4	mA	Stand by	Vpss & Vpsv	1
		Ips1	—	42	56	mA			
Power switch	Output on resistance	Ron0	—	0.2	0.3	Ω		VpsIN VpsOUT	
	Output leacage current	Icer0	—	—	±10	µA	VpsOUT=15V, VpsIN=0V, Vss=0V, Vpss=Vpsv=0V		
Logic input	Input low current	Iil1	—	—	±10	µA	Vil=0V	CLK, COMM,	
	Input high current	Iih1	—	—	±10	µA	Vih1=5V	$\overline{\text{SCLK}}$, DATA,	
	Input low voltage	Vil1	—	—	0.8	V		$\overline{\text{SEENAB}}$, VIPWMH,	
	Input high voltage	Vih1	2.0	—	—	V		VIPWML, SPNCTL	
	Clock frequency	fclk	19	—	21	MHz			
Logic output1	Output high voltage	Voh1	4.6	—	—	V	Ioh=1mA	PHASE	
	Output low voltage	Vol1	—	—	0.4	V	Iol=2mA		
Logic output2	Output leakage current	Icer1	—	—	±10	µA	Vo=5.5V	$\overline{\text{POR}}$, 12VGOOD	5
	Output low voltage	Vol2	—	—	0.4	V	Iol=2mA		

Electrical Characteristics (Ta = 25°C, Vss = 5 V, Vpss = Vpsv = 12 V) (cont)

Item		Symbol	Min	Typ	Max	Unit	Test Conditions	Applicable Pins	Note
Spindle motor driver	Output on resistance	Ron1	—	1.2	1.5	Ω	Io≤1.5A	U, V, W	2
	On resistance during braking	Ron2	—	—	3.0	Ω	Io=0.4A, BRK=3V		
	Output leakage current	Icer3	—	—	±2	mA	Vo=15V		
	Output clamp diode forward voltage	Vf	—	0.9	1.2	V	If=0.5A		
	Output MOS operating threshold voltage	Vthb	—	2	—	V	Ron=(Ron/2)×10		
	Leakage current on brake terminal	Icer4	—	—	0.6	µA	Vpsv=GND, Vo=8V	BRK, BRKDLY	
	Input filter & current control amp.	Vref2	—	490	±10%	mV	SPNGAIN=1, SPNCTL=Vss	ISENSE, FLTOUT	
		Vref3	—	250	±10%	mV	SPNGAIN=0, SPNCTL=Vss		
	Current control amp. offset voltage	Voff1	—	–10	±20	mV	SPNCTL=GND		
B-EMF amp.	Input offset voltage	Voff2	—	—	±20	mV	Synchronous drive	U, V, W, UFLT, NFLT	
		Voff3	—	—	±20	mV	B-EMF sens drive		
	Input hysteresis voltage	Vhys1	70	90	110	mVp-p	Synchronous drive		
		Vhys2	35	45	55	mVp-p	B-EMF sens drive		

Electrical Characteristics (Ta = 25°C, Vss = 5 V, Vpss = Vpsv = 12 V) (cont)

Item		Symbol	Min	Typ	Max	Unit	Test Conditions	Applicable Pins	Note
VCM driver	Output on resistance	Ron2	—	1.4	1.8	Ω	Io≤1.0A	VCMP, VCMN	2
	Output leakage current	Icer5	—	—	±2	mA	Vo=15V		
	Output quiescent voltage	Vq	—	Vpsv/2	±5%	V	R_S=0.47Ω, R_L=10Ω, L=2mH, R104=1.6MΩ, C108=120pF		
	Transfer gain	Gvcm	—	–18	—	dB		VCMPS, Rs	4
	Gain band width	BW1	—	10	—	kHz			
	Input resistance	Rin	—	60	±30%	kΩ		VCMIN	
PWM DAC	Input minimum pulse width	Tpwm	50	—	—	ns		VIPWMH, VIPWML	
	Output resistance	R1	—	740	±30%	Ω		FLTOUT	
	Output voltage	Vo1	—	0.4	±10%	V	VIPWMH=High, VIPWML=High	VCMPS, Rs	3
		Vo2	—	0.4	±10%	V	VIPWMH=Low, VIPWML=Low		
	Output offset voltage	Voff4	—	—	±10	mV			
	Gain ratio	Rat	—	64	±2%	—	Rat=VIPWMH/ VIPWML		
	Reference voltage	Vref	—	5.3	±5%	V	Io=±1mA	VREF	
Retract driver	Retract driver output voltage	Vretout	—	1.0	±8%	V	Vpss=6.0V, R105=13k Ω, R106=33k Ω, R_L=10 Ω, R_S=0.47 Ω	VCMP	
	VCMN output saturation voltage	Vretsat	0.1	0.2	0.4	V		VCMN	

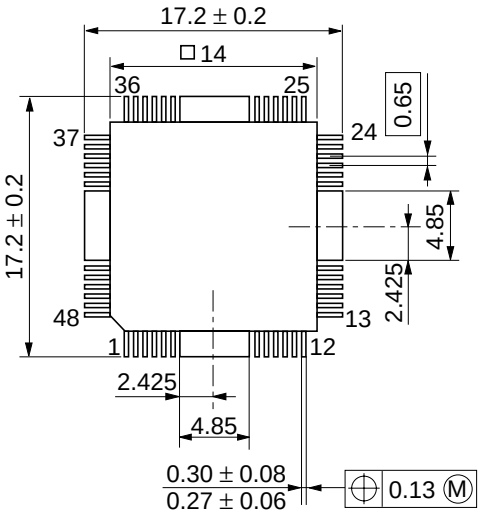
Electrical Characteristics (Ta = 25°C, Vss = 5 V, Vpss = Vpsv = 12 V) (cont)

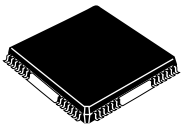
Item		Symbol	Min	Typ	Max	Unit	Test Conditions	Applicable Pins	Note
Power monitor	Operating voltage	Vsd1	—	1.415	±3%	V		LVI1, LVI2	
	Hysteresis	Vhys3	—	60	—	mV		LVI1	
		Vhys4	—	30	—	mV		LVI2	
	Cut off voltage	Vsd2	4.1	—	—	V		Vss	
	Recovery voltage	Vrec	—	—	4.4	V			
	POR delay time	tpor	10	14	20	ms	C105=0.1µF	$\overline{\text{POR}}$	
OP amp.1	Output resistance	Rout2	—	—	10	Ω	Shorted between OP1OUT and OP1IN(–)	OP1OUT	
	Output maximum current	Iomax1	—	—	±1	mA			
	Output voltage deviation	Vdev	—	1.415	±3%	V			
	Input bias current	IB1	—	—	±10	nA		OP1IN(–)	
	Gain band width	BW2	—	1.0	—	MHz		OP1OUT	
OTSD	Operating temperature	Tsd	125	150	—	°C			4
	Hysteresis	Thys	—	25	—	°C			

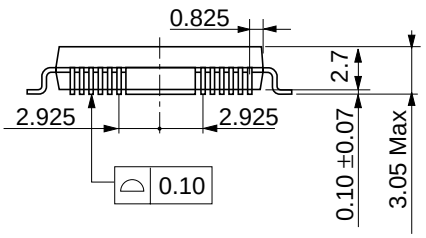
Note: 1. Specified by sum of supply current to Vpss and Vpsv terminal.
2. Specified by sum of saturation voltage and lower saturation voltage.
3. Specified by differential voltage on both side of R_S at shorting between DACOUT and OP2IN(+), and between OP2OUT and VCMIN, respectively.
4. Guaranteed by design.
5. The 12VGOOD terminal is open drain output type.

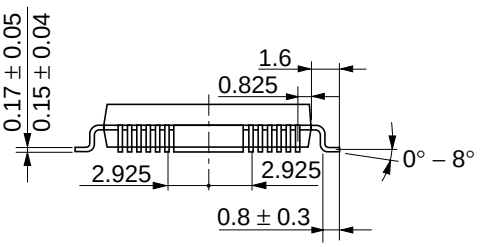
Package Dimensions

Unit: mm









Hitachi Code	FP-48T
JEDEC	—
EIAJ	—
Weight (reference value)	1.2 g

Dimension including the plating thickness
Base material dimension

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