NIPPON PRECISION CIRCUITS INC.

SM1126 Series

Melody IC with Built-in SRAM

OVERVIEW

The SM1126 Series are melody ICs for use in mobile telecommunications equipment. A maximum of 15 melodies can be stored in programmable ROM and one in built-in read/write SRAM.

FEATURES

- 2.0 to 3.6 V supply voltage
- Maximum of 16 melody selections (15 in ROM + 1 in SRAM)
- Level hold playback mode
- External reference clock input versions and built-in RC oscillator versions available, set by master-slice option (RC oscillator versions require an external resistor and capacitor).
- Selectable clock frequencies (fixed for all melodies)
  - External clock input versions (6 frequencies)
    - 32.768 kHz system: 32.768, 65.536 and 131.072 kHz
    - 38.4 kHz system: 38.4, 76.8 and 153.6 kHz
  - Built-in RC oscillator versions (1 frequency)
    - 131.072 kHz
- 2-pin serial data melody selection and 1-pin melody playback control
- Parity check function
- Delivery pattern alarm
- Power save function
  - External clock input versions
    Clock gating in non-play modes
  - Built-in RC oscillator versions
    Oscillator stopped in non-play modes

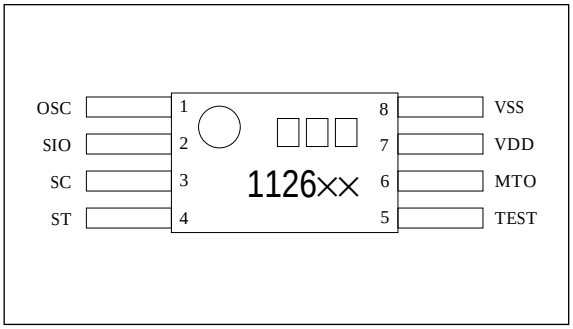
ORDERING INFORMATION

Device	Package
SM1126××V	8-pin VSOP

PINOUT

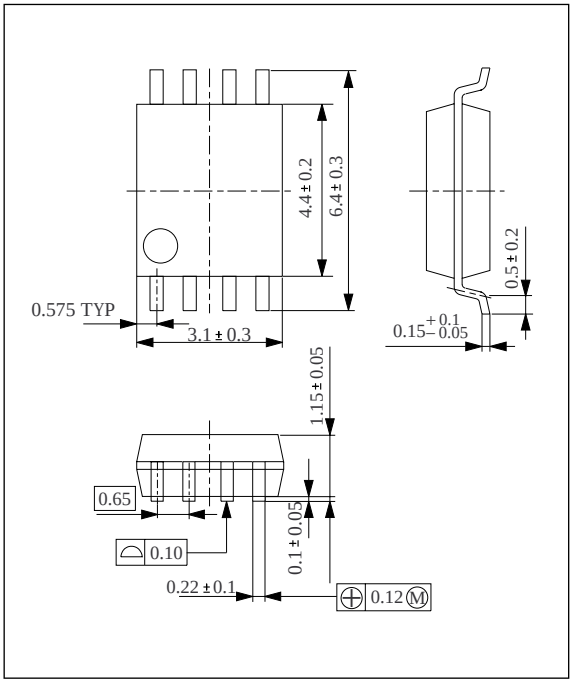
(Top View)

8-pin VSOP

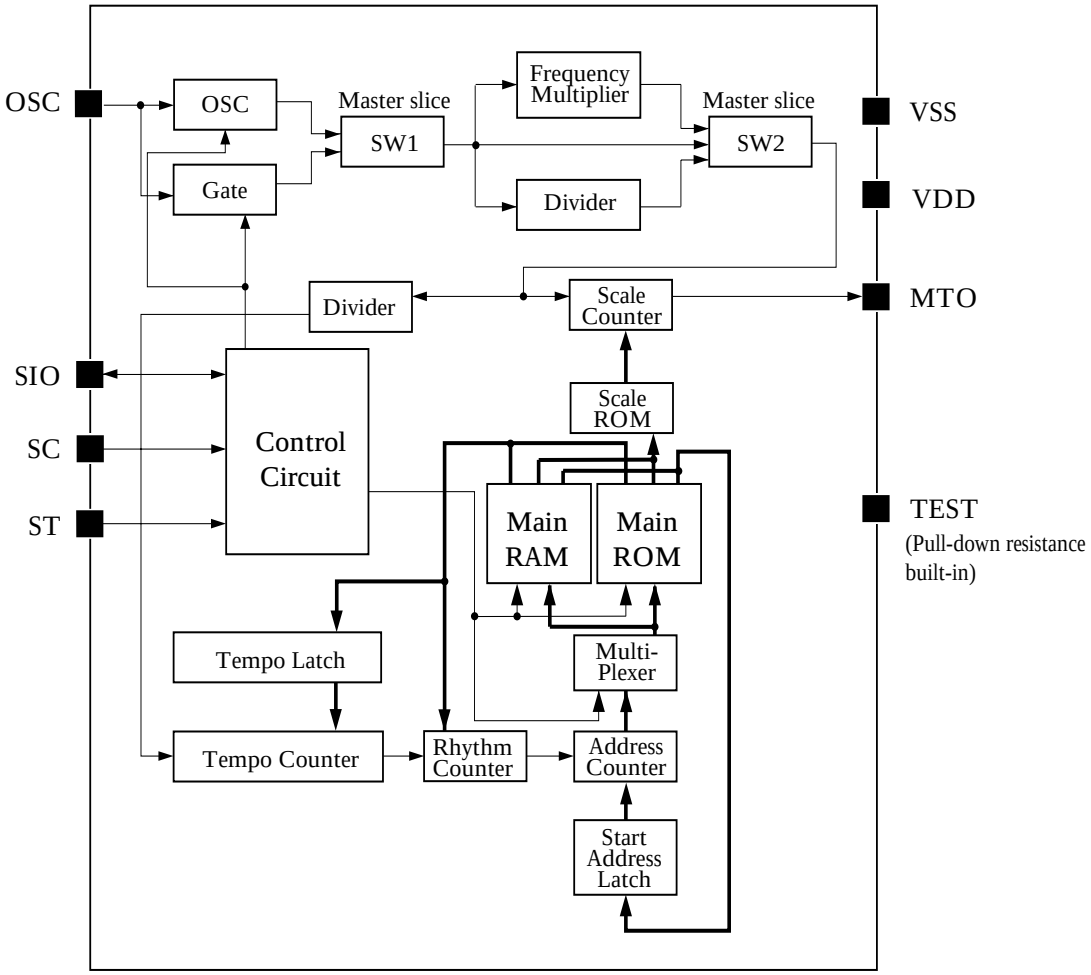


PACKAGE DIMENSIONS

(Unit: mm)



BLOCK DIAGRAM



PIN DESCRIPTION

Number	Name	Function
1	OSC	Built-in RC oscillator option: External resistor and capacitor connection pins External clock input option: External reference clock input (gate circuit built-in)
2	SIO	Playback control serial interface data input. During parity check, the G flag is output while ST is HIGH.
3	SC	Playback control serial interface clock input
4	ST	Play mode: Playback start/stop control signal input Write mode: Serial interface data write control signal input
5	TEST	Test input. Pull-down resistor built-in. Leave open or connect to VSS.
6	MTO	Playback melody signal output
7	VDD	Supply
8	VSS	Ground

SPECIFICATIONS

Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating	Unit
Supply voltage range	$V_{DD} - V_{SS}$		–0.3 to 5.0	V
Input voltage range	V_{IN}		V_{SS} – 0.2 to V_{DD} + 0.2	V
Power dissipation	P_D		100	mW
Storage temperature range	T_{stg}		–40 to 125	°C
Soldering temperature	T_{sld}		255	°C
Soldering time	t_{sld}		10	s

Recommended Operating Conditions

V_{SS} = 0 V

Parameter	Symbol	Condition	Rating	Unit
Supply voltage	V_{DD}		2.0 to 3.6	V
Operating temperature	T_{opr}		–20 to 70	°C

DC Characteristics

T_a = –20 to 70 °C, V_{SS} = 0 V, V_{DD} = 2.0 to 3.6 V

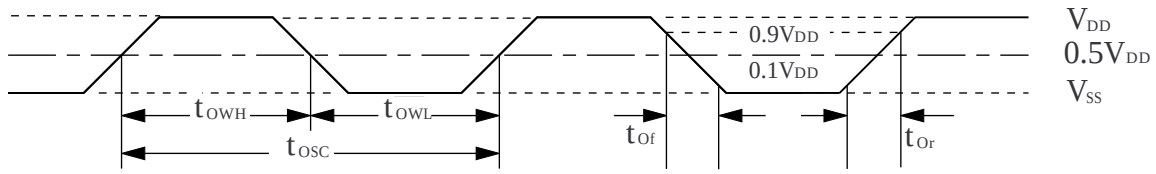
Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
Supply voltage	V_{DD}		2.0	3.0	3.6	V
Current consumption (1)	I_{DD1}	Non-playback mode, T_a = 25°C	–	–	0.5	µA
Current consumption (2)	I_{DD2}	External clock input option: Playback mode, MTO pin open	–	25	200	µA
Current consumption (3)	I_{DD3}	Built-in RC oscillator option: Playback mode, MTO pin open	–	215	600	µA
Input voltage	V_{IH}	External clock input option: ST, SIO, SC and OSC pins, Built-in RC oscillator option: ST, SIO and SC pins	V_{DD} – 0.2	–	V_{DD}	V
	V_{IL}		V_{SS}	–	V_{SS} + 0.2	V
Input current (1)	I_{IH1}	$V_{IH} = V_{DD}$, T_a = 25°C External clock input option: ST, SIO, SC and OSC pins, Built-in RC oscillator option: ST, SIO and SC pins	–	–	0.5	µA
	I_{IL1}	V_{IL} = 0 V, T_a = 25°C External clock input option: ST, SIO, SC and OSC pins, Built-in RC oscillator option: ST, SIO and SC pins	–	–	0.5	µA
Input current (2)	I_{IH2}	TEST pin, $V_{IH} = V_{DD}$	–	–	200	µA
Start voltage	V_{OPN}	TEST pin	–	–	0.1	V
Output voltage (1)	V_{OH1}	SIO pin, I_{OH1} = 1 mA, V_{DD} = 2.4 V	V_{DD} – 0.4	–	V_{DD}	V
	V_{OL1}	SIO pin, I_{OL1} = 1 mA, V_{DD} = 2.4 V	V_{SS}	–	V_{SS} + 0.4	V
Output voltage (2)	V_{OH2}	MTO pin, I_{OH2} = 1 mA	V_{DD} – 0.4	–	V_{DD}	V
	V_{OL2}	MTO pin, I_{OL2} = 1 mA	V_{SS}	–	V_{SS} + 0.4	V
Oscillator frequency	f_{OSC}	Built-in RC oscillator option: NPC test board measurement, V_{DD} = 3.0 V, R_O = 82 kΩ, C_O = 130 pF	117.965	131.072	144.179	kHz
Frequency stability	Δf/f	Built-in RC oscillator option	–	0.2	–	%/0.1V
Oscillator start voltage	V_{DOB}	Built-in RC oscillator option	–	–	1.6	V
Oscillator stop voltage	V_{DOS}	Built-in RC oscillator option	–	–	1.6	V

AC Characteristics

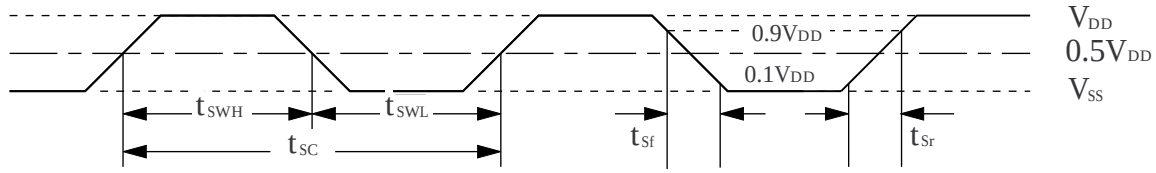
T_a = –20 to 70 °C, V_{SS} = 0 V, V_{DD} = 2.0 to 3.6 V

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
OSC pulse cycle	t_{OSC}	"OSC input pulse (external clock input version)" timing	4.0	–	–	µs
OSC HIGH-level pulsewidth	t_{OWH}		2.0	–	–	µs
OSC LOW-level pulsewidth	t_{OWL}		2.0	–	–	µs
OSC pulse rise time	t_{Or}		–	–	200	ns
OSC pulse fall time	t_{Of}		–	–	200	ns
SC pulsewidth	t_{SC}	"SC input pulse" timing	4.0	–	–	µs
SC HIGH-level pulsewidth	t_{SWH}		2.0	–	–	µs
SC LOW-level pulsewidth	t_{SWL}		2.0	–	–	µs
SC pulse rise time	t_{Sr}		–	–	200	ns
SC pulse fall time	t_{Sf}		–	–	200	ns
SIO-SC setup time	t_{DS}	"SC-SIO-ST serial input pulse" timing	2.0	–	–	µs
SIO-SC hold time	t_{DH}		2.0	–	–	µs
ST input write pulsewidth	t_{WP}		2.0	–	–	µs
ST input write pulse rise time	t_{Wr}		–	–	200	ns
ST input write pulse fall time	t_{Wf}		–	–	200	ns
SIO output enable delay	t_{OE}	"SIO parity check G-flag output data" timing	–	–	600	ns
SIO output disable delay	t_{OD}		–	–	600	ns

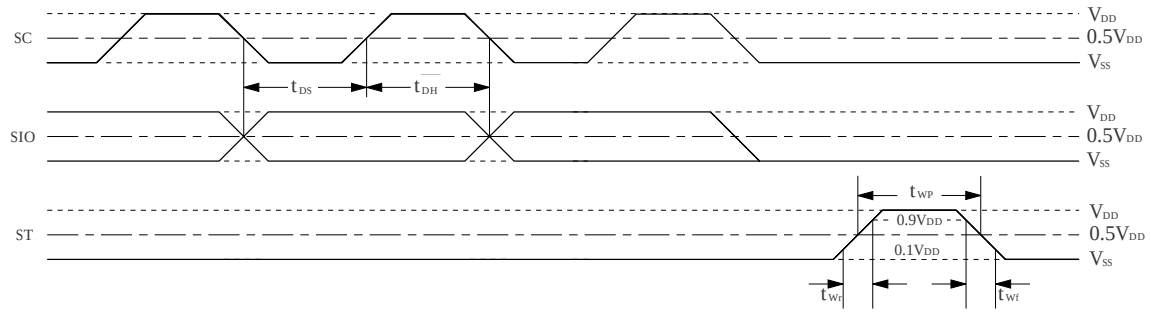
OSC input pulse (external clock input version)



SC input pulse

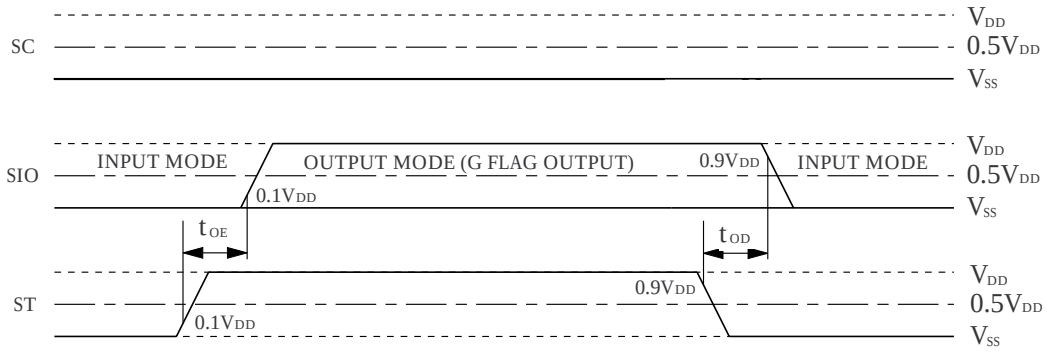


SC-SIO-ST serial input pulse



ST must be set to LOW when switching ST

SIO parity check G-flag output data



ST must be set to LOW when switching ST

FUNCTIONAL DESCRIPTION

Control Functions

External reference clock

SM1126 Series devices are available in external clock input versions and built-in RC oscillator versions, set by master-slice option. In the case of the built-in RC oscillator option, an external resistor and capacitor is required for the oscillator function.

SM1126 Series devices can operate at 6 selectable reference clock frequencies. All melodies playback at the fixed speed set by the reference clock frequency. External clock input versions operate at one of 6 selectable clock frequencies, as shown in table 1. Built-in RC oscillator versions operate at only one oscillator frequencies—131.072 kHz.

Table 1. Reference clock frequencies (external clock)

Frequency system	Selectable frequencies		
32.768 kHz	32.768 kHz	65.536 kHz	131.072 kHz
38.4 kHz	38.4 kHz	76.8 kHz	153.6 kHz

Power-save function

In external clock input versions, the external reference clock input is used during playback mode only and is otherwise ignored. If a clock signal is input when not in playback mode (when ST is LOW), the gate circuit switches to cutoff the external reference clock signal from entering the device, preventing unwanted current flow.

In built-in RC oscillator versions, the oscillator is stopped when not in playback mode (when ST is LOW), preventing unwanted current flow.

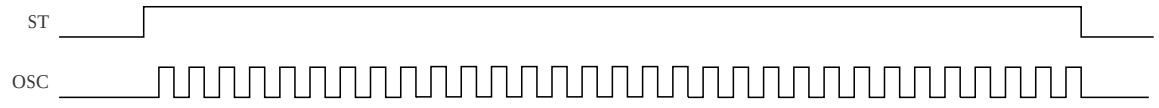


Figure 1. External clock input version: OSC input during playback mode only

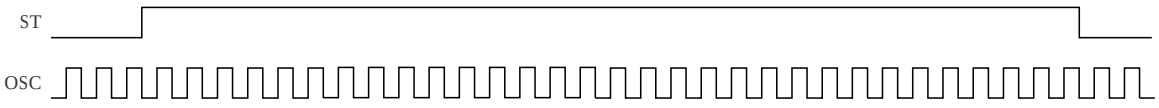


Figure 2. External clock input version: Continuous OSC input

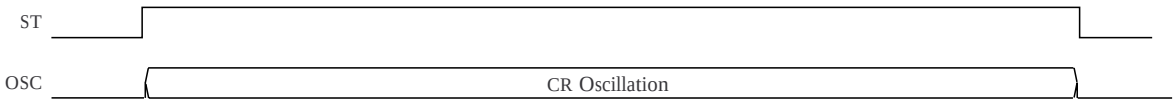


Figure 3. Built-in RC oscillator version

Serial inputs

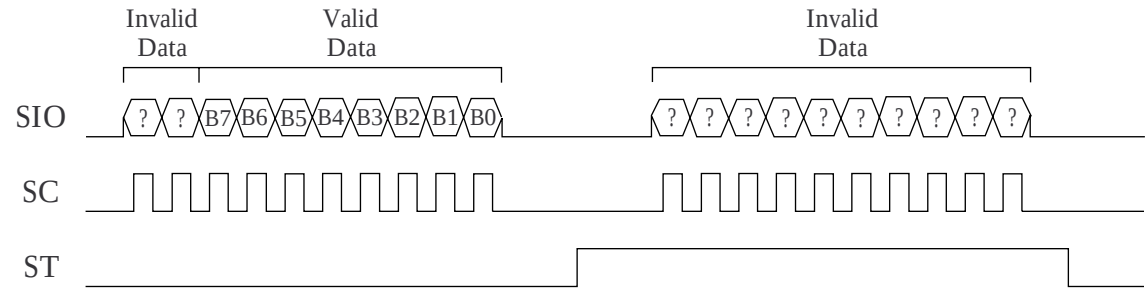
Serial data is input on SIO in sync with the SC clock in 8-bit units when ST is LOW. Data is not accepted when ST is HIGH. When ST goes HIGH, the 8-bit data is latched. Note that if the input data exceeds 8 bits in length, the most recent 8 bits are used and any preceding bits are ignored. Data is in MSB first format.

Input data is interpreted as a command or as a data word (in write mode), depending on the current operating mode of the device. There are 3 types of commands:

- Playback start command
- SRAM write command
- End-of-write command

The SRAM write command is used to invoke write mode operation, and end-of-write command is used to return to play mode operation. In write mode, however, data is interpreted as data words to be written to SRAM.

Note that pin SIO is an output pin only when the parity check command is executed. At all other times, SIO is an input pin.

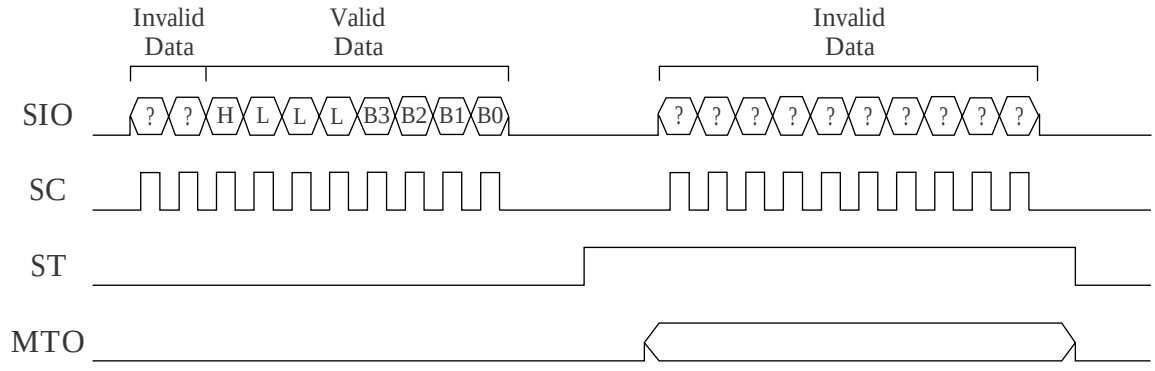


Pin SC should be LOW when either a LOW-to-HIGH or HIGH-to-LOW transition occurs on pin ST.

Figure 4. Serial input timing

Playback control

The ST pin controls the start of playback. While ST is HIGH, the melody is played repeatedly, and when ST goes LOW, playback stops. Melodies are selected by input serial data on pins SIO and SC, as shown in table 2. The melody select command comprises a fixed code (1000) followed by 4 melody select data bits (B3 to B0). The 8 bits of data are retained even after playback. If serial data is input during playback, the data is ignored and playback continues.



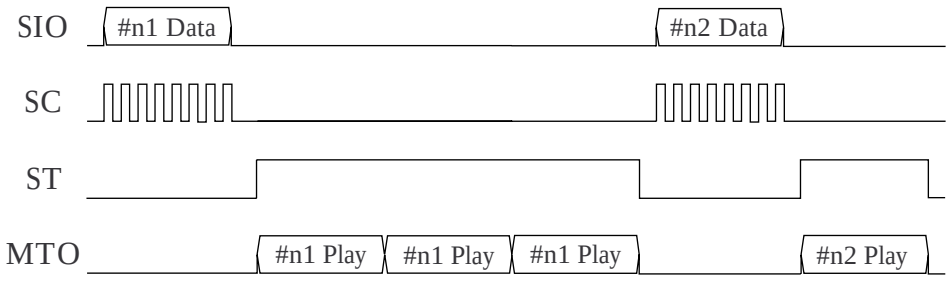
Pin SC should be LOW when either a LOW-to-HIGH or HIGH-to-LOW transition occurs on pin ST.

Figure 5. Serial data input timing

Table 2. Serial data melody select

B3	B2	B1	B0	ST	Melody
L	L	L	L	L → H	1st melody
L	L	L	H	L → H	2nd melody
L	L	H	L	L → H	3rd melody
L	L	H	H	L → H	4th melody
L	H	L	L	L → H	5th melody
L	H	L	H	L → H	6th melody
L	H	H	L	L → H	7th melody
L	H	H	H	L → H	8th melody

B3	B2	B1	B0	ST	Melody
H	L	L	L	L → H	9th melody
H	L	L	H	L → H	10th melody
H	L	H	L	L → H	11th melody
H	L	H	H	L → H	12th melody
H	H	L	L	L → H	13th melody
H	H	L	H	L → H	14th melody
H	H	H	L	L → H	15th melody
H	H	H	H	L → H	SRAM melody



Melody plays repeatedly when ST is HIGH, and stops immediately when ST goes LOW.

Figure 6. Melody repetition timing

Playback timing diagrams

Playback start

Playback starts after an interval t_{ST} after ST goes HIGH.
When the reference clock frequency is 32.768 kHz, t_{ST} = (256 ± 1 oscillator cycles) + 1/128 seconds.
When the reference clock frequency is 38.4 kHz, t_{ST} = (300 ± 1 oscillator cycles) + 1/128 seconds.

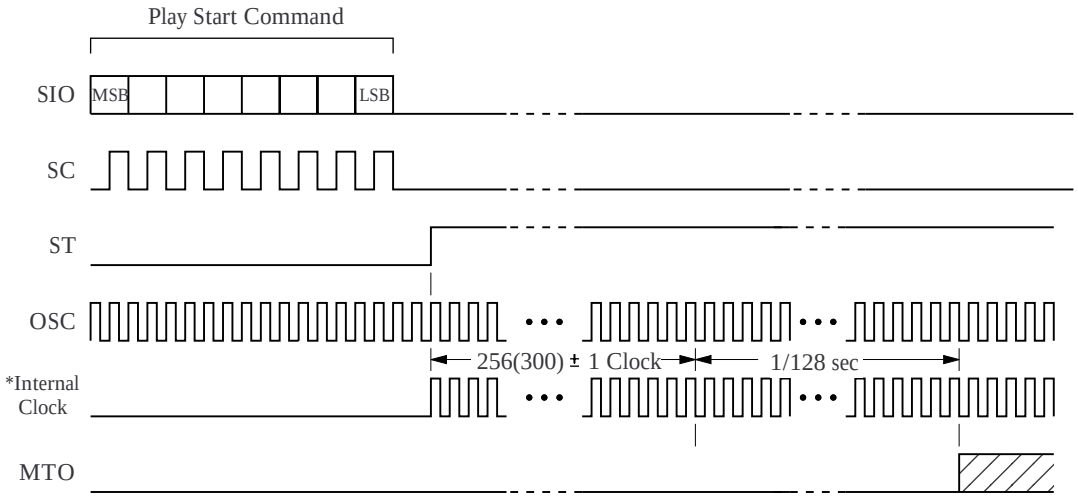


Figure 7. Playback start timing

Playback stop

Playback stops immediately when ST goes LOW. In external clock input versions, the IC internal clock also stops when ST goes LOW, regardless of whether or not there is a clock input signal on pin OSC. In built-in RC oscillator versions, the oscillator also stops when ST goes LOW.

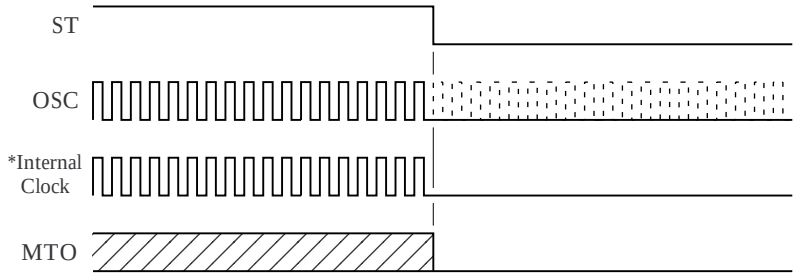


Figure 8. Stop timing

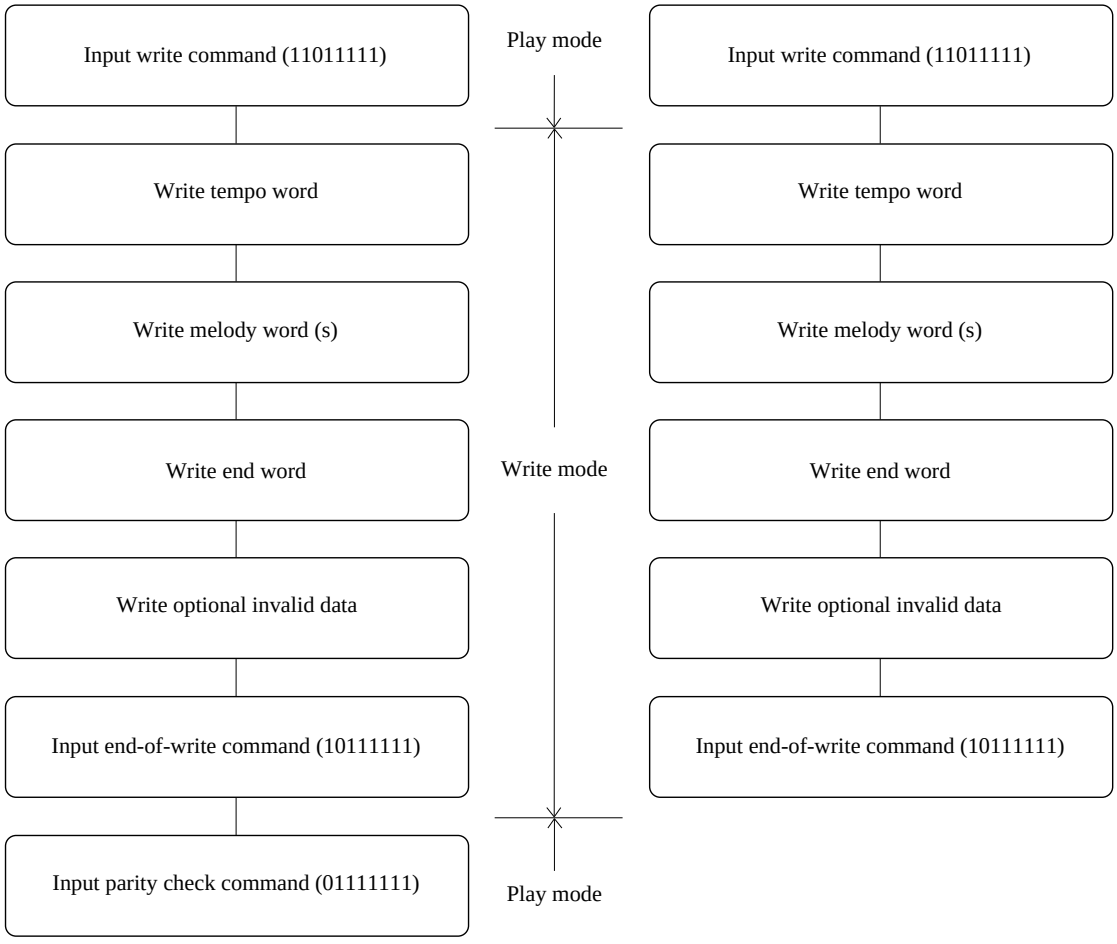
Write Mode Control

Write sequence

The SM1126 Series devices can accept data words written to the built-in SRAM to play any melody. The SRAM write sequence is described below.

1. Write the SRAM write command (11011111) to invoke write mode.
2. Write the tempo word (parity check ON/OFF selectable).
3. Write all necessary melody data words (parity check ON/OFF selectable).
4. Write the melody end word (parity check ON/OFF selectable).
5. Optionally, write extra data words (these are ignored).
6. Write the end-of-write command (10111111) to return to play mode.
7. If parity check was ON, write the parity check command (01111111) to perform an error check.

The built-in SRAM can store 64 words, so all melody and end words must fit within this limit. Note that the tempo word is not stored in SRAM, but in a separate register. Playback of melodies stored in SRAM begins from the SRAM leading address and continues until the end word is detected, at which point playback continues again from the SRAM leading address. All data in SRAM after the end word is ignored.



Example 1. Parity check selected

Example 2. Parity check not selected

Figure 9. Write control sequence

Write command

The SRAM write command (11011111), shown below, is used to invoke write mode.

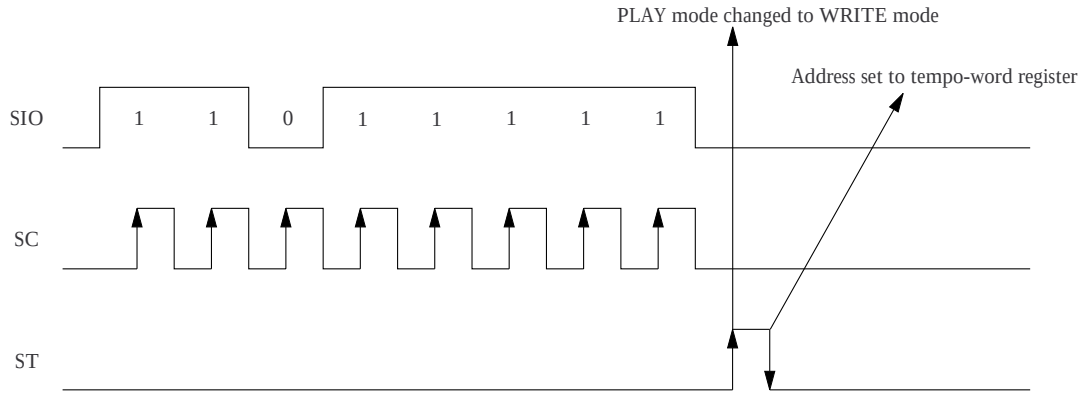


Figure 10. Write command timing

Tempo word

The tempo word controls the melody playback speed. The tempo word comprises a fixed code (000) followed by the tempo code (T4 to T0), as shown below. The tempo word is always the first word written after invoking write mode, and all subsequent words are melody data words.

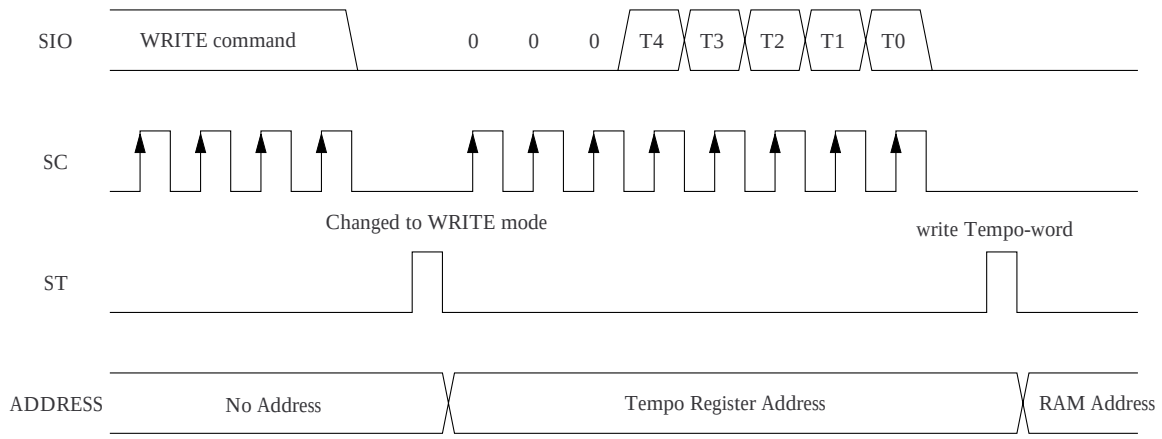


Figure 11. Tempo word timing

Melody words

Melody words contain all the information needed for playback of a single note, including the note duration and type (name or rest). Each melody word comprises a 3-bit length code (R2 to R0) followed by a 5-bit type code (S4 to S0).

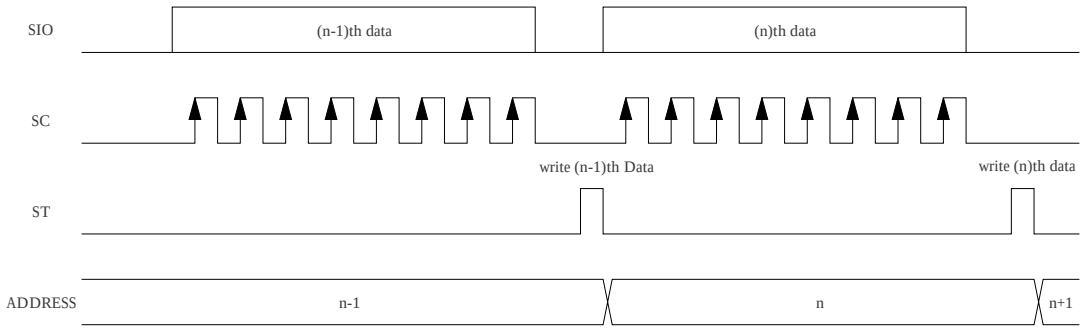


Figure 12. Melody word timing

End word

The end word (01011111) indicates the end of the melody. When the end word is detected during melody playback, operation returns to the SRAM leading address. All data in SRAM after the end word is ignored.

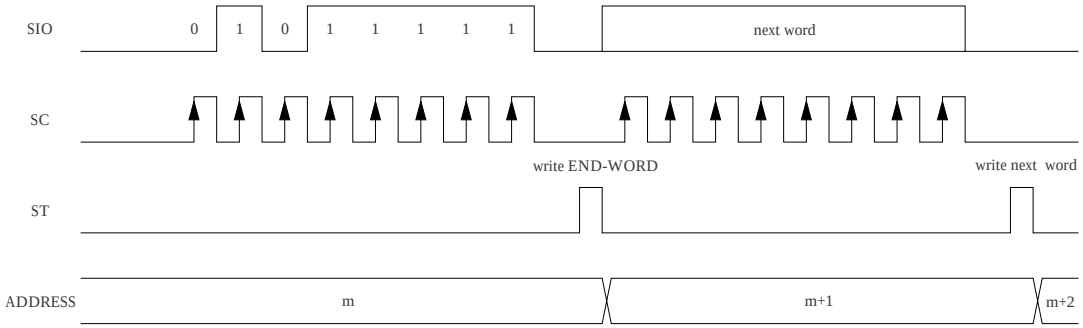


Figure 13. End word timing

End-of-write command

The end-of-write command (10111111) is used to return to play mode from write mode. This command should be executed when power is first applied to set play mode.

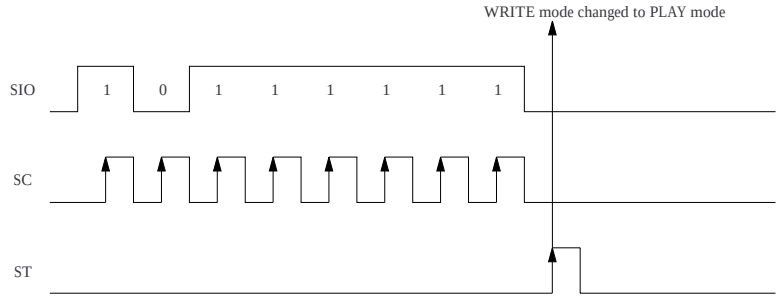


Figure 14. End-of-write command timing

Parity check command

Data words (tempo word, melody words, end word) can have an optional parity bit added, forming 9-bit data words, for a parity check function. The parity check command is executed in play mode, immediately after the end-of-write command is executed.

The parity bit is added at the beginning of the data word. Note that the last 8 bits are always the valid data bits. The parity check function performs an odd parity check (an odd number of 1s within the 9-bit data). If the parity check command is not executed, play mode operation continues using the valid 8 bits of data in each data word.

The parity check sequence is described below.

1. The internal G flag (Good flag) is set to 1 when the write command is executed.
2. When writing data words, the G flag remains set to 1 for odd parity, but is set to 0 if even parity is detected.
3. The G flag remains set to 1 only if all data words have odd parity.
4. Write the end-of-write command to return to play mode.
5. Write the parity check command.
6. When ST is HIGH, the SIO pin functions as the G flag output.
7. When ST goes LOW, the G flag output is released.

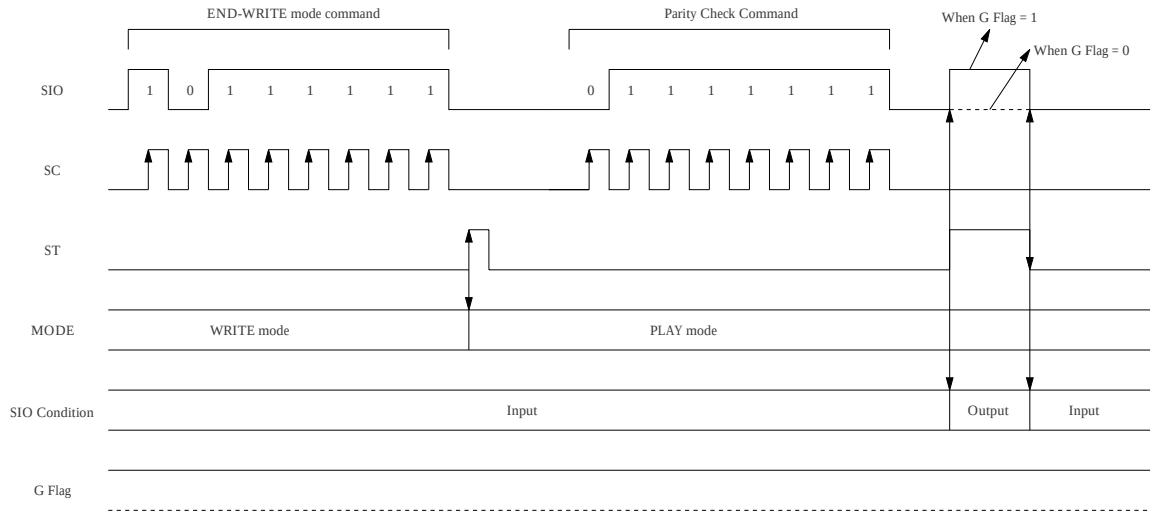


Figure 15. Parity check timing

Command summary

Command	MSB	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	LSB
Melody start command	1	0	0	0	B3	B2	B1	B0
Write command	1	1	0	1	1	1	1	1
Tempo word	0	0	0	T4	T3	T2	T1	T0
Melody word	R2	R1	R0	S4	S3	S2	S1	S0
End word	0	1	0	1	1	1	1	1
End-of-write command	1	0	1	1	1	1	1	1
Parity check command	0	1	1	1	1	1	1	1

Musical Specifications

Maximum program steps

A maximum of 256 steps can be programmed into mask-programmable ROM, and a maximum of 64 steps (including one end word) can be stored in built-in SRAM. Each step represents either a note (sound pitch and length) a rest, or a tie.

Note length (including rests)

Eight rhythm values for notes and rests can be programmed. Also, 2 or more notes can be musically tied.

Table 3. Rhythm values

Type	Code							
	0	1	2	3	4	5	6	7
Note								
Rest								

Pitch and scale

SM1126 Series devices support 27 pitches from F4 to G6. The pitch varies with the clock frequency, as shown in the frequency listing in table 4. The reference clock selected at master-slice does not affect the pitch range.

Also, two pitches higher than G6 can be set as alarm pitches in mask ROM. Note that an alarm pitch option cannot be specified in SRAM.

The frequency error calculation for a given pitch is shown below.

Error calculation: (A4 pitch with 32.768 kHz clock)

$$1200 \times \log_2 \frac{\text{Output frequency}}{\text{Reference frequency}} = 1200 \times \frac{\log_{10} \frac{\text{Output frequency}}{\text{Reference frequency}}}{\log_{10} 2}$$

$$\approx 3986.3 \times \log_{10} \frac{\text{Output frequency}}{\text{Reference frequency}}$$

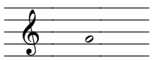
$$\approx 3986.3 \times \log_{10} \frac{439.839}{440.000}$$

$$\approx -0.63 \text{ cent}$$

Table 4. Frequency range

Note code					System clock		32.768 kHz system			38.4 kHz system		
S4	S3	S2	S1	S0	Pitch	Reference frequency	Frequency divider	Frequency (Hz)	Relative error (cent)	Frequency divider	Frequency (Hz)	Relative error (cent)
0	0	0	0	0	Rest	–	–	–	–	–	–	–
0	0	0	0	1	F4	349.228	188	348.596	–3.14	220	349.091	–0.68
0	0	0	1	0	F#4	369.994	177	370.260	1.24	208	369.231	–3.58
0	0	0	1	1	G4	391.995	167	392.431	1.92	196	391.837	–0.70
0	0	1	0	0	G#4	415.305	158	414.785	–2.17	185	415.135	–0.71
0	0	1	0	1	A4	440.000	149	439.839	–0.63	175	438.857	–4.50
0	0	1	1	0	A#4	466.164	141	464.794	–5.09	165	465.455	–2.64
0	0	1	1	1	B4	493.883	133	492.752	–3.97	156	492.308	–5.53
0	1	0	0	0	C5	523.251	125	524.288	3.43	147	522.449	–2.66
0	1	0	0	1	C#5	554.365	118	555.390	3.20	139	552.518	–5.78
0	1	0	1	0	D5	587.330	112	585.143	–6.46	131	586.260	–3.16
0	1	0	1	1	D#5	622.254	105	624.152	5.27	123	624.390	5.93
0	1	1	0	0	E5	659.255	99	661.980	7.14	116	662.069	7.37
0	1	1	0	1	F5	698.456	94	697.191	–3.14	110	698.182	–0.68
0	1	1	1	0	F#5	739.989	89	736.360	–8.51	104	738.462	–3.58
0	1	1	1	1	G5	783.991	84	780.190	–8.41	98	783.673	–0.70
1	0	0	0	0	G#5	830.609	79	829.570	–2.17	92	834.783	8.68
1	0	0	0	1	A5	880.000	74	885.622	11.02	87	882.759	5.42
1	0	0	1	0	A#5	932.328	70	936.229	7.23	82	936.585	7.89
1	0	0	1	1	B5	987.767	66	992.970	9.10	78	984.615	–5.53
1	0	1	0	0	C6	1046.502	63	1040.254	–10.37	73	1052.055	9.16
1	0	1	0	1	C#6	1108.731	59	1110.780	3.20	69	1113.043	6.72
1	0	1	1	0	D6	1174.659	56	1170.286	–6.46	65	1181.538	10.11
1	0	1	1	1	D#6	1244.508	53	1236.528	–11.14	62	1238.710	–8.08
1	1	0	0	0	E6	1318.510	50	1310.720	–10.26	58	1324.138	7.37
1	1	0	0	1	F6	1396.913	47	1394.383	–3.14	55	1396.364	–0.68
1	1	0	1	0	F#6	1479.978	44	1489.455	11.05	52	1476.923	–3.58
1	1	0	1	1	G6	1567.982	42	1560.381	–8.41	49	1567.347	–0.70
1	1	1	0	0	AL1	–	–	–	–	–	–	–
1	1	1	0	1	AL2	–	–	–	–	–	–	–
1	1	1	1	0	Tie	–	–	–	–	–	–	–
1	1	1	1	1	End word	–	–	–	–	–	–	–

(Note) A4 is the following note.



A4 (440Hz)

Pitches AL1 and AL2 are optional alarm pitches which can take any value higher than G6, set in mask ROM. This option is not supported in SRAM.

Tempo

There are 29 tempos that can be selected for each melody. The tempo does not vary with the clock frequency.

Table 5. Tempo range

Code	Frequency divider	Tempo	♩=
03	4	Prestissimo	320.0
04	5		256.0
05	6		213.3
06	7	Presto	182.9
07	8	Allegro	160.0
08	9		142.2
09	10		128.0
0A	11	Moderato	116.4
0B	12		106.7
0C	13	Andante	98.5
0D	14		91.4
0E	15		85.3
0F	16		80.0
10	17	Adagio	75.3
11	18		71.1
12	19		67.4
13	20	Larghetto	64.0
14	21		61.0
15	22	Largo	58.2
16	23		55.7
17	24		53.3
18	25		51.2
19	26		49.2
1A	27		47.4
1B	28		45.7
1C	29		44.1
1D	30		42.7
1E	31		41.3
1F	32		40.0

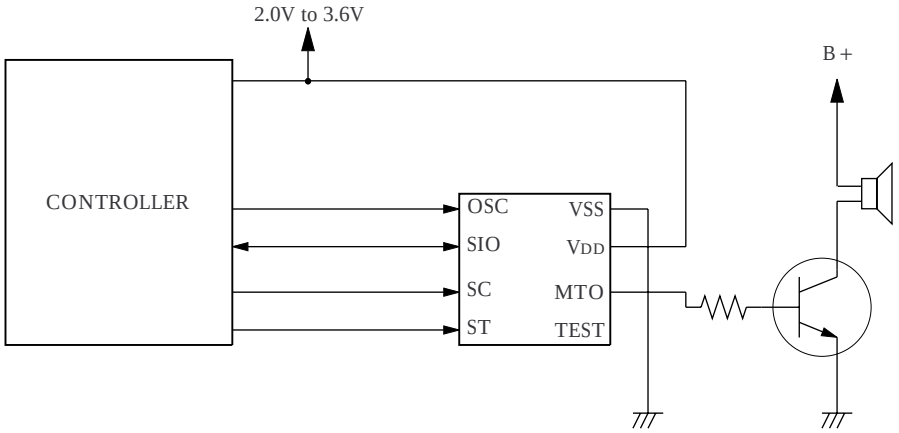
Quarter note (♩) length = {1536 (32.768 kHz system) or 1800 (38.4 kHz system)} × tempo counter frequency divider ÷ clock frequency

(Ex. 1) Tempo code = 1F (divider = 32), clock frequency = 32.768 kHz (32.768 kHz system)
$1536 \times 32 \div 32768 = 1.5$ (seconds)

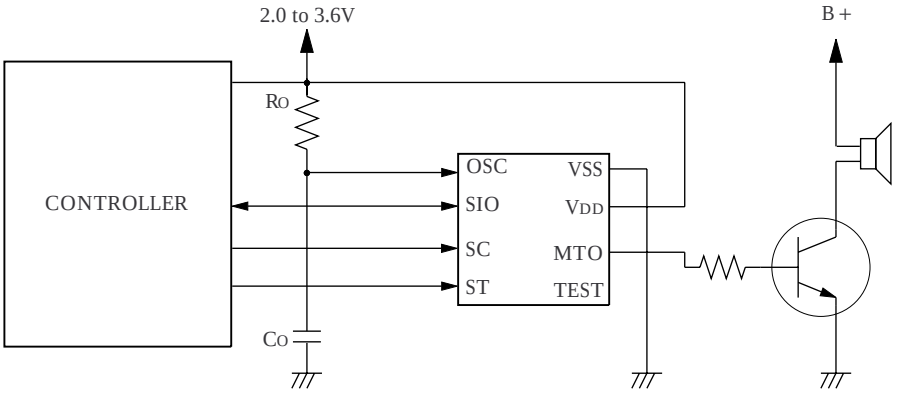
(Ex. 2) Tempo code = 18 (divider = 25), CLK frequency = 153.6 kHz (38.4 kHz system)
$1800 \times 25 \div 38400 = 1.17$ (seconds)

TYPICAL APPLICATION

External Clock Input Versions



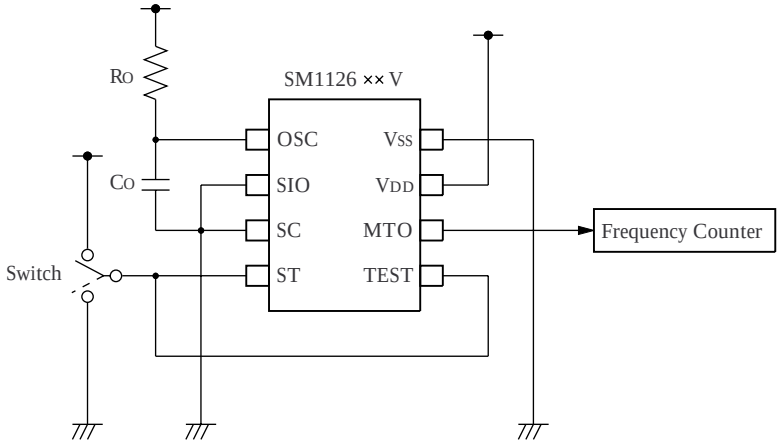
Built-in RC Oscillator Versions



OSCILLATOR FREQUENCY MEASUREMENT

The measurement circuit below shows a SM1126××V with built-in RC oscillator circuit and external RC oscillator components capacitor C_O and resistor R_O.

When ST is switched to V_{DD}, the oscillator starts and outputs a pulse on MTO with a frequency double that of the RC oscillator. The output pulse is counted using a frequency counter.



Note that the board mounting and wiring will marginally affect the output frequency, even for equivalent values for R_O and C_O.

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