October 1998
Edition 1.1

MB87L2250 *- MPEG2 Transport, Video and Audio Decoder with integrated 32-Bit RISC CPU*

OVERVIEW

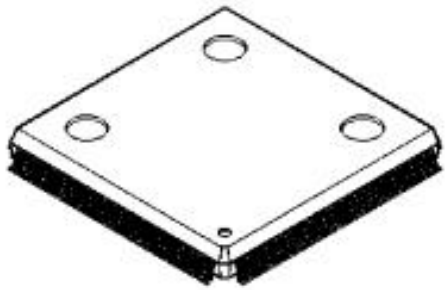
Fujitsu's MB87L2250 is a single chip MPEG video and audio decoder which also includes the transport demultiplexer and 32-Bit RISC CPU. This offers a very cost effective high integrated solution for set top box applications.

MPEG decoding and transport demultiplexing are implemented in hardware. The on-chip CPU, operating at 54 MHz, is fully available for customer application software, for example the EPG function.

The MB87L2250 uses a 2.5 frame architecture which requires only one 16 Mbit SDRAM memory for MPEG decoding, OSD and section data buffering.

In addition the chip provides advanced features like letterbox format conversion or teletext insertion into the VBI.

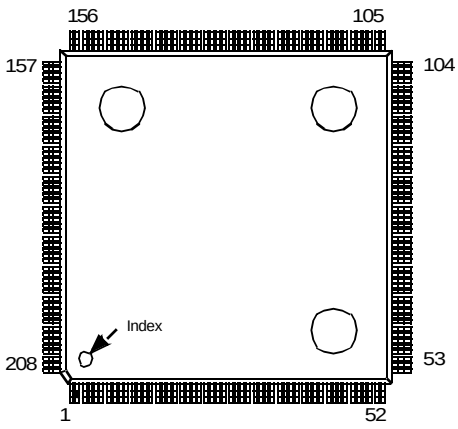
Plastic Flat Package
FPT-208P-M01



FEATURES

- RISC CPU integrated (32-bit)
- 1 KByte I-Cache
- 2.5 Frame Architecture
- Only 16 Mbit SDRAM required
- 32 PID's supported
- Hardware Filter for PID and Sections
- IR Receiver
- DVB Descrambler
- Memory Save Mode to reduce Picture Memory
- Teletext Insertion in VBI
- Letterbox Format Conversion
- 3:2 Pull Down
- FR30 / 68k / SPARClite Processor Interface
- I^2C Interface
- Two Smart Card Interfaces
- 2, 4, 6 or 8 Bit OSD
- 16 Programmable General Purpose I/O's
- Automatic Clock Recovery

Pin Assignment



1. Chip Architecture

Figure 1 shows the chip architecture of Demultiplexer and Audio/Video Decoder MB87L2250, which is dedicated for DVB compliant applications (DVB-S, DVB-C, DVB-T).

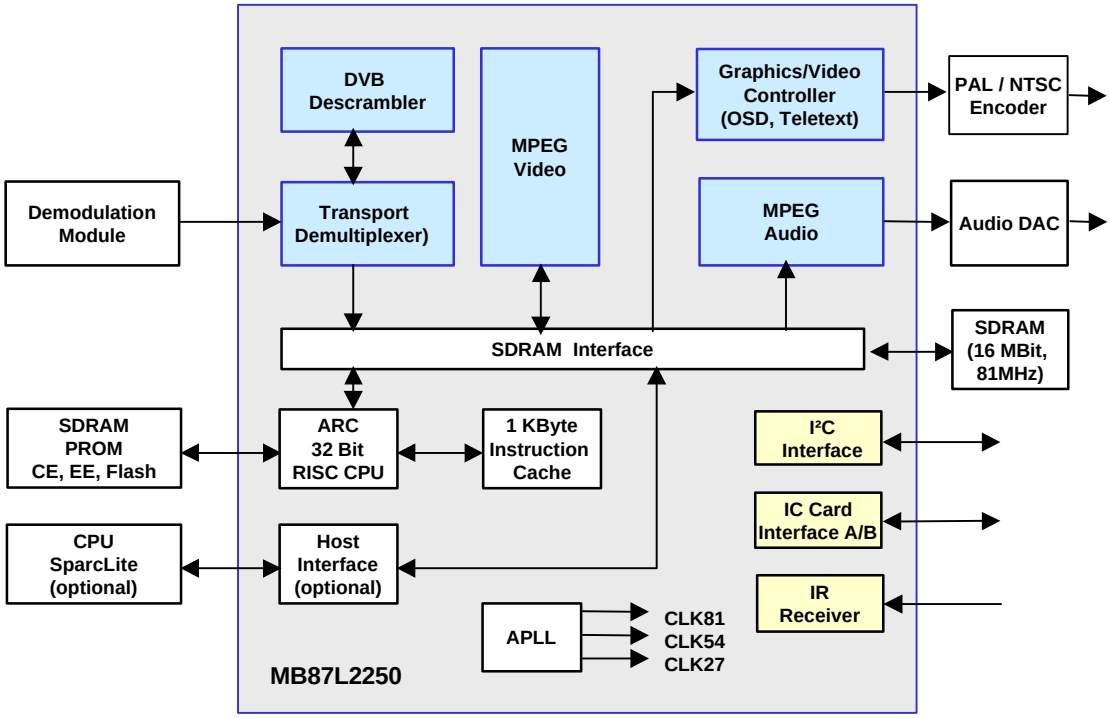


Figure 1: Block Diagram

2. General Features

2.1. ARC 32-Bit RISC CPU

- Pipelined 32-bit RISC Microprocessor
- 32 x 32 bit general purpose registers as standard
- 4 stage pipeline; 1 Kbyte I-Cache
- 8 Mbyte SRAM address space for instruction and data
- 8 Mbyte SDRAM address space for instruction and data
- Basic core contains ALU for arithmetic and logic operations
- 2 and 3-operated instructions
- 9-bit sign-extended or 32-bit immediate data
- Delayed branches
- Conditional execution of regular instructions
- Optional flag setting
- Zero overhead loop feature
- Score boarded delayed loads from memory
- Loads and Stores support 32/16/8 bit data at any 32-bit address
- Address write back for table traversal in memory
- Access local RAM and control registers via special load & store instructions
- Auxiliary register space provides a 32-bit address space separate from the memory system
  - Mapping MPEG registers and MPEG memory into auxiliary address space
  - Mapping ARC registers into auxiliary address space
- Commercial development tools
  - MetaWare **High C**™ 'C' compiler, assembler, linker
  - MetaWare **SeeCode**™ graphical debugger operates in 2 modes:
    - interfaces to hardware evaluation board, or: simulates software using a 'C' model of the ARC

2.2. Host Interface (optional)

- Three different CPU's supported (FR30, 68xxx, SPARClite)

2.3. Transport Demultiplex

- Parallel or serial input format for transport stream
- 60 Mbit/s max. input data rate
- MPEG-2 transport stream ISO/IEC 13818-1 compliant
- DVB descrambler for TS and PES descrambling
- Support for 32 PID's:
  - 1 PID for video / 1 PID for audio / 1 PID for Teletext (EBU Teletext SPB-492)
  - 29 PID's for section data (PAT, PMT, PSI and private SI as Electronic Program Guide etc.)
- Flexible section processing like:
  - individual compare resource allocation to each stream
  - target number and compare length programmable on a stream base
  - maximum compare size of 32 targets
  - maximum compare length of 16 bytes (including TID)
  - special mode for version number filtering (not equal filtering)
  - each bit of all the targets individually maskable
  - overall compare capacity of 422 byte
  - IRQ generation at the end of a received section
  - IRQ generation at the end of a received packet
  - IRQ generation in case of incomplete section (verification with section length)
  - IRQ generation in case of continuity counter error
  - IRQ status register with stream number, IRQ source
  - stream disabling in case of section error
  - IRQ generation in case of incomplete section comparing (packet end)
  - all IRQ s maskable on a stream base

2.4. BUFFER MANAGEMENT

- Individual buffer allocation for each stream
  - Video Buffer / Audio Buffer / Teletext Buffer / 29 Section Data Buffer
- Section buffer types
  - circular buffer
  - buffer size individually programmable for each stream between 256 byte and 32 Kbytes
  - each buffer with write and stop pointers for buffer management
  - stop pointer software controlled
  - IRQ generation and stream disable in case of buffer overflow (programmable)

2.5. Video Decoder

- Decoding of MPEG-2 Video ML@MP ISO/IEC 13818-2, MP@LL, SP@ML
- Error concealment using syntax checker and concealment vectors
- MPEG-1 Bit stream inside ISO-11172-2 decoded DVB compliant
- Supports 3:2 pull down
- 2.5 Frame architecture

2.6. Video Output

- Supports different Video-DAC's (CCIR/ITU 601, CCIR/ITU 656)
- 8 bit Y, Cr, Cb
- 4:2:0 or 4:2:2 output format
- Vertical filtering
  - 4:2:0 -> 4:2:2 conversion (chrominance up sampling),
  - letterbox for 4:3 monitors
  - SIF-upsampling (chrominance and luminance up sampling)
- Horizontal filtering with 8 tap poly phase filter
  - pan/scan
  - DVB full screen up sampling
- digital insertion for Teletext into the VBI
- picture down scaling (75% picture size)

2.7. OSD

- no limitation of the number of OSD-regions (depends only on the available memory)
- individual mode and colour palette for each defined OSD region
- load of colour map for each region programmable
- 4 bits mix weight
- 256 colours (8 Bit), 64 colours (6 Bit), 16 colours (4 Bit), 4 colours (2 Bit) mode supported
- full resolution or SIF format
- in one region transparent, mixed and OSD-only possible
- memory save mode to increase OSD memory
- independent or same bit map for even / odd-field.

2.8. Audio Decoder

- ISO/IEC 11172-3 (MPEG 1 Audio)
- ISO/IEC 13818-3 (MPEG 2 Audio in two channel mode)
- Layer I & Layer II Decoding
- Single / Dual / Joint Stereo / Stereo
- Sampling Rates: 32 KHz / 44,1 KHz / 48 KHz / 16 KHz / 22.05 KHz / 24 KHz
- All bit rates supported
- CRC error detection
- Error concealment

2.9. Audio Output

- Over sampling clock: 384 fs/256 fs
- Bit clock: 32 fs / 48 fs / 64 fs
- Support of different audio-DAC's via serial I/F
- Fractional counter for audio clock generation
- Programmable bit order (MSB or LSB First)
- skip / repeat sample programmable

2.10. External RAM

- 16 Mbit SDRAM, 16 Bit data bus
- Pipelined Type, >83 MHz @ 81 MHz system clock
- Organisation: 2 banks, 2048 rows x 256 words

2.11. Synchronisation

- dedicated system synchronisation hardware for
  - clock recovery (PCR handling)
  - video / audio synchronisation (PTS / DTS handling)
  - PWM generator for external VCXO control
- automatic hardware control (software control optional) for
  - video output
  - video decoder
  - audio decoder
  - PWM signal for 27 MHz VCXO

2.12. IC Card Interface

- two IC card interfaces with timer function

2.13. IIC Interface

- The I^2C master interface supports I^2C master mode with four operating modes:
  - random access write, writing of one data byte to a specified address
  - random access read, reading of one data byte from a specified address
  - direct write, writing of a data burst
  - direct read, reading of a data burst

2.14. General Purpose I/O

- 16 general purpose I/O's
- write data
  - open drain output (programmable)
- read data
- IRQ sensitive (programmable)
  - level / edge sensitive

2.15. Infra Red Receiver

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Device Handling
This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

REVISION CONTROL

Rev. No.	Date	Description of the Changes
1.0	August 1998	First Edition
1.1	October 1998	Features