

## UNIVERSAL PROGRAMMABLE DUAL PLL

The DMD5802/3 is a low power CMOS integrated circuit with two independent programmable PLL. It is specially designed for cordless telephone application in various countries and radio application with a frequency up to 80MHz.

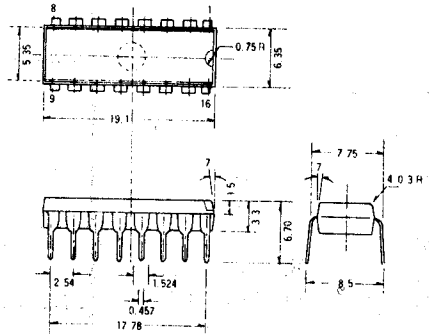
### □ FEATURES

- Two 16 bit programmable counter for transmit and receive loop
  - Dividing number ..... 16 to 65535
- Two independent programmable reference counter
  - 12 bit programmable counter ..... 16 to 4095
  - 14 bit Aux. programmable counter ..... 16 to 16383
- Two independent phase frequency Detector
- On chip oscillator whth external crystal up to 16MHz
- 3 or 4 pin selectable MCU serial interface
- Built-in stand-by mode
- Power supply voltage : 2.5V to 5.5V
- Maximum operating frequency : 80MHz @ 300mVp-p
- Two independent phase frequency detector

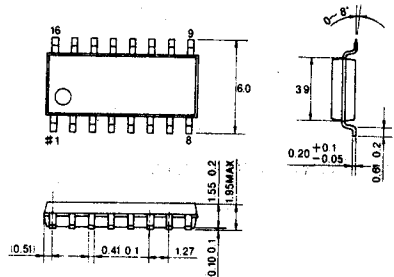
### □ MAXIMUM RATINGS(T<sub>a</sub>=25°C)

Characteristics	Symbol	Rating	Unit
DC supply voltage	VDD	-0.5~6.0	V
Input voltage	V <sub>in</sub>	-0.5~VDD+0.5	V
DC current per pin	I <sub>in</sub> , I <sub>out</sub>	-10 ~ 10	mA
DC current for pin VDD or VSS	IDD, ISS	-30 ~ 30	mA
Operating temperature	T <sub>opr</sub>	-40 ~ +80	°C
Storage temperature	T <sub>stg</sub>	-55 ~ 125	°C

### 16DIP



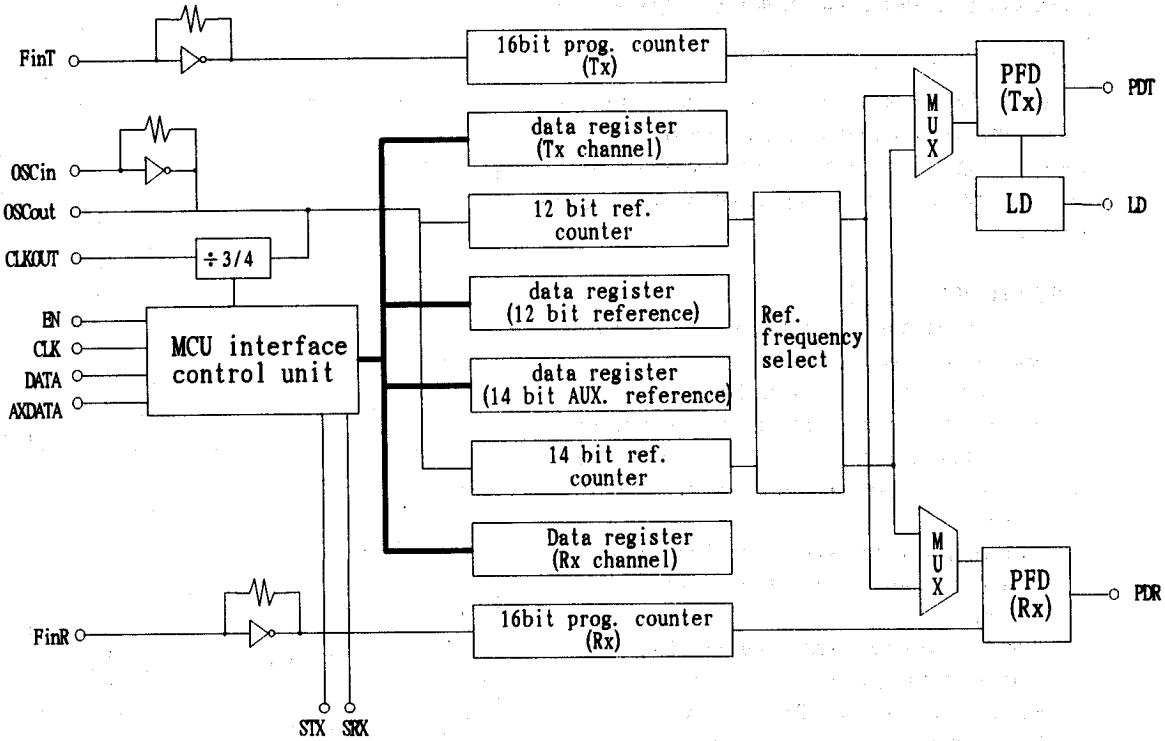
### 16SOP



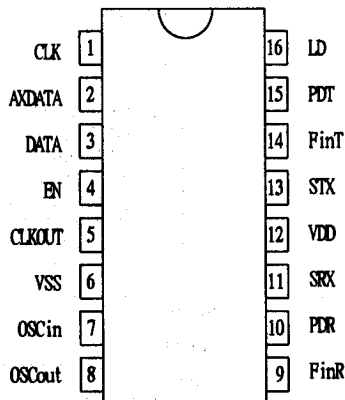
- PIN5 CLOCK OUTPUT  
 DMD5802 : Clock Output  
 DMD5803 : No Connection  
 No connection at Pin5 is performed in order to prevent it from crosstalk phenomenon caused by clock output at certain channel.

# DMD 5802/3

## □ BLOCK DIAGRAM



## □ PIN CONFIGURATION



PIN DESCRIPTION

Name	No	I/O	Description
CLK	1	I	Clock input for programming(see Note 1)
AXDATA	2	I	Auxiliary data input for 4-pins interface
DATA	3	I	Main Data input
EN	4	I	Control input for serial interface(see Note 1) "1" - Programming the Control/Reference register "0" - Programming the Tx/Rx channel data register
CLKOUT	5	O	Frequency output : $F_{osc} \div 3$ or $F_{osc} \div 4$
VSS	6	-	Ground
OSCin	7	I	Crystal oscillator input / External clock input (16MHz max)
OSCOut	8	O	Crystal oscillator output
FinR	9	I	Frequency Input to Rx programmable counter(see Note 1)
PDR	10	O	Rx Phase Frequency detector output(see Note 2)
SRX	11	O	Stand-by mode flag of Rx part
VDD	12	-	Supply Voltage
STX	13	O	Stand-by mode flag of Tx part
FinT	14	I	Frequency Input to Tx programmable counter(see Note 1)
PDT	15	O	Tx Phase frequency Detector output(see Note 2)
LD	16	O	Lock detetor output

Note 1) These pins are normally pull-downed.

Note 2) FinR, FinT are typically derived from the VCO and ac-coupled. For large signal, it needs DC coupling. The minimum input voltage is 300mVp-p @80MHz.

Note 3) These are 3 state output.

Condition	Output
$F_v < F_r$ or $F_v$ lagging	"High"
$F_v > F_r$ or $F_v$ leading	"Low"
$F_v = F_r$ or in phase	High impedance

□ ELECTRICAL CHARACTERISTICS (Ta=25°C, Vss=0 unless otherwise noted)

● DC characteristics

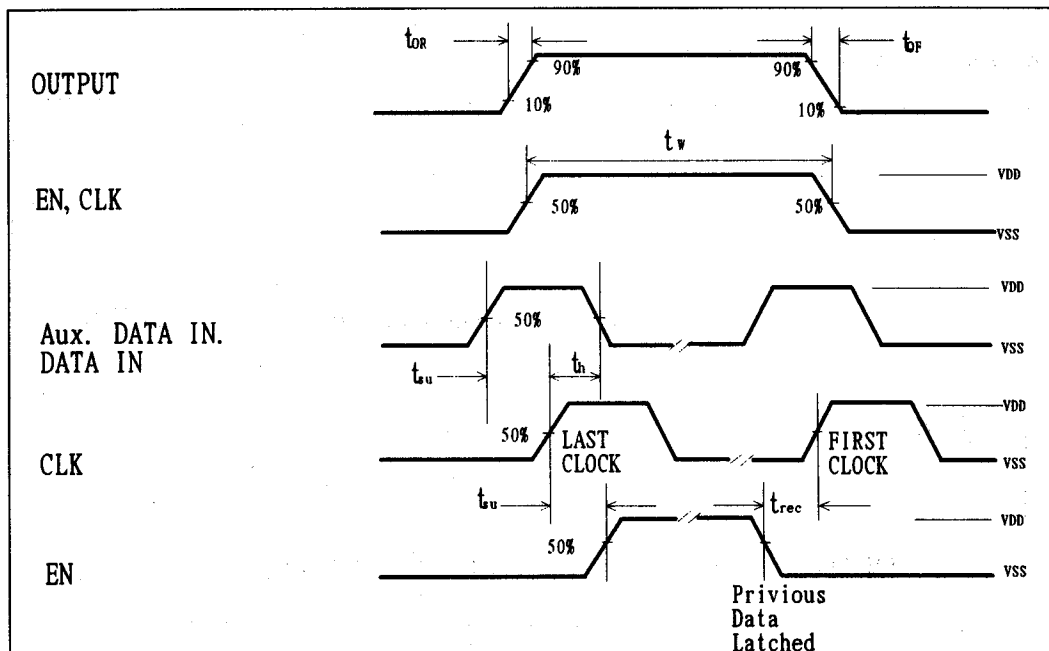
Symbol	Characteristics	Test conditions		VDD (V)	Limits		Unit
					Min.	Max.	
V <sub>DD</sub>	Power supply voltage				2.5	5.5	V
V <sub>IL</sub>	Low level input voltage	V <sub>out</sub> = V <sub>DD</sub> - 0.5V		2.5 2.5	— —	0.75 1.65	V
V <sub>IH</sub>	High level input voltage	V <sub>out</sub> = 0.5V		2.5 5.5	1.75 3.80	— —	V
V <sub>OL</sub>	Low level output voltage	I <sub>out</sub> = 0, V <sub>in</sub> = V <sub>DD</sub>		2.5 5.5	— —	0.05 0.05	V
V <sub>OIH</sub>	High level output voltage	I <sub>out</sub> = 0, V <sub>in</sub> = 0		2.5 5.5	2.45 5.45	— —	V
I <sub>IL</sub>	Low level input current	V <sub>in</sub> = 0	OSCin, FinR, FinT	2.5 5.5	— —	30 66	μA
			ALL digital inputs	2.5 5.5	— —	1.0 1.0	
I <sub>IH</sub>	High level input current	V <sub>in</sub> = V <sub>DD</sub> -0.5	OSCin, FinR, FinT	2.5 5.5	— —	30 66	μA
			ALL digital inputs	2.5 5.5	— —	5.0 5.0	
I <sub>OL</sub>	Low level output current	V <sub>out</sub> = 2.2V V <sub>out</sub> = 5.0V		2.5 5.5	(-)0.18 (-)0.55	— —	mA
I <sub>OIH</sub>	High level output current	V <sub>out</sub> = 2.2V V <sub>out</sub> = 5.0V		2.5 5.5	0.18 0.55	— —	mA
I <sub>DD</sub>	Stand-by current current	All stand-by mode, only oscillator working		2.5 5.5	— —	0.3 1.5	mA
I <sub>del</sub>	Dynamic current	300mVp-p at FinR = FinT = 80MHz, F <sub>osc</sub> = 10.24MHz		2.5 5.5	— —	3.0 10	mA
I <sub>Z</sub>	3 state leakage current	V <sub>in</sub> = 0 or 5.5		5.5	—	0.1	μA
C <sub>in</sub>	Input capacitance			—	—	8.0	pF
C <sub>out</sub>	Output capacitance			—	—	8.0	pF

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● AC characteristics (CL = 50pF)

Symbol	Characteristics		VDD (V)	Limits		Unit
				Min.	Max.	
$f_{MAX}$	Input frequency, Pk to Pk = 300mV	OSCin	2.5–5.5	–	16	MHz
		FinR, Fint	2.5–5.5	–	80	MHz
$t_{OR}, t_{OF}$	Output rise and fall time		2.5	–	200	ns
			5.5	–	100	
$t_R, t_F$	Input rise and fall time		2.5	–	5.0	$\mu$ s
			5.5	–	4.0	
$t_{SU}$	Setup time	Data to Clock	2.5–5.5	100	–	ns
		Enable to Clock	2.5–5.5	200	–	ns
$t_{HOLD}$	Hold time, clock to data		2.5	80	–	ns
			5.5	40	–	
$t_{REC}$	Recovery time, Enable to clock		2.5	80	–	ns
			5.5	40	–	
$t_W$	Input pulse width (CLK, DATA and AXDATA)		2.5	80	–	ns
			5.5	40	–	

Figure 1. Switching diagram



**□ OPERATION OF PFD(Phase Frequency Detector)**

PFD outputs a phase difference signal between falling edges of  $F_r$ (reference frequency) and  $F_v(F_{inT} \div N1$  or  $F_{inR} \div N2)$ . When  $F_v$  leads  $F_r$ , PFD output goes low and sinking current. On the other hand, when  $F_v$  lags  $F_r$ , PFD output goes high and sourcing current. Also if  $F_v$  and  $F_r$  are in phase, output is in high impedance state. See figure 2 and 3.

Figure 2. PFD and lock detector output waveform vs.  $F_v/F_r$  frequencies

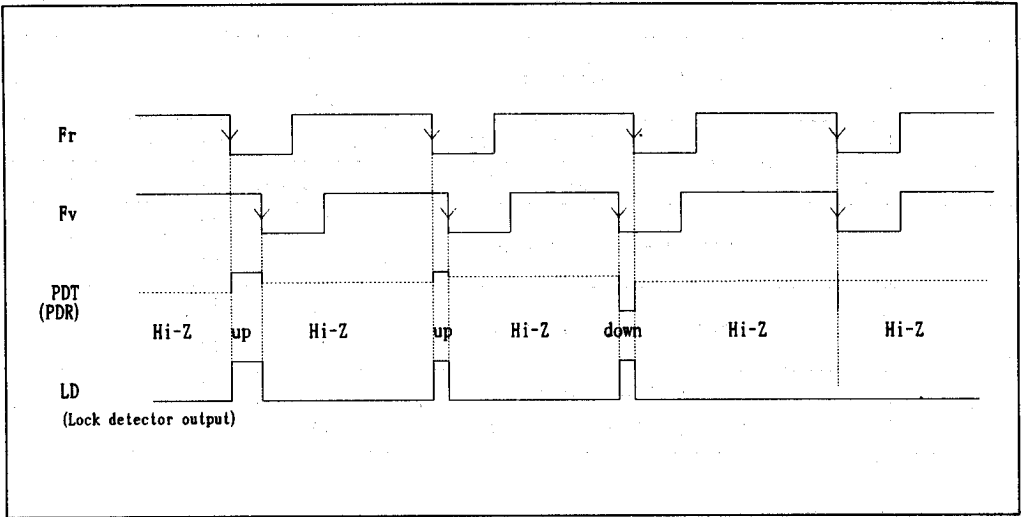
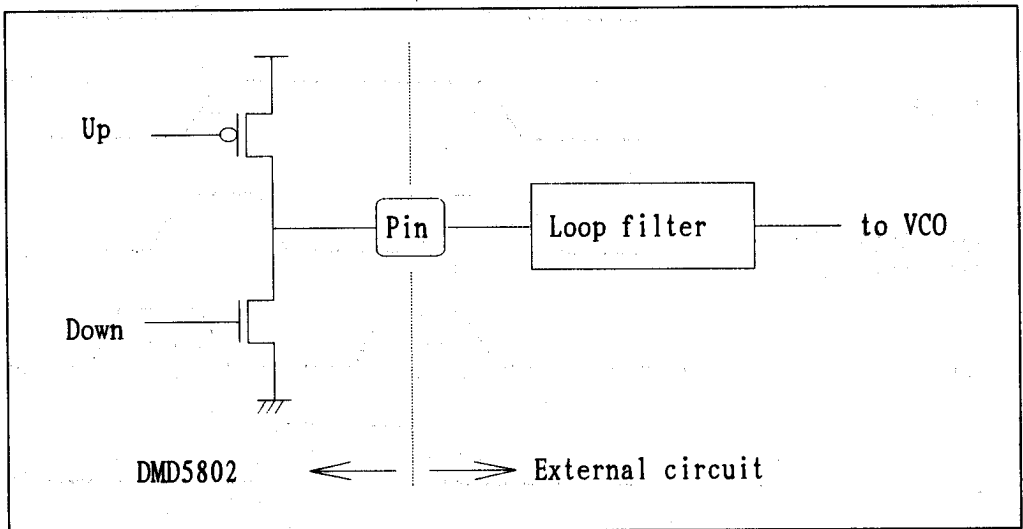
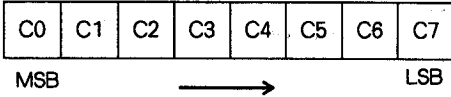


Figure 3. Simplified schematic of PFD output port



## □ CONTROL REGISTER

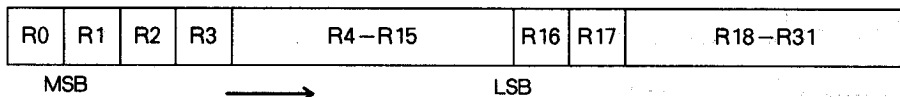


- C0 – control data identifier = “1”
- C1 – Test mode 1. Set to “0” in normal application.
- C2 – Test mode 2. Set to “0” in normal application.
- C3 – Select 3 or 4 – pin interface
  - “0” → 3-pin interface
  - “1” → 4-pin interface
- C4 – Select clock frequency divided by 3 or 4
  - “0” →  $F_{osc} \div 4$
  - “1” →  $F_{osc} \div 3$
- C5 – Control stand-by mode of Tx block
  - “1” → Tx programmable counter, Tx PFD will be in stand-by mode.  
STX will be set “1”.
- C6 – Control stand-by mode of Rx block
  - “1” → Rx programmable counter, Rx PFD will be in stand-by mode.  
SRX will be set “1”.
- C7 – Control stand-by mode of Ref block
  - “1” → 12bit/14bit reference programmable counter will be in stand-by mode.

## □ HOW TO CONTROL STAND-BY MODE

C5	C6	C7	Tx block	Rx block	Ref. block
0	0	0			
0	0	1			Stand-by
0	1	0		Stand-by	
0	1	1		Stand-by	Stand-by
1	0	0	Stand-by		
1	0	1	Stand-by		Stand-by
1	1	0	Stand-by	Stand-by	
1	1	1	Stand-by	Stand-by	Stand-by

## REFERENCE REGISTER



- R0 — Reference data identifier = "0"
- R1 — 14bit AUX. reference counter enable bit. "1" → Enable
- R2, R3 — Select a reference frequency of Tx PFD and Rx PFD, respectively  
 "1" → the reference frequency of Tx(Rx) PFD Fref1  
 "0" → the reference frequency of Tx(Rx) PFD Fref2
- R4~R15 — 12bit reference counter data
- R16, R17 — Reference frequency selection
- R18~R31 — 14bit AUX. reference counter data

## REFERENCE FREQUENCY SELECTION

The DMD5802/3 has a 12bit reference counter and a 14bit aux, reference counter. Also, to select various reference frequency without reprogramming the reference register, the ÷4 and the ÷25 modules are supported. The Reference frequency selection diagram was shown in figure 4. The combination of selection bits was shown in Table 1.

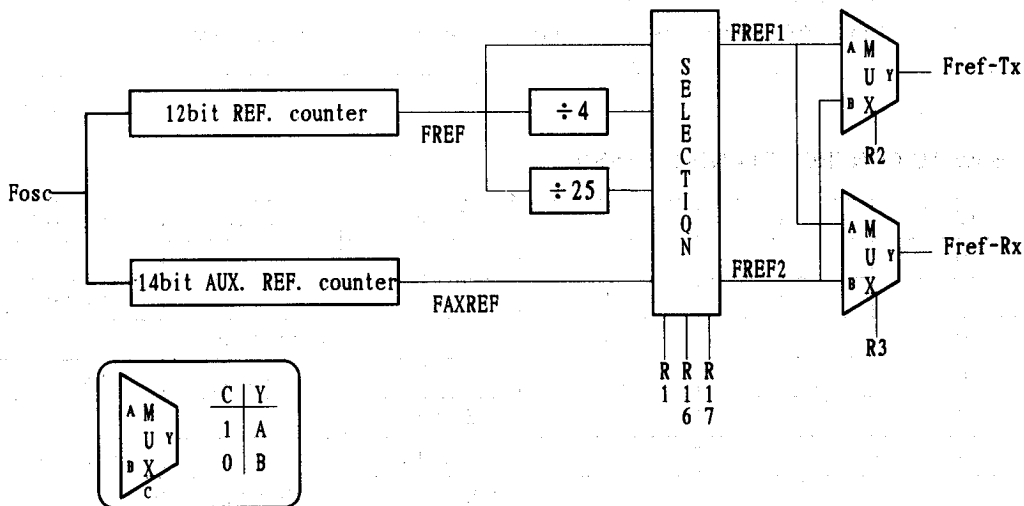
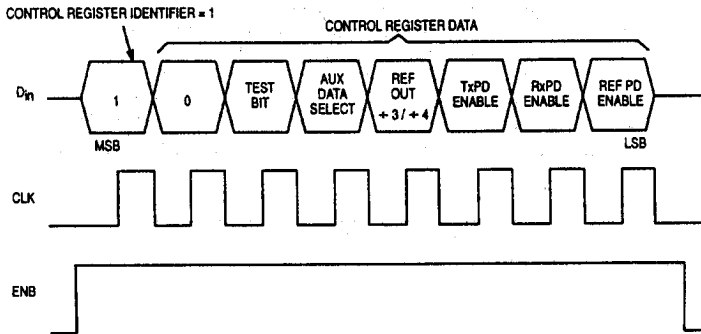


Figure 4. Reference frequency selection diagram

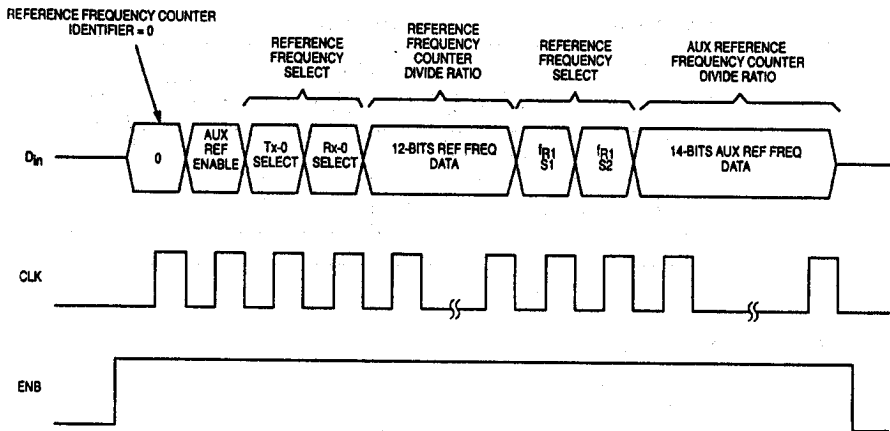


## A. Programming Format of the Control Register



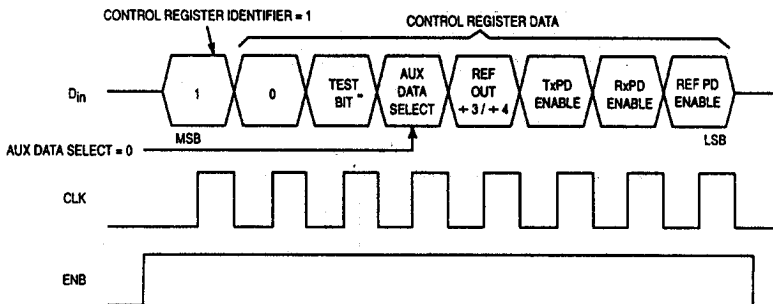
Note: ENB must be high during the serial transfer.

## B. Programming Format of the Auxiliary/Reference Frequency Counters



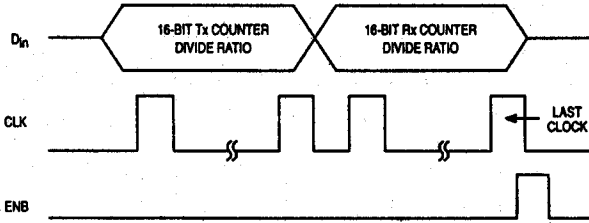
Note: ENB must be high during the serial transfer.

## C. Programming Format for Control Register (3-Pin Interfacing Scheme)



Note: ENB must be high during the serial transfer.

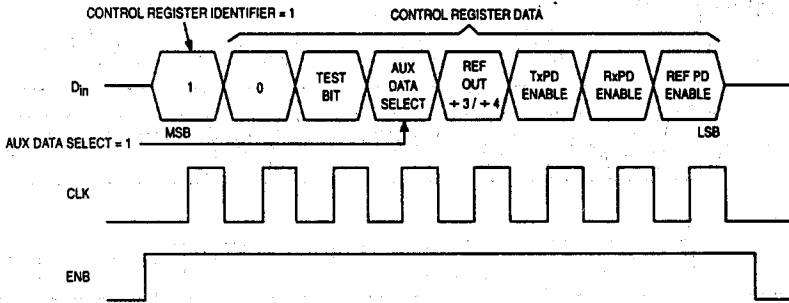
## D. Programming Format for Transmit and Receive Counters (3-Pin Interfacing Scheme)



Note: ENB must be low during the serial transfer.

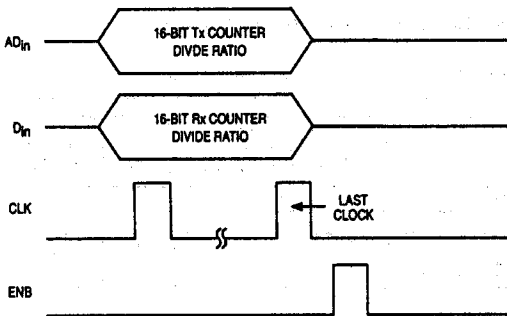
## E. Programming Format for Control Register (4-Pin Interfacing Scheme)

### Programming Format for Control Register (4-Pin Interfacing Scheme)



Note: ENB must be high during the serial transfer.

## F. Programming Format for Transmit and Receive Counters (4-Pin Interfacing Scheme)



Note: ENB must be low during the serial transfer.

Table 1. Combination of Selection bits

R1	R16	R17	FREF1	FREF2
0	0	0	FREF/4	X
	0	1	FREF	X
	1	0	FREF/4	FREF/25
	1	1	FREF	FREF/25
1	0	0	FREF/4	FAXREF
	0	1	FREF	FAXREF
	1	0	FREF/4	FAXREF
	1	1	FREF/25	FAXREF

# DMD 5802/3

## Korea CT-1 Frequency Table

Base set				
Channel Number	Tx Channel Frequencies (MHz)	Tx Divider (5.0 KHz Ref)	1st LO Frequencies (MHz) 1st 1F = 10.695 MHz	Rx Divider (5.0 KHz Ref)
1	46.610	9322	38.975	7795
2	46.630	9326	39.150	7830
3	46.670	9334	39.165	7833
4	46.710	9342	39.075	7815
5	46.730	9346	39.135	7836
6	46.770	9354	39.195	7827
7	46.830	9366	39.235	7839
8	46.870	9374	39.295	7847
9	46.930	9386	39.275	7859
10	46.970	9394	39.275	7855
11	46.510	9302	39.000	7800
12	46.530	9306	39.015	7803
13	46.550	9310	39.030	7806
14	46.570	9314	39.045	7809
15	46.590	9318	39.060	7812

Hand set				
Channel Number	Tx Channel Frequencies (MHz)	Tx Divider (5.0 KHz Ref)	1st LO Frequencies (MHz) 1st 1F = 10.695 MHz	Rx Divider (5.0 KHz Ref)
1	49.670	9934	35.915	7183
2	49.845	9969	35.935	7187
3	49.860	9972	35.975	7195
4	49.770	9954	36.015	7203
5	49.875	9975	36.035	7207
6	49.830	9966	36.075	7215
7	49.890	9978	36.135	7227
8	49.930	9986	36.175	7235
9	49.990	9998	36.235	7247
10	49.970	9994	36.275	7255
11	49.695	9939	35.815	7163
12	49.710	9942	35.835	7167
13	46.275	9945	35.855	7171
14	49.740	9948	35.875	7175
15	49.755	9951	35.895	7179

# DMD 5802/3

## USA CT-1 Frequency Table

Base set				
Channel Number	Tx Channel Frequencies (MHz)	Tx Divider (5.0 KHz Ref)	1st LO Frequencies (MHz) 1st 1F = 10.695 MHz	Rx Divider (5.0 KHz Ref)
1	46.610	9322	38.975	7795
2	46.630	9326	39.150	7830
3	46.670	9334	39.165	7833
4	46.710	9342	39.075	7815
5	46.730	9346	39.180	7836
6	46.770	9354	39.135	7827
7	46.830	9366	39.195	7839
8	46.870	9374	39.235	7847
9	46.930	9386	39.295	7859
10	46.970	9394	39.275	7855
New Channels				
11	43.720	8744	38.065	7613
12	43.740	8748	38.145	7629
13	43.820	8764	38.165	7633
14	43.840	8768	38.225	7645
15	43.920	8784	38.325	7665
16	43.960	8792	38.385	7577
17	44.120	8824	38.405	7681
18	44.160	8832	38.465	7693
19	44.180	8836	38.505	7701
20	44.200	8840	38.545	7709
21	44.320	8864	38.585	7717
22	44.360	8872	38.665	7733
23	44.400	8880	38.705	7741
24	44.460	8892	38.765	7753
25	44.480	8896	38.805	7761

# DMD 5802/3

## USA CT-1 Frequency Table

Hand set				
Channel Number	Tx Channel Frequencies (MHz)	Tx Divider (6.25 KHz Ref)	1st LO Frequencies (MHz) 1st 1F = 10.7 MHz	Rx Divider (6.25 KHz Ref)
1	49.670	9934	35.915	7183
2	49.845	9969	35.935	7187
3	49.860	9972	35.975	7195
4	49.770	9954	36.015	7203
5	49.875	9975	36.035	7207
6	49.830	9966	36.075	7215
7	49.890	9978	36.135	7227
8	49.930	9986	36.175	7235
9	49.990	9998	36.235	7247
10	49.970	9994	36.275	7255
New Channels				
11	48.760	9752	33.025	6605
12	48.840	9768	33.045	6609
13	48.860	9772	33.125	6625
14	48.920	9784	33.145	6629
15	49.020	9804	33.225	6645
16	49.080	9816	33.265	6653
17	49.100	9820	33.425	6685
18	49.160	9832	33.465	6693
19	49.200	9840	33.485	6687
20	49.240	9848	33.505	6701
21	49.280	9856	33.625	6725
22	49.360	9872	33.665	6733
23	49.400	9880	33.705	6741
24	49.460	9892	33.765	6753
25	49.500	9900	33.785	6757

# DMD 5802/3

## China CT-1 Frequency Table

Base Set				
Channel Number	Tx Channel Frequencies (MHz)	Tx Divider (5.0 KHz Ref)	1st LO Frequencies (MHz) 1st 1F = 10.695 MHz	Rx Divider (5.0 KHz Ref)
1	45.250	9050	37.555	7511
2	45.275	9055	37.580	7516
3	45.300	9060	37.605	7521
4	45.325	9065	37.630	7526
5	45.350	9070	37.655	7531
6	45.375	9075	37.680	7536
7	45.400	9080	37.705	7541
8	45.425	9085	37.730	7546
9	45.450	9090	37.775	7551
10	45.475	9095	37.780	7556

Hand Set				
Channel Number	Tx Channel Frequencies (MHz)	Tx Divider (5.0 KHz Ref)	1st LO Frequencies (MHz) 1st 1F = 10.695 MHz	Rx Divider (5.0 KHz Ref)
1	48.250	9650	34.555	6911
2	48.275	9655	34.580	6916
3	48.300	9660	34.605	6921
4	48.325	9665	34.630	6926
5	48.350	9670	34.655	6931
6	48.375	9675	34.680	6936
7	48.400	9680	34.705	6941
8	48.425	9685	34.730	6946
9	48.450	9690	34.775	6951
10	48.475	9695	34.780	6956

# DMD 5802/3

## France CT-1 Frequency Table

Base set				
Channel Number	Tx Channel Frequencies (MHz)	Tx Divider (6.25 KHz Ref)	1st LO Frequencies (MHz) 1st 1F = 10.7 MHz	Rx Divider (6.25 KHz Ref)
1	26.4875	4238	30.7875	4926
2	26.4750	4236	30.7750	4924
3	26.4625	4234	30.7625	4922
4	26.4500	4232	30.7500	4920
5	26.4375	4230	30.7375	4918
6	26.4250	4228	30.7250	4916
7	26.4125	4226	30.7125	4914
8	26.4000	4224	30.7000	4912
9	26.3875	4222	30.6875	4910
10	26.3750	4220	30.6750	4908
11	26.3625	4218	30.6625	4906
12	26.3500	4216	30.6500	4904
13	26.3375	4214	30.6375	4902
14	26.3250	4212	30.6250	4900
15	26.3125	4210	30.6125	4898

Hand set				
Channel Number	Tx Channel Frequencies (MHz)	Tx Divider (5.0 KHz Ref)	1st LO Frequencies (MHz) 1st 1F = 10.695 MHz	Rx Divider (5.0 KHz Ref)
1	41.4875	6638	37.1875	5950
2	41.4750	6636	37.1750	5948
3	41.4625	6634	37.1625	5946
4	41.4500	6632	37.1500	5944
5	41.4375	6630	37.1375	5942
6	41.4250	6628	37.1250	5940
7	41.4125	6626	37.1125	5938
8	41.4000	6624	37.1000	5936
9	41.3875	6622	37.0875	5934
10	41.3750	6620	37.0750	5932
11	41.3625	6618	37.0625	5930
12	41.3500	6616	37.0500	5928
13	41.3375	6614	37.0375	5926
14	41.3250	6612	37.0250	5924
15	41.3125	6610	37.0125	5922



# DMD 5802/3

## Spain CT-1 Frequency Table

Base Set				
Channel Number	Tx Channel Frequencies (MHz)	Tx Divider (5.0 KHz Ref)	1st LO Frequencies (MHz) 1st 1F = 10.695 MHz	Rx Divider (5.0 KHz Ref)
1	31.0250	6205	29.2300	5846
2	31.0500	6210	29.2550	5851
3	31.0750	6215	29.2800	5856
4	31.1000	6220	29.3050	5861
5	31.1250	6225	29.3300	5866
6	31.1500	6230	29.3550	5871
7	31.1750	6235	29.3800	5876
8	31.2000	6240	29.4050	5881
9	31.2500	6250	29.4550	5891
10	31.2750	6255	29.4800	5896
11	31.3000	6260	29.5050	5901
12	31.3250	6265	29.5300	5906

Hand Set				
Channel Number	Tx Channel Frequencies (MHz)	Tx Divider (5.0 KHz Ref)	1st LO Frequencies (MHz) 1st 1F = 10.695 MHz	Rx Divider (5.0 KHz Ref)
1	39.8250	7885	20.3300	4066
2	39.9500	7990	20.3550	4071
3	39.9750	7995	20.3800	4076
4	40.0000	8000	20.4050	4081
5	40.0250	8005	20.4300	4086
6	40.0500	8010	20.4550	4091
7	40.0750	8015	20.4800	4096
8	40.1000	8020	20.5050	4101
9	40.1500	8030	20.5550	4111
10	40.1750	8035	20.5800	4116
11	40.2000	8040	20.6050	4121
12	40.2250	8045	20.6300	4126

## New Zealand CT-1 Frequency Table

Base Set				
Channel Number	Tx Channel Frequencies (MHz)	Tx Divider	1st LO Frequencies (MHz) 1st 1F = 10.7 MHz	Rx Divider (6.25 KHz Ref)
1	1.7820	1782	29.7625	4762
2	1.7620	1762	29.7500	4760
3	1.7420	1742	29.7375	4758
4	1.7220	1722	29.7250	4756
5	1.7020	1702	29.7125	4754
6	34.3500	5496	29.7000	4752
7	34.3625	5498	29.6875	4750
8	34.3750	5500	29.6750	4748
9	34.3875	5502	29.6625	4746
10	34.4000	5504	29.6500	4744

Hand Set				
Channel Number	Tx Channel Frequencies (MHz)	Tx Divider (6.25 KHz Ref)	1st LO Frequencies (MHz)	Rx Divider (5.0 KHz Ref)
1	40.4625	6474	2.2370	2237
2	40.4500	6472	2.2170	2217
3	40.4375	6470	2.1970	2197
4	40.4250	6468	2.1770	2177
5	40.4125	6466	2.1570	2157
6	40.4000	6464	23.6500	3784
7	40.3875	6462	23.6625	3786
8	40.3750	6460	23.6750	3788
9	40.3625	6458	23.6875	3790
10	40.3500	6456	23.7000	3792

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## Australia CT-1 Frequency Table

Base Set				
Channel Number	Tx Channel Frequencies (MHz)	Tx Divider (5.0 KHz Ref)	1st LO Frequencies (MHz) 1st 1F = 10.695 MHz	Rx Divider (5.0 KHz Ref)
1	30.0750	6015	29.0800	5816
2	30.1250	6025	29.1300	5826
3	30.1750	6035	29.1800	5836
4	30.2250	6045	29.2300	5846
5	30.2750	6055	29.2800	5856
6	30.1000	6020	29.1050	5821
7	30.1500	6030	29.1550	5831
8	30.2000	6040	29.2050	5841
9	30.2500	6050	29.2550	5851
10	30.3000	6060	29.3050	5861

Hand Set				
Channel Number	Tx Channel Frequencies (MHz)	Tx Divider (5.0 KHz Ref)	1st LO Frequencies (MHz) 1st 1F = 10.695 MHz	Rx Divider (5.0 KHz Ref)
1	39.7750	7955	19.3800	3876
2	39.8250	7965	19.4300	3886
3	39.8750	7975	19.4800	3906
4	39.9250	7985	19.5300	3916
5	39.9750	7995	19.5800	3881
6	39.8000	7960	19.4050	3891
7	39.8500	7970	19.4550	3901
8	39.9000	7980	19.5050	3901
9	39.9500	7990	19.5550	3911
10	40.0000	8000	19.6050	3921

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## U.K. CT-1 Frequency Table

Base Set				
Channel Number	Tx Channel Frequencies (MHz)	Tx Divider (1.0 KHz Ref)	1st LO Frequencies (MHz) 1st 1F = 10.7 MHz	Rx Divider (6.25 KHz Ref)
1	1.6420	1642	36.75625	5881
2	1.6620	1662	36.76875	5883
3	1.6820	1682	36.78125	5885
4	1.7020	1702	36.79375	5887
5	1.7220	1722	36.80625	5889
6	1.7420	1742	36.81875	5891
7	1.7620	1762	36.83125	5893
8	1.7820	1782	36.84375	5895

Hand Set				
Channel Number	Tx Channel Frequencies (MHz)	Tx Divider (6.25 KHz Ref)	1st LO Frequencies (MHz) 1st 1F = 455 MHz	Rx Divider (1.0 KHz Ref)
1	47.45625	7593	2.097	2097
2	47.46875	7595	2.117	2117
3	47.48125	7597	2.137	2137
4	47.49375	7599	2.157	2157
5	47.50625	7601	2.177	2177
6	47.51875	7603	2.197	2197
7	47.53125	7605	2.217	2217
8	47.54375	7607	2.237	2237