LCP02-150M

A.S.D.™

PROGRAMMABLE TRANSIENT VOLTAGE SUPPRESSOR FOR RINGING SLICS

FEATURES

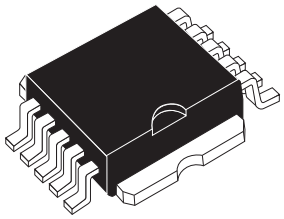
- Protection IC recommended for ringing SLICs.
- Wide firing voltage range: from -110V to +95V.
- Low gate triggering current
- Peak pulse current: I_{PP} = 100A (10/1000µs) .
- Holding current: I_H = 150mA min.
- High power dissipation capability
- UL497B approved (file E136224)

MAIN APPLICATIONS

- Dual battery supply voltage SLICs
  - negative battery supply configuration
  - negative & positive battery supply configuration
- Central Office (CO)
- Private Branch Exchange (PBX)
- Digital Loop Carrier (DLC)
- Asymmetrical Digital Subscriber Line (ADSL)
- Fiber in the Loop (FITL)
- Wireless Local Loop (WLL)
- Hybrid Fiber Coax (HFC)
- ISDN Terminal Adapter
- Cable modem

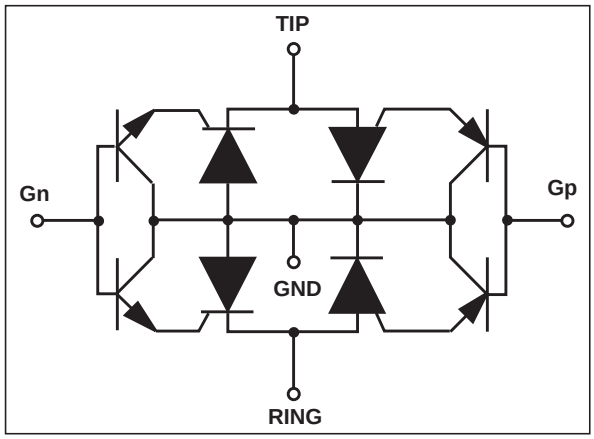
DESCRIPTION

The LCP02-150M has been developed to protect SLICs operating on both negative and positive supplies, as well as on high voltage SLICs. It provides crowbar mode protection for both TIP and RING lines. Surge suppression is assumed for each wire by two thyristor structures, one dedicated to positive surges, the second one to negative surges. Both positive and negative threshold levels are programmable by two gates (Gn and Gp). The use of transistors decreases the battery currents during surge suppression.
The LCP02-150M has high Bellcore Core, ITU-T and FCC Part 68 lightning surge ratings, ensuring rugged performance in the field.
The choice of the PowerSo-10™ package is driven by its high power dissipation capability.
In addition, the LCP02-150M is also specified to assist a designer to comply with UL1950, IEC950 and CSA C22.2. It is UL 497B approved (file E136224), and has UL94-V0 resin approved

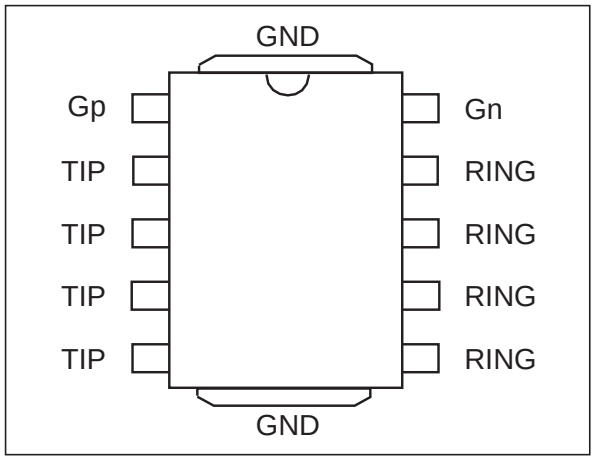


PowerS0-10™

FUNCTIONAL DIAGRAM



PIN-OUT CONFIGURATION



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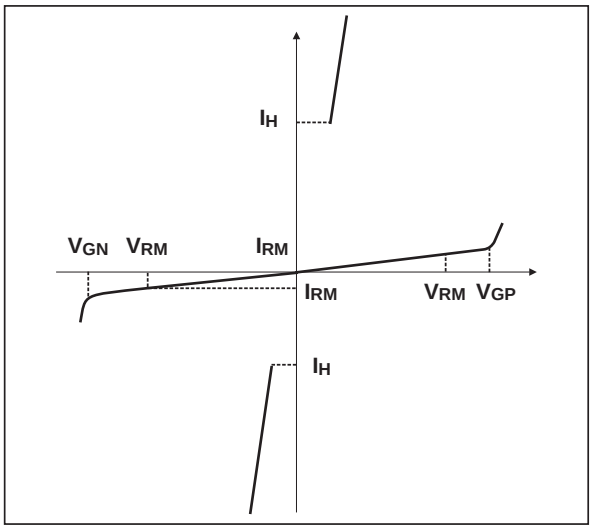
ELECTRICAL CHARACTERISTICS (Tamb = 25°C)

Symbol	Parameter
I_{GP}	Positive gate triggering current
I_{GN}	Negative gate triggering current
I_H	Holding current
I_{RG}	Reverse leakage current GATE / LINE
I_{RM}	Reverse leakage current
V_{RM}	Reverse voltage LINE/ GND
V_{DGL}	Dynamic switching voltage GATE / LINE
V_{GATE}	GATE / GND voltage
V_{RG}	Reverse voltage GATE / LINE
C	Capacitance LINE / GND



COMPLIES WITH FOLLOWING STANDARDS

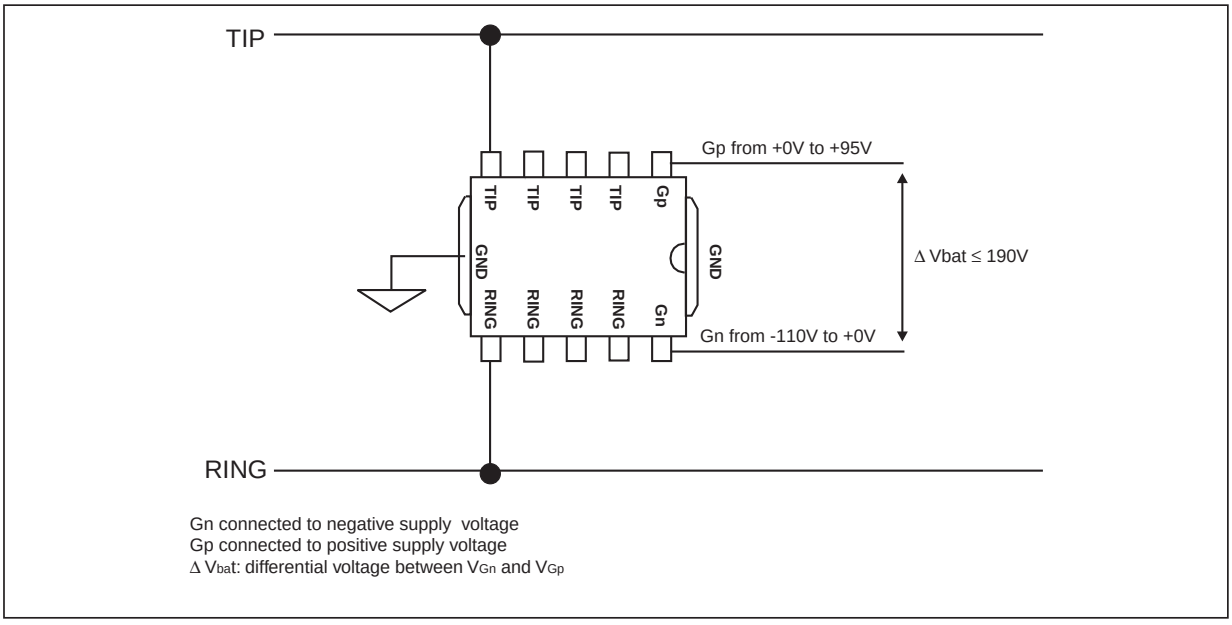
	Peak surge voltage (V)	Voltage waveform (µs)	Required peak current (A)	Current waveform (µs)	Minimum serial resistor to meet standard (Ω)
ITU-T K20	6000 1500	10/700 10/700	150 37.5	5/310 5/310	- -
ITU-T K21	6000 1500	10/700 10/700	150 37.5	5/310 5/310	- -
VDE0433	2000	10/700	50	5/310	-
VDE0878	2000	1.2/50	50	1/20	-
IEC61000-4-5	level 4 level 4	10/700 1.2/50	100 100	5/310 8/20	- -
FCC Part 68 lightning surge type A	1500 800	10/160 10/560	200 100	10/160 10/560	- -
FCC Part 68 lightning surge type B	1000	9/720	25	5/320	-
BELLCORE GR-1089-CORE First level	2500 1000	2/10 10/1000	500 100	2/10 10/1000	- -
BELLCORE GR-1089-CORE Second level	5000	2/10	500	2/10	-

ABSOLUTE RATINGS (T_{amb} = 25 °C)

Symbol	Parameter		Value	Unit
I_{PP}	Peak pulse current	10/1000µs 8/20µs 10/560µs 5/310µs 10/160µs 1/20µs 2/10µs	100 250 120 150 200 250 500	A
I_{TSM}	Non repetitive surge peak on-state current (sinusoidal)	t = 0.2 s t = 1s t = 15 min	13 10 3.5	A
V_{GN} max V_{GP} max ΔV_{bat} max	Maximum negative battery voltage range Maximum positive battery voltage range Total battery supply voltage	See fig.1	-110 to 0 0 to +95 190	V
T_{op}	Operating temperature range (see note 1)		-20 to +85	°C
T_{stg}	Storage temperature range		- 55 to + 150	°C
T_L	Maximum lead temperature for soldering during 10s		260	°C

Note 1: Within the Top range, the LCP02-150M keeps on operating. The impacts of the ambient temperature are given by derating curves.

Fig. 1: Test circuit



THERMAL RESISTANCE

Symbol	Parameter	Value	Unit
$R_{th\ (j-a)}$	Junction to ambient	60	°C/W

ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C)

1 - PARAMETERS RELATED TO THE NEGATIVE SUPPRESSOR

Symbol	Test conditions	Min.	Max.	Unit
I_{Gn}	$V_{Gn/GND}$ = -60V Measured at 50Hz		5	mA
I_{H-}	Go-No Go test, V_{Gn} = -60V	150		mA
I_{RGL-}	Tj = 25°C, $V_{Gn/line}$ = -190V		5	µA
V_{DGL-}	$V_{Gn/GND}$ = -60V 10/1000µs 1kV R_P = 25Ω I_{PP} = 30A 10/700µs 2kV R_P = 25Ω I_{PP} = 30A 1.2/50µs 2kV R_P = 25Ω I_{PP} = 30A		 10 6 12	V

2 - PARAMETERS RELATED TO THE POSITIVE SUPPRESSOR

Symbol	Test conditions	Min.	Max.	Unit
I_{Gp}	$V_{Gp/GND}$ = 60V Measured at 50Hz		10	mA
I_{RGL+}	Tj = 25°C, $V_{Gp/line}$ = +190V		5	µA
V_{DGL+}	$V_{Gp/GND}$ = +60V 10/1000µs 1kV R_P = 25Ω I_{PP} = 30A 10/700µs 2kV R_P = 25Ω I_{PP} = 30A 1.2/50µs 2kV R_P = 25Ω I_{PP} = 30A		 12 8 18	V

3 - PARAMETERS RELATED TO LINE/GND

Symbol	Test conditions	Typ.	Max.	Unit
I_R	Tj = 25°C, V_{LINE} = +90V, $V_{GP/LINE}$ = +1V Tj = 25°C, V_{LINE} = -105V, $V_{GN/LINE}$ = -1V		5 5	µA
C_{off}	V_R = -3V, F =1MHz, V_{Gp} = 60V, V_{Gn} = -60V	150		pF

Fig. 2: Non repetitive surge peak on state current versus overload duration (Tj initial = 25°C).

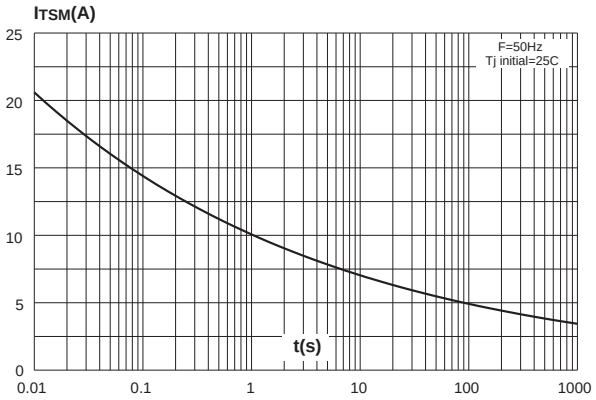


Fig. 3: Relative variation of holding current versus junction temperature.

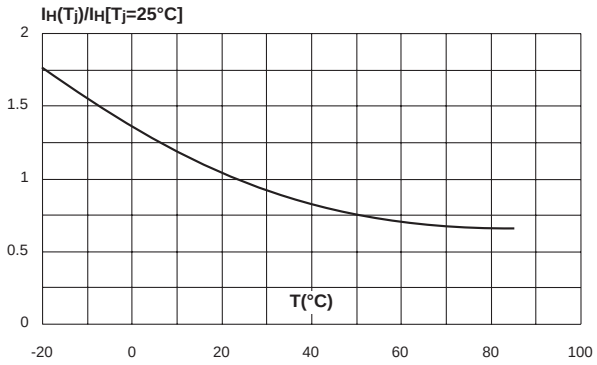


Fig. 4: Variation of junction capacitance versus reverse voltage applied (typical calues) with: V_{GN} = -90V and V_{GP} = +90V.

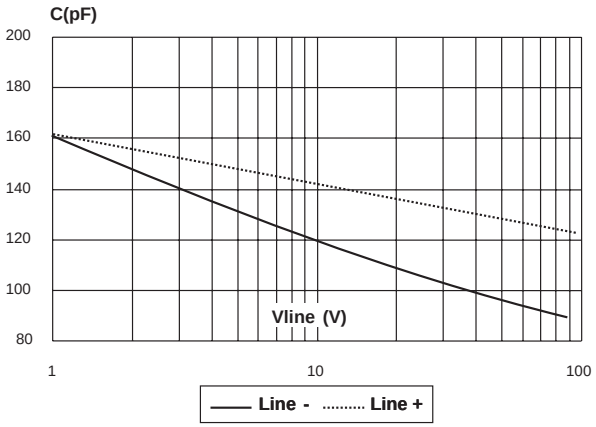


Fig. 5: LCP02 concept behavior.

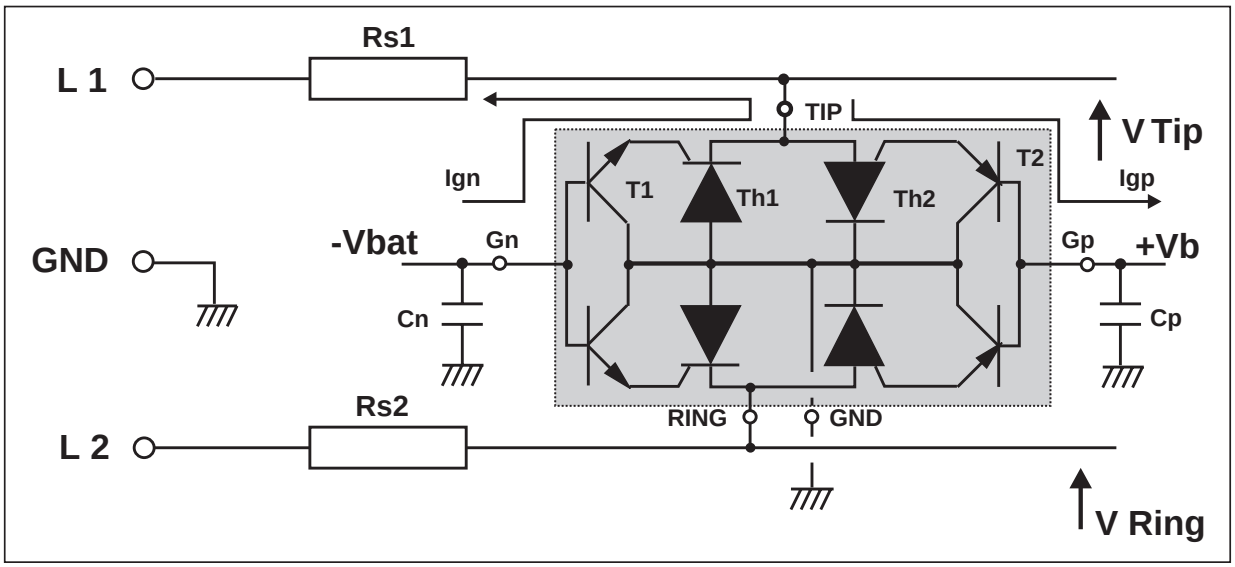


Figure 5 shows the classical protection circuit using the LCP02-150M crowbar concept. This topology has been developped to protect the new two-battery voltage SLICs. It allows both positive and negative firing thresholds to be programmed. The LCP02-150M has two gates (Gn and Gp). Gn is biased to negative battery voltage -Vbat, while Gp is biased to the positive battery voltage +Vb.

When a negative surge occurs on one wire (L1 for example), a current Ign flows through the base of the transistor T1 and then injects a current in the gate of the thyristor Th1 which fires. The entire surge current flows through the ground. After the surge, when the current flowing through Th1 becomes less negative than the negative holding current, Th1 switches off. This holding current I_{H-} is temperature dependant as per figure 2.

When a positive surge occurs on one wire (L1 for example), a current Igp flows through the base of the transistor T2 and then injects a current in the gate of the thyristor Th2 which fires. The entire surge current flows through the ground. After the surge, when the current flowing through Th2 becomes less positive than the positive holding current Ih+, Th2 switches off. This holding current I_{H+} is temperature dependant and is equal to 30mA at 25°C.

The capacitors Cn and Cp are used to speed up the crowbar structure firing during the fast surge rise or falling edges. This allows to minimize the dynamical breakover voltage at the SLIC Tip and Ring inputs during fast surges. Please note that these capacitors are generally available around the SLIC. To be efficient they have to be as close as possible to the LCP02-150M gate pins (Gn and Gp) and to the reference ground track (or plan). The optimized value for Cn and Cp is 220nF.

The series resistors Rs1 and Rs2 represent the fuse, fuse resistors or the PTCs which are needed to withstand the power contact or the power induction tests imposed by the country standards. Taking this factor into account, the actual lightning surge current flowing through the LCP02-150M is equal to :

$$I_{surge} = V_{surge} / (Rg + Rs)$$

With
V_{surge} = peak surge voltage imposed by the standard.
Rg = series resistor of the surge generator
Rs = series resistor of the line card (e.g. PTC)

The LCP02-150M topology is particularly optimized for the new telecom applications such as cable modem, fiber in the loop, WLL systems, and decentralized central office for example. The schematics of figures 6 and 7 give the 2 most frequent topologies used for these emergent applications.

Fig. 6: Protection of SLIC with positive and negative battery voltages.

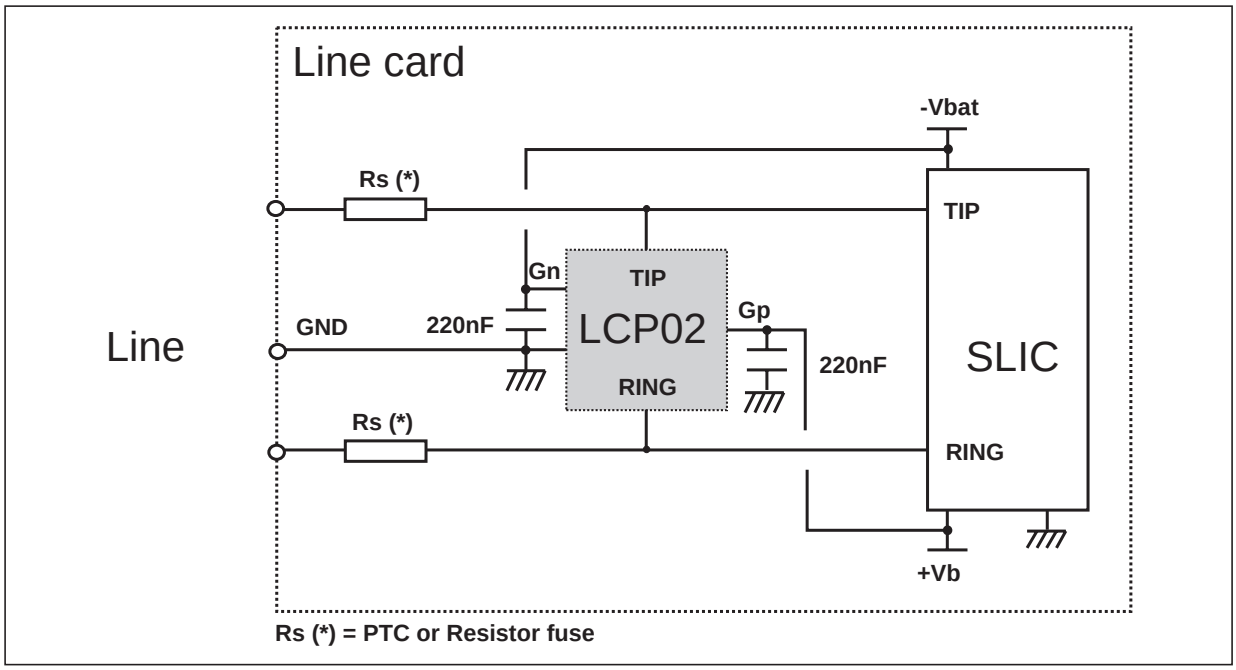


Fig. 7: Protection of high voltage SLIC

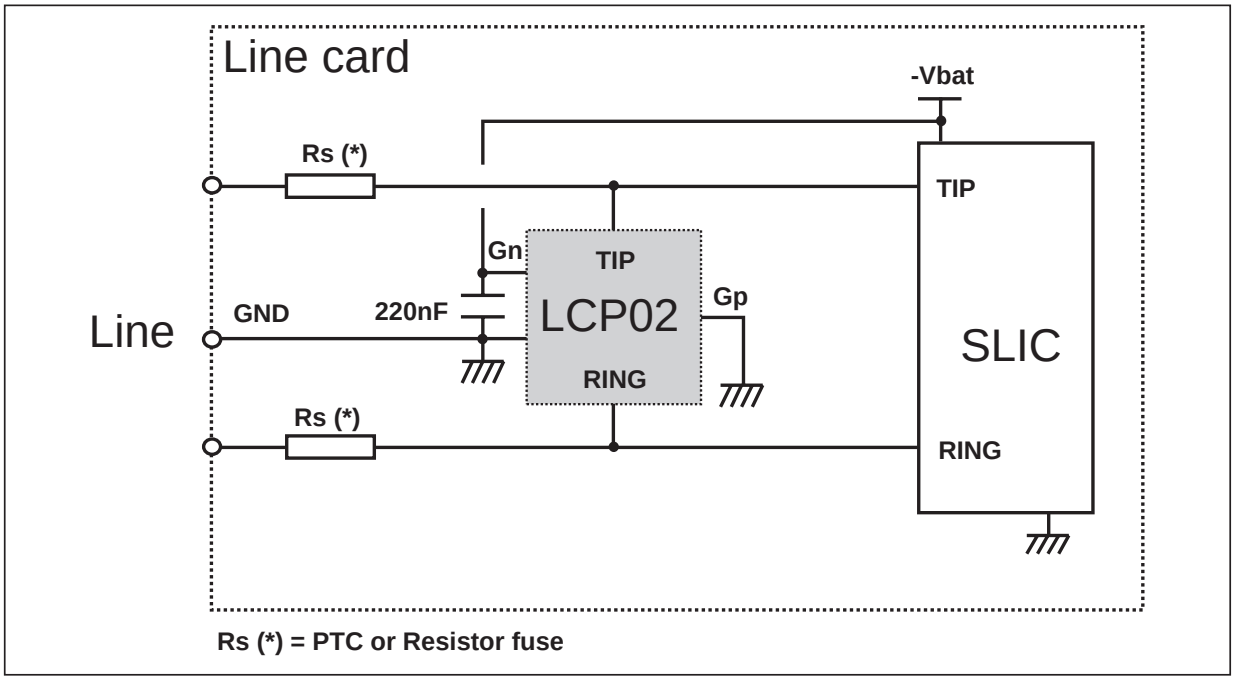
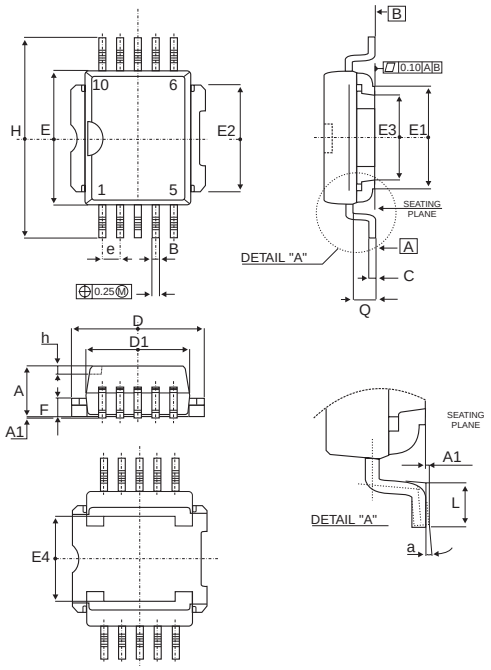


Figure 6 shows the classical protection topology for SLIC using both positive and negative battery voltages. With such a protection the SLIC is protected against surge over +Vb and lower than -Vbat. In this case, +Vb can be programmed up to +95V while -Vbat can be programmed down to -110V. Please note that the differential voltage does not exceed ΔV_{bat} max at 190V.

Figure 7 gives the protection topology for the new SLIC using high negative voltage down to -110V.

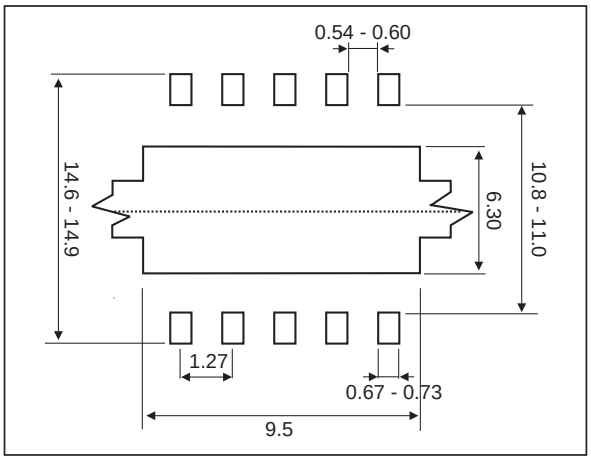
PACKAGE MECHANICAL DATA

PowerSO-10™ (Plastic)



REF.	DIMENSIONS			
	Millimeters		Inches	
	Min.	Max.	Min.	Max.
A	3.35	3.65	0.131	0.143
A1	0.00	0.10	0.00	0.0039
B	0.40	0.60	0.0157	0.0236
C	0.35	0.55	0.0137	0.0217
D	9.40	9.60	0.370	0.378
D1	7.40	7.60	0.291	0.299
E	9.30	9.50	0.366	0.374
E1	7.20	7.40	0.283	0.291
E2	7.20	7.60	0.283	0.299
E3	6.10	6.35	0.240	0.250
E4	5.90	6.10	0.232	0.240
e	1.27 Typ.		0.05 Typ.	
F	1.25	1.35	0.0492	0.0531
H	13.80	14.40	0.543	0.567
h	0.5 Typ.		0.019 Typ.	
L	1.20	1.80	0.0472	0.0708
Q	1.70 Typ		0.067 Typ.	
a	0°	8°	0°	8°

FOOTPRINT DIMENSIONS (in millimeters)



ORDER CODE

Ordering Type	Marking	Package	Weight	Base qty	Delivery mode
LCP02-150M	LCP02-150M	PowerSO-10	1.02 g	50	Tube
LCP02-150M-TR				600	Tape & Reel