DATA SHEET

TEA1401T
Power plug for the universal mains

Preliminary specification
Supersedes data of 1996 Sep 27
File under Integrated Circuits, IC03

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Philips
Semiconductors

PHILIPS

Power plug for the universal mains TEA1401T

FEATURES

- Designed for compact power plugs supplying up to 20 W
- Integrated high-voltage power DMOS FET 625 V/1 A
- Operates from all mains supplies (90 to 280 V AC)
- Major design: current regulation at the primary side (no opto-coupler, no secondary electronics)
- Low external/peripheral component count
- Combines accurate constant-voltage source (for supply) and accurate constant-current source (for charging) in one IC
- Foldback feature
- Requires simple input filter as a result of good EMC design
- Overshoot protection (output voltage)
- Protects against under-voltage input, over-current and over-temperature
- 20-pin SO medium-power package.

GENERAL DESCRIPTION

The TEA1401T is a Self Oscillating Power Supply (SOPS) controller IC that operates directly from the rectified universal mains. It is implemented in the BCD power logic 750 V process and includes the high voltage power switch making an integrated single-switch flyback converter.

Dedicated circuitry for high power efficiency is built-in, which makes a slim-line electronic power plug concept possible.

The basic function is a galvanically isolated, combined current and voltage source. No electronics are required at the secondary side of the transformer. Implementation of the TEA1401T renders a simple, small and accurate battery charger system. The TEA1401T is capable of self starting directly from the high voltage mains line.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{20}	output voltage at pin 20 (DRAIN)	20 times	–	–	625	V
I_{20}	current in MOS switch	peak value	–	–	1	A
f_{sw}	operating switching frequency range	C_{CPFM} = 470 pF	5	–	150	kHz
I_1	input current at pin 1 (V_{in}), from the high input voltage. V_{AT} can supply from the low voltage auxiliary winding	V_{AT} < 10 V (peak)	–	–	3	mA
		V_{AT} > 10 V (peak); f_{sw} = 90 kHz	–	430	530	µA
		V_{AT} > 10 V (peak); f_{sw} = 150 kHz	–	560	660	µA
I_{17}	average input current at pin 17 (V_{AT})	V_{AT} < 10 V (peak)	–	–	300	µA
		V_{AT} > 10 V (peak)	–	–	3	mA
T_{amb}	operating ambient temperature		–20	–	+85	°C

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TEA1401T	SO20	plastic small outline package; 20 leads; body width 7.5 mm	SOT163-1

BLOCK DIAGRAM

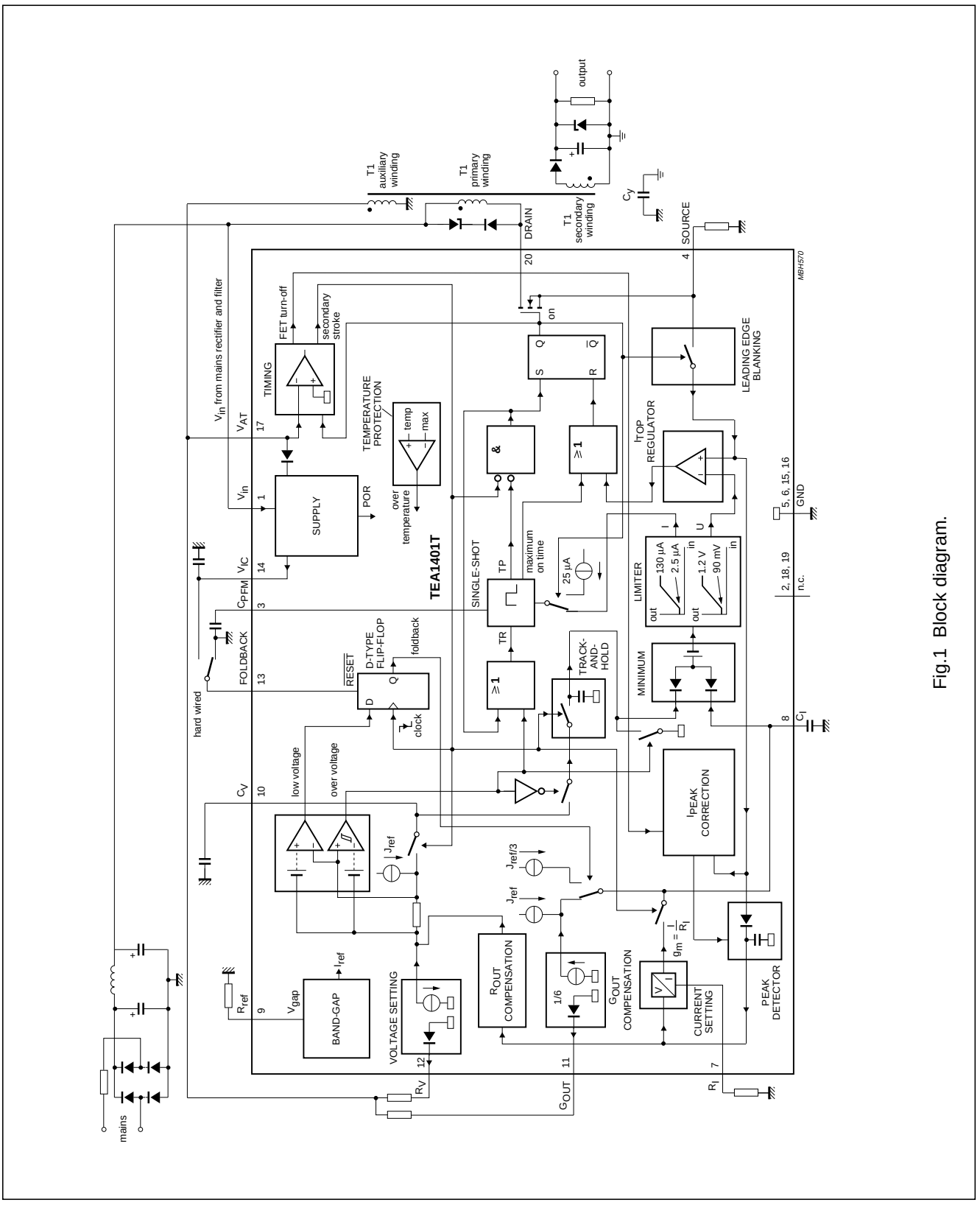


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
V_{in}	1	input for rectified and filtered mains voltage for initial powering
n.c.	2	not connected
C_{PFM}	3	frequency range setting for the pulse frequency modulation
SOURCE	4	source of internal MOS switch
GND1	5	ground 1
GND2	6	ground 2
R_I	7	setting of nominal output current
C_I	8	frequency compensation of current control loop
R_{ref}	9	setting of reference current
C_V	10	frequency compensation of voltage control loop
G_{OUT}	11	nulling of the output conductance of the current source function
R_V	12	setting of the nominal output voltage
FOLDBACK	13	enabling of the foldback feature in the output characteristic
V_{IC}	14	buffering of internal supply voltage
GND3	15	ground 3
GND4	16	ground 4
V_{AT}	17	input for voltage and power from auxiliary winding for timing and powering
n.c.	18	not connected
n.c.	19	not connected
DRAIN	20	drain of internal MOS switch

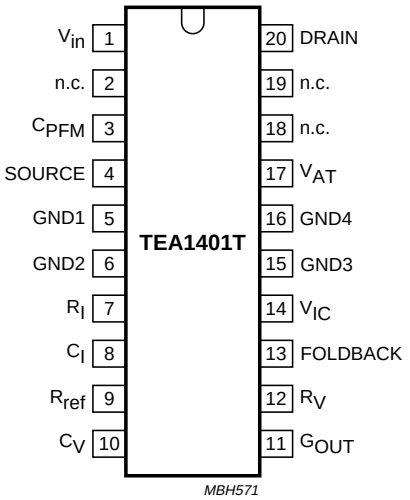


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

The TEA1401T is the heart of a compact flyback DC-to-DC converter, with the IC placed at the primary side.
An auxiliary primary winding of the transformer is used for indirect feedback to control the isolated output. This extra winding also powers the device.

Control of the converted power is carried out by current mode control and Pulse Frequency Modulation (PFM), as illustrated in Fig.1. The primary current is sensed by a comparator. The frequency is determined by the maximum of the transformer demagnetizing time and the time of the voltage controlled monostable multivibrator (single-shot).

The TEA1401T senses signals at the primary side of the transformer to reconstruct the current and voltage which are present at the secondary side. Comparison of these reconstructions with the internal reference leads to adaptation of the turn-off current level for the primary switch and also to adaptation of the single-shot time.

Current control (see Fig.3)

The current through the main switch is measured by the peak detector shown in Fig.1. The timing block generates a signal 'secondary stroke' which is logic 1 when the voltage of the auxiliary winding is negative.
The measured peak current, multiplied by the ratio of the resistors connected to pins 4 (SOURCE) and 7 (R_I), is integrated by a capacitor during the secondary stroke.

In this way a reconstruction is made of the secondary charge transfer. The charge estimation Q-pulse' (see Fig.3) is drawn from the capacitor at pin 8 (C_I) for each pulse. Also this capacitor, the charge error memory, is continuously charged with the reference current. In this way the real (reconstructed) current is compared with the reference yielding the voltage V_{CI} at pin 8. The V_{CI} level provides the turn-off current level for the main switch and the single-shot time.

Input from the voltage part of the loop is used to improve the current reconstruction, resulting in a lower output conductance of the complete converter. In the block diagram this is denoted as 'G_{OUT} compensation'.

The block 'I_{PEAK} correction' is able to increase the output from the peak detector to improve line regulation.

Voltage control

The voltage from the auxiliary winding is sensed as a measure of the secondary voltage. During the secondary stroke the auxiliary winding delivers a negative voltage. This voltage is converted into a current by an external resistor at the R_V pin between the transformer winding and virtual ground. This current is compared with a reference current.

The difference between the reconstructed voltage and the reference is integrated during the secondary stroke by a capacitor on the C_V pin. The voltage on the C_V pin is transferred, via a 'track-and-hold' circuit, to the connection point of the current and the voltage loop.
The 'track-and-hold' output provides the turn-off current level for the main switch and the single-shot time.

The 'track-and-hold' circuit itself is present for loop stability.

Input from the current part of the loop is used to improve the voltage reconstruction, resulting in lower output impedance of the complete converter (analog to the current control). In the block diagram this is denoted as 'R_{OUT} compensation'.

Combined control

The two loops, I loop and V loop, each request their own turn-off current level for the main switch and single-shot time. The block 'minimum' in the block diagram outputs the lowest value of the two, preventing the output voltage or current from exceeding its nominal value. The output characteristics of the power plug are displayed in Fig.4 (with enabled foldback option).

Optional foldback (see Fig.4)

The optional foldback feature of the TEA1401T is performed by sensing the voltage of the auxiliary winding at the end of the flyback stroke. It is actually not a voltage, but the current through pin 12 (R_V) that is measured. When this voltage is low, the reference current in the current control loop is set to the low level $J_{ref}/3$.

The steep foldback enables a turn-down of the converter by short-circuiting the output on the secondary side, for example by a switch-transistor.

Overshoot protection

Sensing the voltage during the previously mentioned flyback stroke is also used to signal a voltage overshoot. A voltage overshoot will delay and minimize the next active stroke. This is achieved by discharging the capacitor in the 'track-and-hold' circuit (see Fig.1). In this way the power level of the converter is turned down to its minimum immediately in case of a voltage overshoot.

Minimum output power

Under no-load condition an additional external pre-load resistor (or Zener diode) is necessary to keep the output voltage at its nominal value (or at the Zener diode voltage).

This is due to the fact that under no-load condition and also at voltage overshoot the converter will keep operating instead of being switched off. Although the converter then will operate with a short active stroke and a low frequency, energy is still being converted to the output. To prevent excessive output voltage this energy has to be dissipated.

The advantage of a pre-load resistor over a Zener diode is that the converter will stay in regulation, maintaining its fast response to load variations.

Duty cycle control

The momentary power level required by the I/V control loop is achieved by controlling the duty cycle of the converter by two actions. First the peak value of the primary current is controlled using a cycle-by-cycle current control. Secondly the pulse frequency is modulated. There is a broad region in which both regulation principles are active simultaneously. Both controls have a minimum and a maximum value which are set by the resistor on the SOURCE pin and the capacitor on the C_{PFM} pin.

SOPS and PFM

The switching frequency f_{sw} is set by the transformer demagnetizing time or the frequency control block within the IC (block 'single-shot' in Fig.1).

At a high power level the transformer determines the frequency. This mode of operation is called Self Oscillating Power Supply (SOPS), and provides maximum efficiency (for a non-continuous conducting flyback converter). In SOPS the next primary stroke is started right after the previous secondary stroke has ended. Timing information is collected from the auxiliary winding.

The SOPS frequency will increase when the power level decreases. The frequency however is limited by the PFM controller (single-shot). When the PFM controller takes over, the frequency will be proportional to the required power level. Thus the frequency is reduced when the power level decreases. In PFM there is a variable dead time after the secondary stroke. The next primary stroke is started after the single-shot time has ended.

Supply

Initially the IC is powered by a high DC input voltage at pin 1 (V_{in}). In operation the auxiliary winding takes over. In the event that the auxiliary winding delivers insufficient power for the internal circuitry of the IC, this deficit is supplemented again via pin 1 (V_{in}).

The supply voltage for the internal circuitry is buffered with an external capacitor at pin 14 (V_{IC}). When the auxiliary winding powers the IC, energy is stored during the active stroke. The rest of the time energy is supplied by the buffer capacitor.

Protections

The IC has a cycle-by-cycle current regulation, with a built-in setting for the absolute maximum voltage across the current sense resistor. Also a maximum time is set for the duration of the active stroke. A provision for temperature shut down has been implemented.

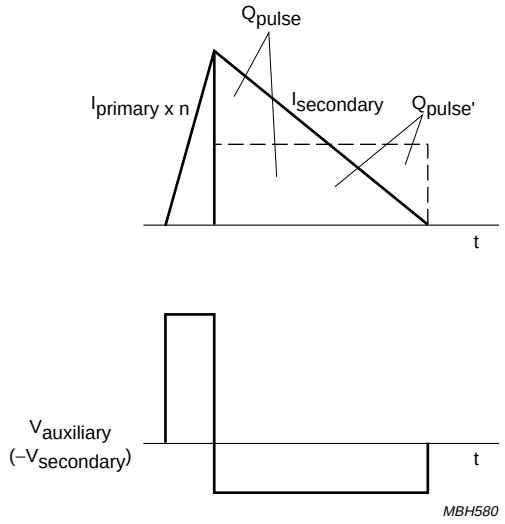


Fig.3 Reconstruction of secondary charge transfer.

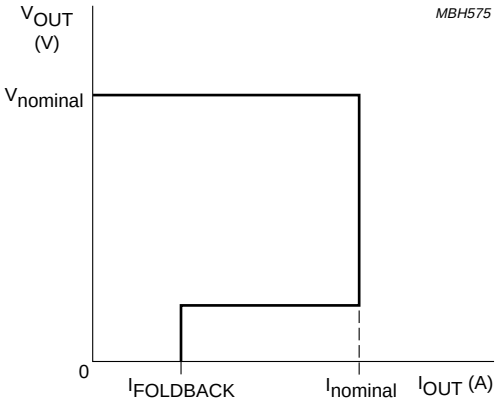


Fig.4 V/I ideal characteristics.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134). All voltages are measured with respect to ground; positive currents flow into the chip; pins 7, 9, 11 and 12 are not allowed to be voltage driven. The voltage ratings are valid provided other ratings are not being violated; current ratings are valid provided the maximum power rating is not violated.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
Voltages					
V_1	pin 1 (V_{in})	continuous	–0.4	+400	V
V_3	pin 3 (C_{PFM})		–0.4	–	V
V_4	pin 4 (SOURCE)		–0.4	+2	V
V_8	pin 8 (C_I)		–0.4	–	V
V_{10}	pin 10 (C_V)		–0.4	–	V
V_{13}	pin 13 (FOLDBACK)		–0.4	V_{IC} + 0.4	V
V_{14}	pin 14 (V_{IC})		–	–	V
V_{17}	pin 17 (V_{AT})		–20	+60	V
V_{20}	pin 20 (DRAIN)	continuous	–	+550	V
Currents					
I_3	pin 3 (C_{PFM})		–	0.2	mA
I_4	pin 4 (SOURCE)		–1	+1	A
I_7	pin 7 (R_I)		–0.2	0	mA
I_9	pin 9 (R_{ref})		–0.2	0	mA
I_{11}	pin 11 (G_{OUT})		–0.2	0	mA
I_{12}	pin 12 (R_V)		–0.2	0	mA
I_{14}	pin 14 (V_{IC})		–300	+1	mA
I_{20}	pin 20 (DRAIN)		–1	+1	A
General					
P_{tot}	total power dissipation	T_{amb} < 50 °C	–	1.4	W
T_{stg}	storage temperature		–55	+150	°C
T_{amb}	operating ambient temperature		–20	+85	°C
T_{vj}	virtual junction temperature		–20	+145	°C

QUALITY SPECIFICATION

According to *“SNW-FQ-611E”*. This specification can be found in the *“Quality reference Handbook”*. The handbook can be ordered using the code 9397 750 00192.

HANDLING

Every pin withstands the ESD test in accordance with the ‘Human Body Model’ except for pins V_{in} and DRAIN of which the performance is:

- Pin V_{in}: 1000 V in accordance with the ‘Human Body Model’
- Pin DRAIN: 1500 V in accordance with the ‘Human Body Model’.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient in free air[1]	65	K/W

Note

1. Pins GND1, GND2, GND3 and GND4 connected to sufficient copper area on the printed-circuit board.

CHARACTERISTICS

V_{in} = 330 V; V_{AT} = 36 V; R_{Rref} = 31 kΩ; T_{amb} = 25 °C; IC not in current foldback mode; no over-voltage; no over-temperature; unless otherwise specified. All voltages are measured with respect to ground; currents are positive when flowing into the IC.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{in}	input voltage		60	–	400	V
	input voltage limit	20 times	500	–	–	V
I_{in}	input supply current to V_{IC} and gate	V_{AT} = 3 V	1.7	2.3	2.9	mA
$I_{in(gate)}$	input supply current to gate only	V_{AT} = 36 V; non-switching	130	230	330	µA
V_{IC}	regulated supply voltage at V_{IC}	V_{AT} = 3 V	6.7	7.2	7.7	V
		V_{AT} = 36 V	7.2	7.9	8.6	V
$\Delta V_{IC}/\Delta R_O$	voltage decrease at V_{IC} due to its output impedance	V_{AT} = 20 V; I_{VIC} = 0 to –100 mA	–	–	200	mV
V_{POR}	power-on reset voltage level, with respect to regulated V_{IC}		–0.7	–0.5	–0.1	V
$I_{LI(VAT)}$	leakage current into pin V_{AT}	V_{AT} = 6 V	–	–	2	µA
V_{VAT}	V_{AT} input voltage		–20	–	+60	V
I_{VAT}	V_{AT} input current	V_{AT} = 70 V; I_{VIC} = 0 mA	11	14	17	mA
Pulse peak modulator						
$V_{SOURCE(max)}$	maximum peak voltage at pin SOURCE	$V_{CV} = V_{CI}$ = 4 V; $\frac{dV_{SOURCE}}{dt}$ = 1 V/µs	1.09	1.19	1.29	V
		$V_{CV} = V_{CI}$ = 4 V; $\frac{dV_{SOURCE}}{dt}$ = 0.1 V/µs	1.05	1.15	1.25	V
$V_{SOURCE(min)}$	minimum peak voltage at pin SOURCE	$V_{CV} = V_{CI}$ = 0 V; $t_{on} > t_{on(min)}$	75	95	120	mV
$\Delta V_{CV\text{-}SOURCE}$	level shift voltage V_{CI} to V_{SOURCE}	V_{CV} = 4 V	–	2	–	V
$\Delta V_{CI\text{-}SOURCE}$	level shift voltage V_{CV} to V_{SOURCE}	V_{CI} = 4 V	–	2	–	V
$t_{on(min)}$	minimum on-time (the minimum time duration of the active stroke)	V-mode	490	550	610	ns
		I-mode	675	750	825	ns

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Pulse (maximum) frequency modulator						
$R_{discharge}$	discharge resistance to ground	V_{CPFM} = 1.0 V	0.3	0.6	0.9	kΩ
$I_{charge(min)}$	minimum charge current	$V_{CV} = V_{CI}$ = 0 V	–	2.5	–	µA
$I_{charge(max)}$	maximum charge current	$V_{CV} = V_{CI}$ = 4 V	–	130	–	µA
$I_{charge(fix)}$	fixed charge current	active stroke	–	25	–	µA
$G_{transferCI}$	transfer from pin C_I to pin C_{PFM}	V_{CI} = 2.1 to 3.1 V	–	–104	–	µA/V
$G_{transferCV}$	transfer from pin C_V to pin C_{PFM}	V_{CV} = 2.1 to 3.1 V	–	–104	–	µA/V
$V_{sw(high)}$	high switching voltage level at pin C_{PFM}		–	1.0	–	V
$V_{sw(low)}$	low switching voltage level at pin C_{PFM}	DC at pin C_{PFM}	–	0.17	–	V
$V_{ton(max)}$	maximum on-time $t_{on(max)}$ switching voltage level at pin C_{PFM}		–	0.54	–	V
Δf_{PFM}	frequency spread of the internal oscillator; $\frac{G_{transferCI}}{V_{sw(high)}}$; $\frac{G_{transferCV}}{V_{sw(high)}}$	$V_{CI} = V_{CV}$ = 2.1 to 3.1 V	93	104	115	µA/V^2
$\Delta t_{on(max)}$	spread of $t_{on(max)}$; $\frac{V_{ton(max)}}{I_{charge(fix)}}$	$V_{CI} = V_{CV}$ = 4 V; V_{SOURCE} < 1 V	19	22	25	V/mA
SOPS						
V_{demag}	demagnetization recognition voltage level		–250	–130	–10	mV
Current regulation						
$V_{i(pkc)}$	V_{PEAK}-I converter input voltage		0.6	–	1.4	V
$V_{i(pkc)(slope)}$	V_{PEAK}-I converter input voltage slope		0.1	–	1.0	V/µs
$V_{pkc(offset)}$	V_{PEAK}-I converter systematic offset	$\frac{dV_{SOURCE}}{dt} > 0.1$ V/µs	–	–13	–	mV
$I_{transfer(RI-CI)}$	R_I to C_I current transfer	I_{GOUT} = 0	–	–0.99	–	A/A
$I_{transfer(GOUT-CI)}$	G_{OUT} to C_I current transfer	I_{RI} = 0	–	0.17	–	A/A
$I_{PEAKcor}$	current through sense capacitor in block 'I_{PEAK} correction' (see Fig.1); sunk by pin FOLDBACK	under test conditions: in lasting active stroke	7	10	13	µA
$I_{chain(CI)}$	C_I chain error current		–3.3	–1.0	+1.3	µA
$I_{ctrl(error)}$	current control total measured error		–5	–	+5	%

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Voltage regulation						
$I_{transfer(RV-CV)}$	R_V to C_V current transfer	V_{RI} < 0.5 V	–	–1.00	–	A/A
$V_{thres(RI)}$	R_{OUT} converter voltage threshold at pin R_I		–	0.65	–	V
$g_{m(ROUT)}$	R_{OUT} converter transconductance I_{CV}/V_{RI}	V_{RI} > 0.7 V	–	4.4	–	µA/V
$I_{chain(CV)}$	C_V chain error current	I_{CV} measurement, analogue to that of $I_{chain(CI)}$	–1.2	0	+1.2	µA
$V_{ctrl(error)}$	total error of voltage control loop in IC		–4	–	+4	%
Current foldback; FOLDBACK (pin 13) connected to V_{IC} (pin 14)						
I_{RV}/I_{Rref}	current ratio discrimination level		0.05	0.1	0.2	A/A
$I_{CI(foldback)}/I_{CI(normal)}$	current ratio		0.26	0.33	0.4	A/A
Voltage overshoot						
I_{RV}/I_{Rref}	current ratio discrimination level		1.1	1.2	1.3	A/A
$V_{4(overshoot)}$	peak voltage at pin 4	at overshoot; $t_{on} > t_{on(min)}$	75	95	120	mV
$I_{charge(overshoot)}$	C_{PFM} charge current	at overshoot; V_{CPFM} = 1 V	–	2.5	–	µA
References						
V_{ref}	R_{ref} reference voltage		1.24	1.28	1.32	V
$I_{transfer(Rref-CI)}$	R_{ref} to C_I current transfer		–	0.99	–	A/A
$I_{transfer(Rref-CV)}$	R_{ref} to C_V current transfer		–	0.99	–	A/A
Output stage						
I_{LO}	DRAIN output leakage current	V_{DRAIN} = 550 V	–	–	100	µA
$V_{DRAIN(cont)}$	DRAIN output voltage	continuous	0	–	550	V
$V_{DRAIN(lim)}$	DRAIN output voltage limit	20 times	625	–	–	V
$\Delta V_{DRAIN-SOURCE}$	DRAIN-SOURCE voltage drop	T_{amb} = 25 °C; I_{DRAIN} = 500 mA	–	–	6	V
		T_{amb} = 125 °C; I_{DRAIN} = 500 mA	–	–	11	V
t_f	DRAIN fall time	V_{in} = 300 V; no external capacitor at pin DRAIN	–	100	–	ns
Temperature protection						
$T_{prot(max)}$	maximum temperature threshold		132	139	146	°C
$T_{prot(hyst)}$	hysteresis temperature		–	±1	–	°C

OUTPUT CHARACTERISTICS OF COMPLETE POWER PLUG

Output power

Maximum switching frequency is approximately 150 kHz. Internal MOS maximum switch current is 0.5 to 1 A. Maximum handled power with universal mains is approximately 10 W.

Accuracy of current regulation

The accuracy of the IC itself is ±5%. Accuracy of the complete converter is approximately ±7%, depending on the transformer and other components.

Accuracy of voltage regulation

The voltage loop inside the IC has an accuracy of ±4%. Accuracy of the complete converter is approximately ±7%.

Voltage overshoot

When voltage overshoot is detected (during the secondary stroke), the IC first has to wait until this stroke is finished in the normal way. After that the power level of the converter is set to the minimum level within one cycle.

Voltage overshoot is triggered at 20% above nominal output voltage. If at the moment that overshoot is detected, the transformer still contains energy; this energy can cause some further increase of the output voltage.

In case of a pre-load resistor across the output, the converter keeps the output voltage under static conditions on its nominal value. Voltage overshoot will only be a dynamic phenomenon in this situation. When only a Zener diode is applied, the Zener voltage will appear at the output continuously under no-load conditions.

Efficiency

An efficiency of 72 to 75% at maximum output power can be achieved for a complete 8 W converter designed for universal mains.

Ripple

The magnitude of the ripple in output voltage is determined by the duty cycle of the converter, the output current level and the value and Electrical Series Resistance (ESR) of the output capacitor.

A minimal ripple is obtained in a system designed on a maximum duty cycle of 50% under normal operating conditions and a minimized dead time.

Ripple is inversely proportional to input and output voltages.

INPUT CHARACTERISTICS OF COMPLETE POWER PLUG

Input voltage

The input voltage range comprises the universal AC-mains (90 to 280 V). The input transient voltage must be filtered to a maximum of 450 V.

APPLICATION INFORMATION

A converter with the TEA1401T consists of an input filter, a transformer with a third winding (auxiliary), a secondary diode with a capacitor plus other external components as illustrated in Fig.5. The load (user) determines the operating mode of the power plug, current or voltage source.

The capacitor at V_{IC} (pin 14) buffers the internal supply voltage of the IC which is powered via V_{in} and/or V_{AT}.

A sense resistor converts the primary current into a voltage at SOURCE (pin 4). The voltage of the auxiliary winding is converted into a current through resistor R_{RV} and fed to pin R_V.

Nominal current and voltage are set by resistors R_{RI} and R_{RV}. Output conductance of the current is nullified by resistor R_{RGOUT}. The band-gap voltage is converted into a reference current by resistor R_{Rref}. Capacitor C_{CPFM} determines the frequency in non-SOPS mode.

There are two loop capacitors, one for current control (C_I), and the other for voltage control (C_V). The impedance at C_V (pin 10) can be made more complex, if required for stability.

The secondary diode also protects the power plug against a short-circuited output (during the primary stroke), and must therefore be placed inside the power plug cabinet. A pre-load resistor or a Zener diode is required to handle an open output which will cause an excessively high output voltage. This is because the power plug continues operating, provided it is connected to the mains, and thus continuously converts energy to the secondary side, even though it is a low, predefined level.

If a Zener diode is used, the Zener voltage must be selected with care, because the over-voltage protection of the IC should not be blocked. If the Zener diode voltage is too close to the nominal output voltage of the converter no voltage overshoot will be detected by the IC, causing increased dissipation in the Zener during switching of the load.

A complete diagram with preliminary component values is shown in Fig.6. More detailed information can be found in the *“Application Note AN96096”*.

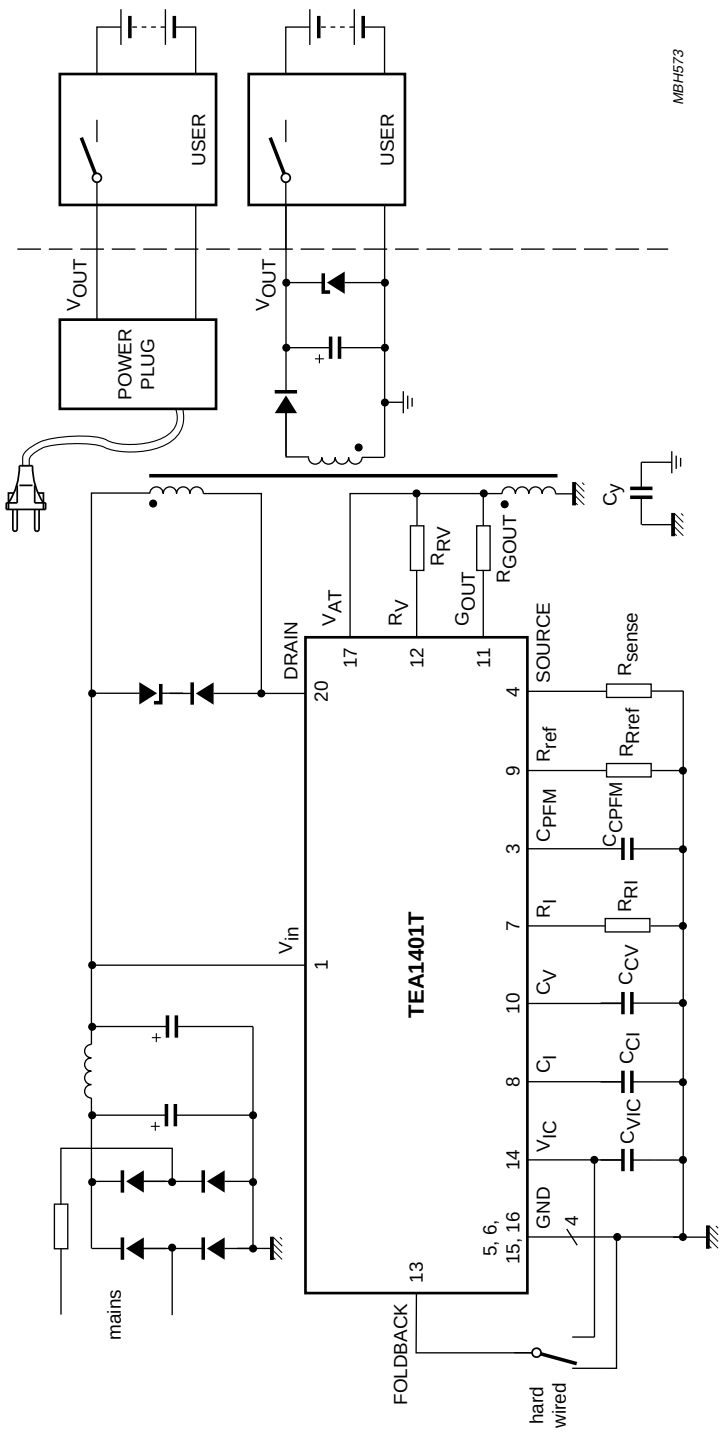
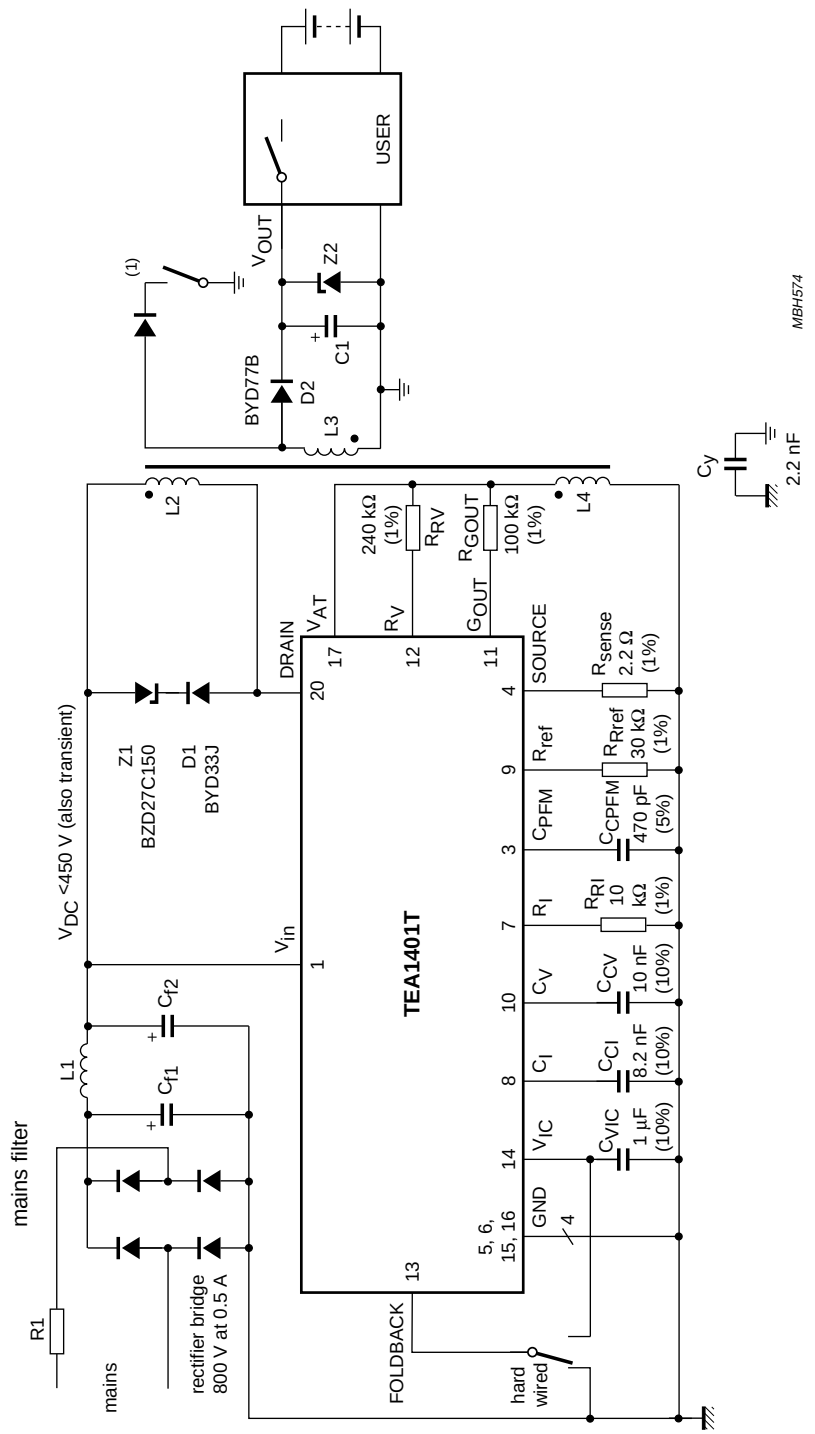


Fig.5 Power plug with TEA1401T.

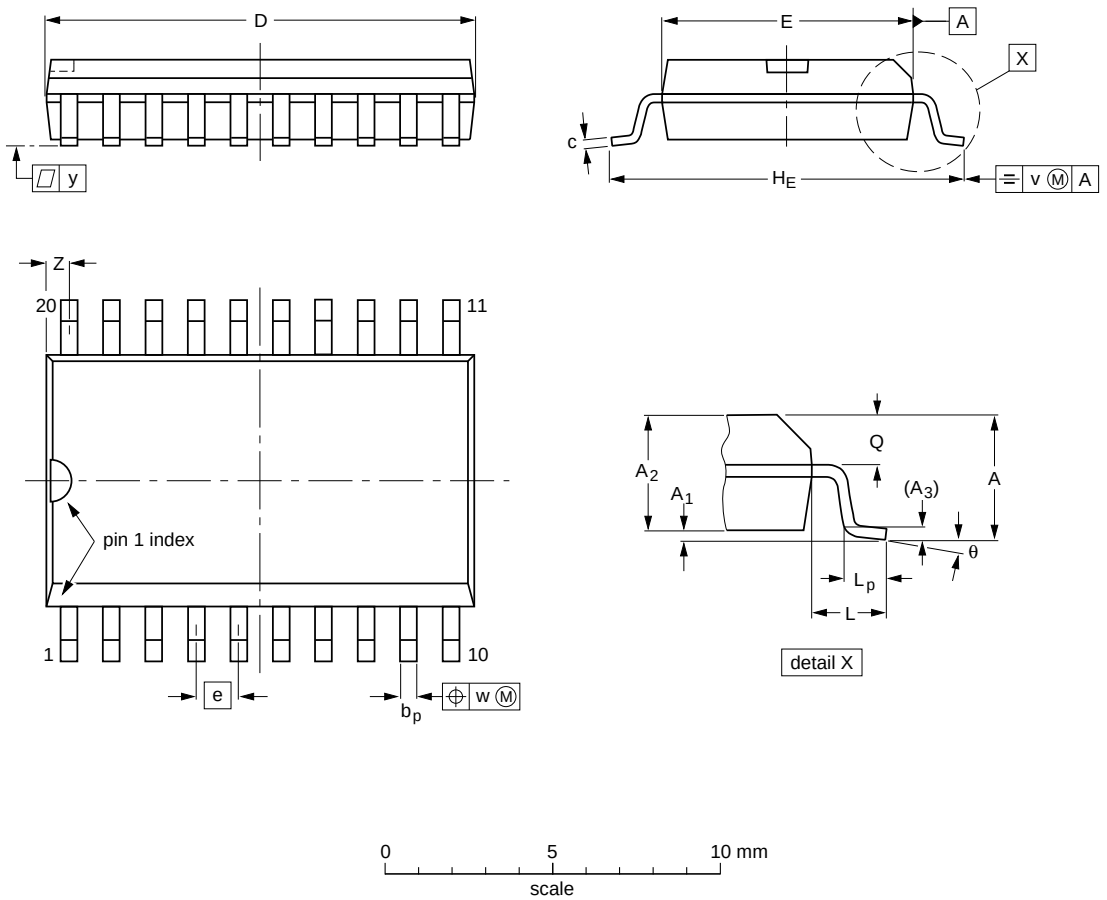


(1) Optional short-circuit provision based on FOLDBACK feature.
C1 = 330 µF 16 V 10%; C_{f1} = C_{f2} = 6.8 µF 385 V 10%.
L1 = inductance filter = 560 µH 10%; L2 = 62 turns 0.14 copper inductance; L3 = 8 turns 0.4 copper inductance; L4 = 8 turns 0.14 copper inductance; core EF16/16/5 gap 130 µ.
R1 = R_{fuse} = 18 Ω 5% at 0.5 W.
Z2 = BZV55B12 2% at 0.4 W.

Fig.6 Power plug with TEA1401T; completed circuit diagram.

PACKAGE OUTLINE

SO20: plastic small outline package; 20 leads; body width 7.5 mm **SOT163-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (1)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	2.65	0.30 0.10	2.45 2.25	0.25	0.49 0.36	0.32 0.23	13.0 12.6	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8^o 0^o
inches	0.10	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.51 0.49	0.30 0.29	0.050	0.42 0.39	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT163-1	075E04	MS-013AC				~~92-11-17~~ 95-01-24

SOLDERING

Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"IC Package Databook"* (order code 9398 652 90011).

Reflow soldering

Reflow soldering techniques are suitable for all SO packages.

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt. Dwell times vary between 50 and 300 seconds depending on heating method. Typical reflow temperatures range from 215 to 250 °C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 minutes at 45 °C.

Wave soldering

Wave soldering techniques can be used for all SO packages if the following conditions are observed:

- A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.
- The longitudinal axis of the package footprint must be parallel to the solder flow.
- The package footprint must incorporate solder thieves at the downstream end.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder is 10 seconds, if cooled to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Repairing soldered joints

Fix the component by first soldering two diagonally-opposite end leads. Use only a low voltage soldering iron (less than 24 V) applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

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