

## CD4512BC 8-Channel Buffered Data Selector

### General Description

The CD4512BC buffered 8-channel data selector is a complementary MOS (CMOS) circuit constructed with N- and P-channel enhancement mode transistors. This data selector is primarily used as a digital signal multiplexer selecting 1 of 8 inputs and routing the signal to a 3-STATE output. A high level at the Inhibit input forces a low level at the output. A high level at the Output Enable (OE) input forces the output into the 3-STATE condition. Low levels at both the Inhibit and (OE) inputs allow normal operation.

### Features

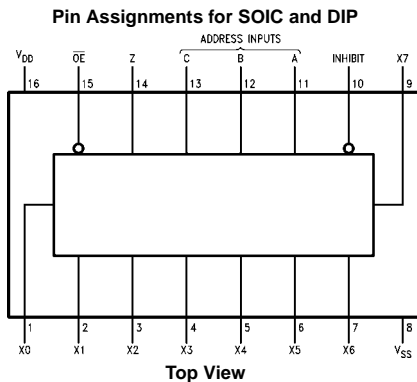
- Wide supply voltage range: 3.0V to 15V
- High noise immunity:  $0.45 V_{DD}$  (typ.)
- 3-STATE output
- Low quiescent power dissipation:  
0.25  $\mu$ W/package (typ.) @  $V_{CC} = 5.0V$
- Plug-in replacement for Motorola MC14512

### Ordering Code:

Order Number	Package Number	Package Description
CD4512BCM	M16A	16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow Body
CD4512BCN	N16E	16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

Devices also available in Tape and Reel. Specify by appending suffix "X" to the ordering code.

### Connection Diagram



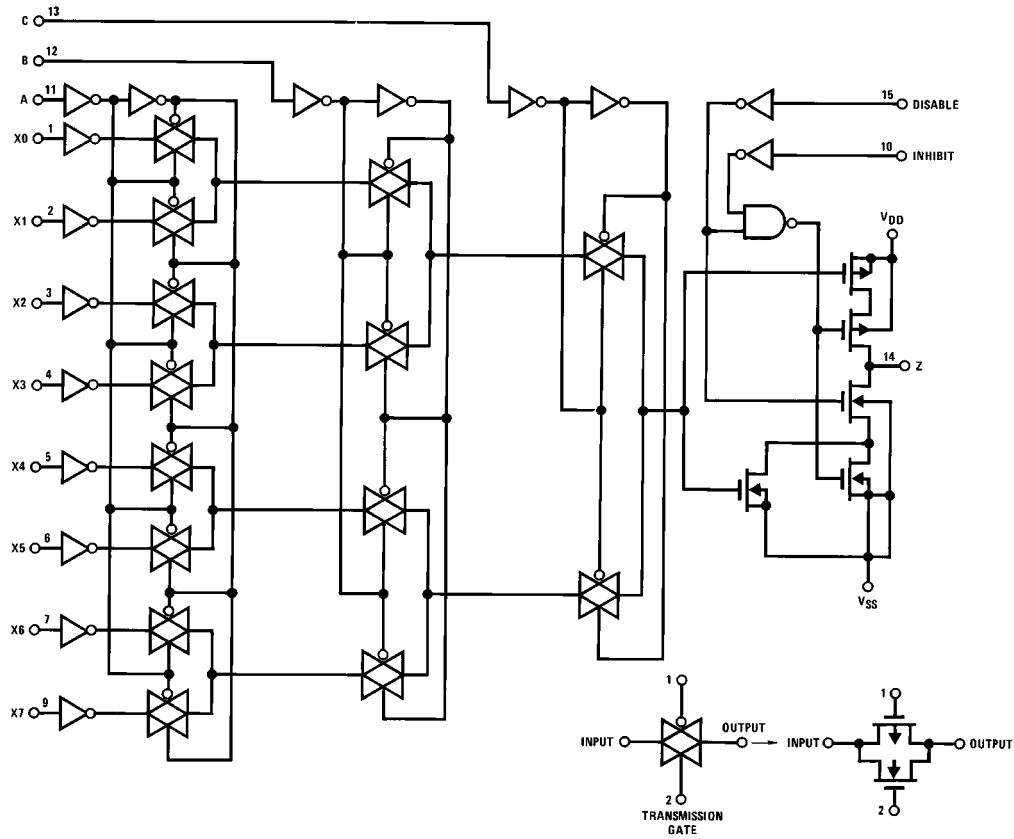
### Truth Table

Address Inputs			Control Inputs		Output
C	B	A	Inhibit	OE	Z
0	0	0	0	0	X0
0	0	1	0	0	X1
0	1	0	0	0	X2
0	1	1	0	0	X3
1	0	0	0	0	X4
1	0	1	0	0	X5
1	1	0	0	0	X6
1	1	1	0	0	X7
2	1	1	1	0	0
2	2	2	2	1	Hi-Z

2 = Don't care  
Hi-Z = 3-STATE condition  
Xn = Data at input n

CD4512BC

### Logic Diagram



<b>Absolute Maximum Ratings</b> (Note 1)		<b>Recommended Operating Conditions</b> (Note 2)	
(Note 2)			
Supply Voltage ( $V_{DD}$ )	-0.5 to +18 $V_{DC}$	DC Supply Voltage ( $V_{DD}$ )	3.0 to 15 $V_{DC}$
Input Voltage ( $V_{IN}$ )	-0.5 to $V_{DD} + 0.5 V_{DC}$	Input Voltage ( $V_{IN}$ )	0 to $V_{DD} V_{DC}$
Storage Temperature Range ( $T_S$ )	-65°C to +150°C	Operating Temperature Range ( $T_A$ )	-40°C to +85°C
Power Dissipation ( $P_D$ )		<b>Note 1:</b> "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The Recommended Operating Conditions and Electrical Characteristics table provide conditions for actual device operation.	
Dual-In-Line	700 mW	<b>Note 2:</b> $V_{SS} = 0V$ unless otherwise specified.	
Small Outline	500 mW		
Lead Temperature, ( $T_L$ )			
(Soldering, 10 seconds)	260°C		

**DC Electrical Characteristics** (Note 2)

Symbol	Parameter	Conditions	-40°C		+25°C			+85°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
$I_{DD}$	Quiescent Device Current	$V_{DD} = 5V, V_{IN} = V_{DD} \text{ or } V_{SS}$		20		0.005	20	150	$\mu A$	
		$V_{DD} = 10V, V_{IN} = V_{DD} \text{ or } V_{SS}$		40		0.010	40	300	$\mu A$	
		$V_{DD} = 15V, V_{IN} = V_{DD} \text{ or } V_{SS}$		80		0.015	80	600	$\mu A$	
$V_{OL}$	LOW Level Output Voltage	$V_{DD} = 5V$		0.05		0	0.05	0.05	V	
		$V_{DD} = 10V$ $ I_{OL}  < 1 \mu A$		0.05		0	0.05	0.05	V	
		$V_{DD} = 15V$		0.05		0	0.05	0.05	V	
$V_{OH}$	HIGH Level Output Voltage	$V_{DD} = 5V$	4.95		4.95	5.0		4.95	V	
		$V_{DD} = 10V$ $ I_{OH}  < 1 \mu A$	9.95		9.95	10.0		9.95	V	
		$V_{DD} = 15V$	14.95		14.95	15.0		14.95	V	
$V_{IL}$	LOW Level Input Voltage	$V_{DD} = 5V, V_O = 0.5V$		1.5		2.25	1.5	1.5	V	
		$V_{DD} = 10V, V_O = 1.0V$		3.0		4.50	3.0	3.0	V	
		$V_{DD} = 15V, V_O = 1.5V$		4.0		6.75	4.0	4.0	V	
$V_{IH}$	HIGH Level Input Voltage	$V_{DD} = 5V, V_O = 4.5V$	3.5		3.5	2.75		3.5	V	
		$V_{DD} = 10V, V_O = 9.0V$	7.0		7.0	5.50		7.0	V	
		$V_{DD} = 15V, V_O = 13.5V$	11.0		11.0	8.25		11.0	V	
$I_{OL}$	LOW Level Output Current (Note 3)	$V_{DD} = 5V, V_O = 0.4V$	0.52		0.44	0.78		0.36	mA	
		$V_{DD} = 10V, V_O = 0.5V$	1.3		1.1	2.0		0.9	mA	
		$V_{DD} = 15V, V_O = 1.5V$	3.6		3.4	7.8		2.4	mA	
$I_{OH}$	HIGH Level Output Current (Note 3)	$V_{DD} = 5V, V_O = 4.6V$	-0.2		-0.16			-0.12	mA	
		$V_{DD} = 10V, V_O = 9.5$	-0.5		-0.4			-0.3	mA	
		$V_{DD} = 15V, V_O = 13.5V$	-1.4		-1.2			-1.0	mA	
$I_{IN}$	Input Current	$V_{DD} = 15V, V_{IN} = 0V$		-0.3		$-10^{-5}$	-0.3	-1.0	$\mu A$	
		$V_{DD} = 15V, V_{IN} = 15V$		0.3		$10^{-5}$	0.3	1.0	$\mu A$	
$I_{OZ}$	3-STATE Output Current	$V_{DD} = 15V, V_O = 0V$		$\pm 1.0$		$\pm 10^{-5}$	$\pm 1.0$	$\pm 7.5$	$\mu A$	

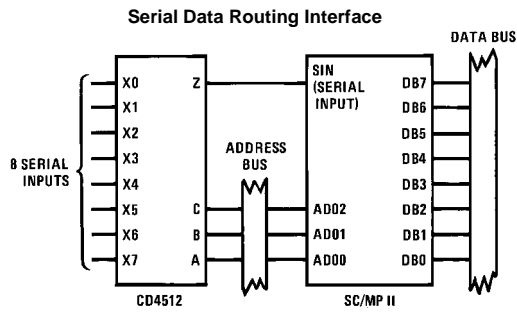
**Note 3:**  $I_{OH}$  and  $I_{OL}$  are tested one output at a time.

**AC Electrical Characteristics** (Note 4) $T_A = 25^\circ\text{C}$ ,  $t_r = t_f = 20 \text{ ns}$ ,  $C_L = 50 \text{ pF}$ 

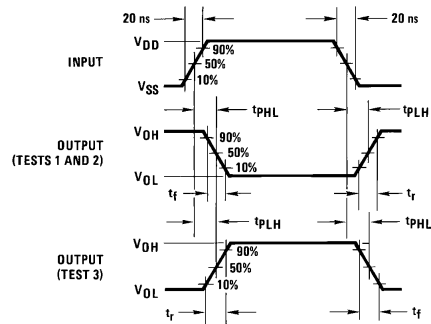
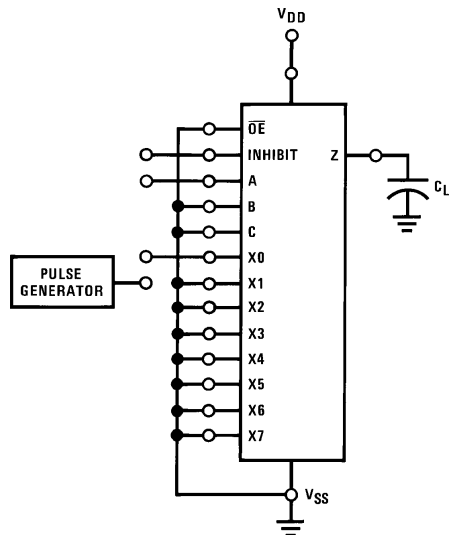
Symbol	Parameter	Conditions	CD4512BM			CD4512BC			Units
			Min	Typ	Max	Min	Typ	Max	
$t_{PHL}$	Propagation Delay HIGH-to-LOW Level	$V_{DD} = 5V$		225	500		225	750	ns
		$V_{DD} = 10V$		75	175		75	200	ns
		$V_{DD} = 15V$		57	130		57	150	ns
$t_{PLH}$	Propagation Delay LOW-to-HIGH Level	$V_{DD} = 5V$		225	500		225	750	ns
		$V_{DD} = 10V$		75	175		75	200	ns
		$V_{DD} = 15V$		57	130		57	150	ns
$t_{THL}, t_{TLH}$	Transition Time	$V_{DD} = 5V$		70	200		70	200	ns
		$V_{DD} = 10V$		35	100		35	100	ns
		$V_{DD} = 15V$		25	80		25	80	ns
$t_{PHZ}, t_{PLZ}$	Propagation Delay into 3-STATE from Logic Level	$V_{DD} = 5V$		50	125		50	125	ns
		$V_{DD} = 10V$		25	75		25	75	ns
		$V_{DD} = 15V$		19	60		19	60	ns
$t_{PZH}, t_{PZL}$	Propagation Delay to Logic Level from 3-STATE	$V_{DD} = 5V$		50	125		50	125	ns
		$V_{DD} = 10V$		25	75		25	75	ns
		$V_{DD} = 15V$		19	60		19	60	ns
$C_{IN}$	Input Capacitance	(Note 5)		7.5	15		7.5	15	pF
$C_{OUT}$	3-STATE Output Capacitance	(Note 5)		7.5	15		7.5	15	pF
$C_{PD}$	Power Dissipation Capacity	(Note 6)		150			150		pF

**Note 4:** AC Parameters are guaranteed by DC correlated testing.**Note 5:** Capacitance guaranteed by periodic testing.**Note 6:**  $C_{PD}$  determines the no load AC power of any CMOS device. For complete explanation, see Family Characteristics Application Note, AN-90.

### Typical Application



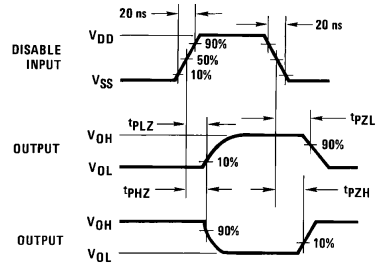
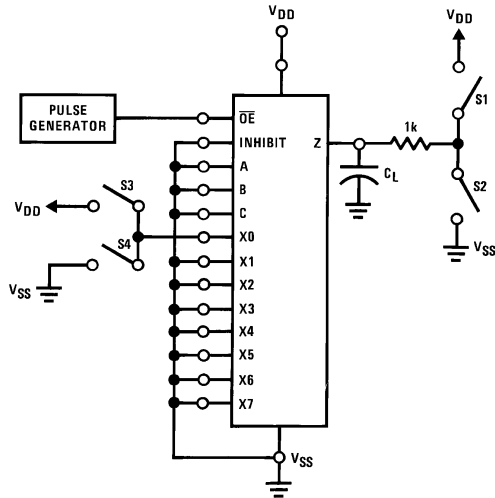
### AC Test Circuit and Switching Time Waveforms



Input Connections for  $t_r$ ,  $t_f$ ,  $t_{PLH}$ ,  $t_{PHL}$

Test	Inhibit	A	X0
1	PG	GND	$V_{DD}$
2	GND	PG	$V_{DD}$
3	GND	GND	PG

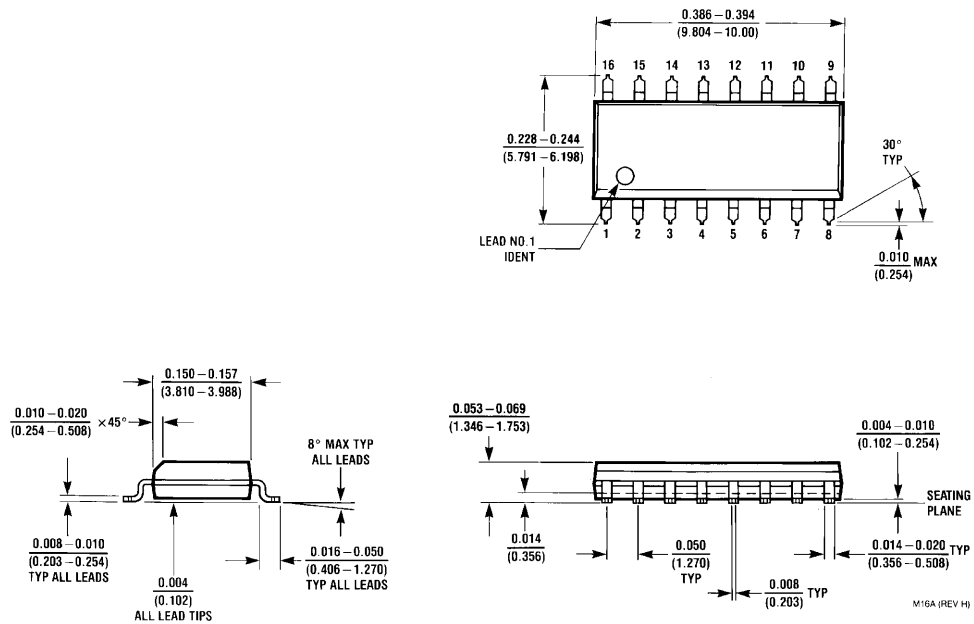
### 3-STATE AC Test Circuit and Switching Time Waveforms



Switch Positions for 3-STATE Test

Test	S1	S2	S3	S4
$t_{PHZ}$	Open	Closed	Closed	Open
$t_{PLZ}$	Closed	Open	Open	Closed
$t_{PZL}$	Closed	Open	Open	Closed
$t_{PZH}$	Open	Closed	Closed	Open

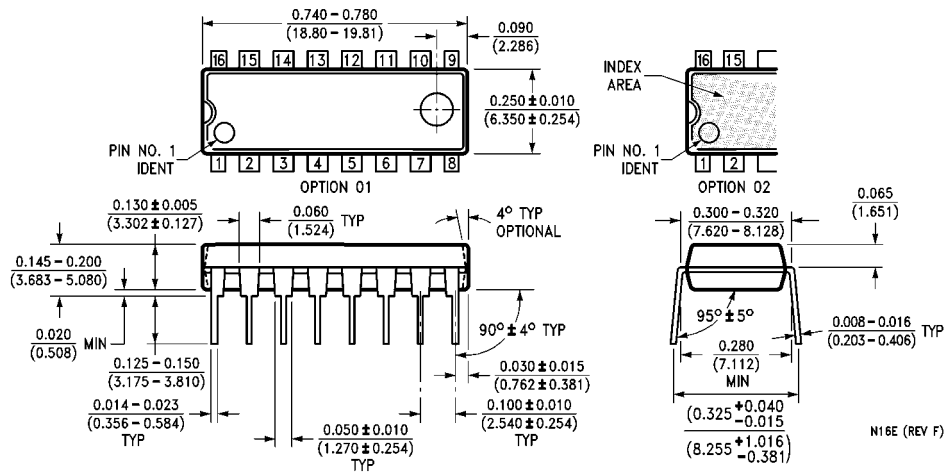
**Physical Dimensions** inches (millimeters) unless otherwise noted



**16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Wide  
Package Number M16A**

M16A (REV H)

**Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)



**16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide Package Number N16E**

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