

SANYO

No.2918A

LC7991**Constant-Speed DC Motor Controller****Overview**

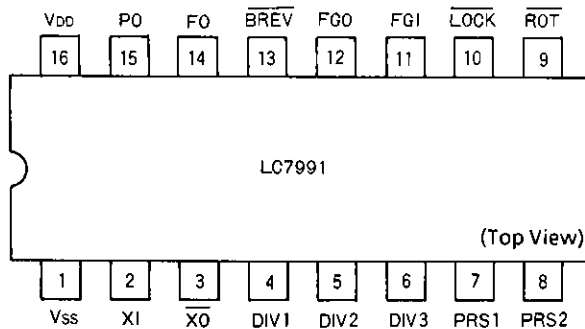
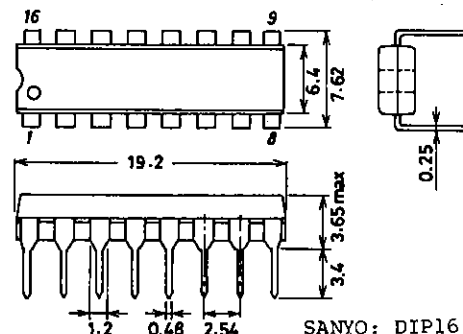
The Sanyo LC7991 is a PLL-type speed controller for constant-speed DC motors. It incorporates a crystal oscillator to provide highly-accurate speed control. Internal frequency dividers support a wide range of motor speeds from low-speed gear motors to high-speed polygon mirror motors. Integrated DACs and a phase comparator allow implementation of a DC motor control system with a minimum of external components.

Applications for the LC7991 include drum, paper feed and scanner motors for plain paper copiers, laser facsimile equipment, laser printers, as well as motors for floppy, hard and optical disk drives.

The LC7991 operates from a single 5V supply, and is available in 16-pin plastic DIPs.

Features

- Wide 200 to 2500Hz operating frequency range (FGI input)
- Low-impedance phase and frequency control outputs
- Speed lock indicator output directly drives an external LED.
- TTL-compatible motor frequency sensor and run/stop control inputs
- CMOS process
- Single 5V supply

Pin Assignment**Package Dimensions 3006B-D16IC**
(unit: mm)

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Absolute Maximum Ratings at Ta = 25°C, VCC = 0V

Parameter	Symbol	Value	unit
Maximum Supply Voltage	V _{DD} max	-0.3 to +7.0	V
Input Voltage	V _{IN}	-0.3 to V _{DD} + 0.3	V
Output Voltage	V _{OUT}	-0.3 to V _{DD} + 0.3	V
Output Current	I _{OUT}	±20	mA
Allowable Power Dissipation	Pd max	Ta = -30 to +75°C	300 mW
Operating Temperature	T _{opr}	-30 to +75	°C
Storage Temperature	T _{stg}	-55 to +125	°C

Allowable Operating Conditions at Ta = -30 to +75°C, VSS = 0V

Parameter	Symbol	min	typ	max	unit
Supply Voltage	V _{DD}	4.5	5	5.5	V
Input Voltage	V _{IN}	0		V _{DD}	V
Output Voltage	V _{OUT}	0		V _{DD}	V

Electrical Characteristics at Ta = 25°C, VDD = 5V ± 10%, VSS = 0V

Parameter	Symbol	min	typ	max	unit
Input 'H'-Level Voltage	V _{IH}	0.7V _{DD}		V _{DD}	V
Input 'L'-Level Voltage	V _{IL}	0	0.3V _{DD}		V
Input 'H'-Level Current	I _{IH}			1	μA
Input 'L'-Level Current	I _{IL}	-1			μA
Input 'H'-Level Current	I _{IH}			1	μA
Input 'L'-Level Current	I _{IL}		-500		μA
Output 'H'-Level Current	I _{OH}			-2	mA
Output 'L'-Level Current	I _{OL}	2			mA
Maximum Non-Linearity (DA Converter)	-		+1	+3	LSB
Output Resistance	R _O		-2	-6	LSB
Current Dissipation	I _{DD}			1000	Ω
				20	mA

AC Characteristics at Ta = 25°C, VDD = 5V ± 10%, VSS = 0V

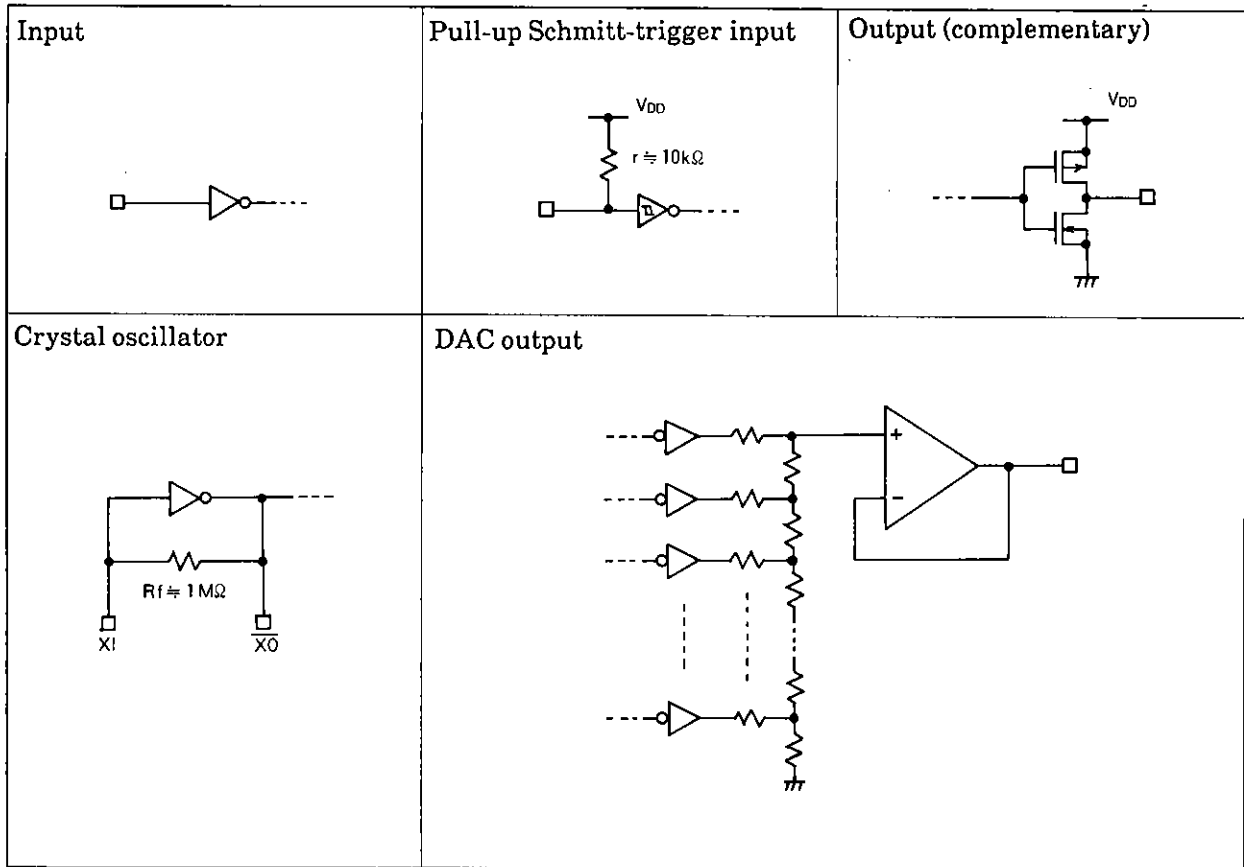
Parameter	Symbol	min	typ	max	unit
Input Frequency	f _{XI}	0.1		10.5	MHz
	f _{FG}			50	kHz
FG Lock Frequency	f _{FG LOCK}	200		2500	Hz
	f _{FG LOCK}	400		5000	Hz

Pin Descriptions

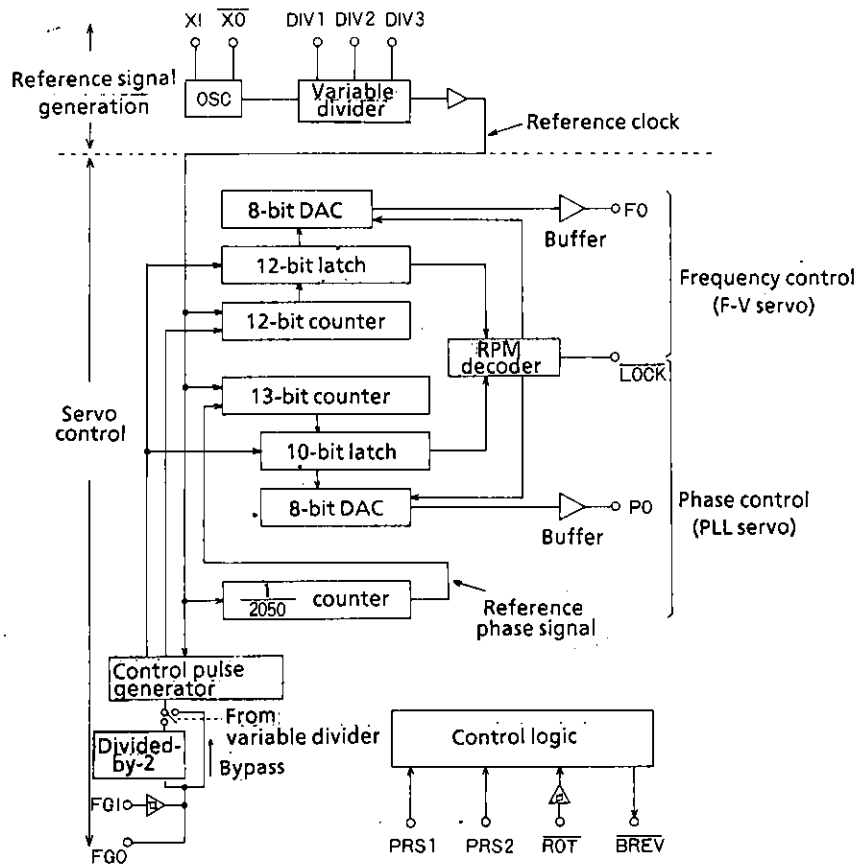
Pin No.	Pin Name	Description	Input/Output
1	V _{SS}	Ground (0V)	-
2	XI	Crystal oscillator	OSC circuit
3	XO		
4	DIV1		
5	DIV2	Variable frequency divider ratio select (FG divider on/off)	Input
6	DIV3		
7	PRS1	Phase comparison range select	Input
8	PRS2		
9	ROT	Rotate/halt control H : halt L : rotate	Pull-up · Schmitt input
10	LOCK	Lock output. LOW during Lock. Can directly drive an external LED.	Output
11	FGI	Motor sensor FG input	Pull-up · Schmitt input
12	FGO	FG shaped output	Output
13	BREV	Brake timing output, LOW during braking.	Output
14	FO	Frequency control output, buffered by internal op-amp	DAC output
15	PO	Phase control output, buffered by internal op-amp	
16	V _{DD}	Positive power supply (5V)	-

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Pin Internal Circuits



Block Diagram



Functional Descriptions

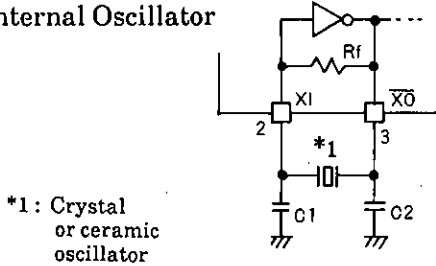
1. Reference Signal Generation

(1) Reference oscillator

The internal oscillator is used by connecting a crystal or a ceramic oscillator between the XI and \overline{XO} pins, and load capacitors to both XI and \overline{XO} , as shown in Fig. 1.

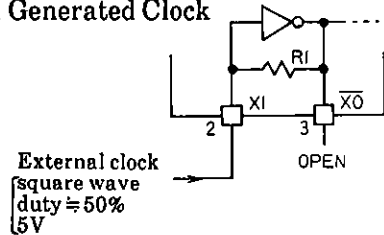
Alternatively, an externally generated clock may be used by leaving \overline{XO} open, and applying the clock to the XI pin, as shown in Fig.2. The clock signal should be 5V in amplitude, with a duty cycle of approximately 50%.

Fig. 1 Internal Oscillator



*1: Crystal or ceramic oscillator

Fig. 2 External Generated Clock



(2) Variable divider and FG divider

The LC7991 incorporates both a five-range selectable divider and a by-passable divide-by-2 circuit for FGI input. These dividers both increase motor speed lock range and simplify selection of a motor speed sensor encoder and oscillator crystal. The division ratio is selected by the DIV1 to DIV3 inputs, as shown in Table 1 below.

Table 1. Divider Control

Control Input			Division Ratio (DIV)	FG Divider
DIV3	DIV2	DIV1		
H	H	H	20	OFF
H	H	L	10	OFF
H	L	H	6	OFF
H	L	L	3	OFF
L	H	H	2	OFF
L	H	L	Test mode	
L	L	H	2	ON
L	L	L	Test mode	

H : High level
 L : Low level
 OFF : Bypass
 ON : Divided-by-2

(3) Crystal/clock frequency selection

The required reference clock frequency is determined from the lock frequency $f_{FG Lock}$ and the division ratio DIV.

If the FG divider is bypassed,

$$f_{xtal} = f_{FG Lock} \times DIV \times 2050 \text{ (Hz)}$$

If the FG divider is selected,

$$f_{xtal} = f_{FG Lock} \times DIV \times 1025 \text{ (Hz)}$$

The available lock frequencies for different clock frequencies are shown below in Table 2. Readily available ceramic resonator include the MURATA CSA6.14MT for 500, 1000 and 1500Hz operation, and the MURATA CSA8.20MT for 2000Hz operation.

Table 2. Clock Frequency and Lock Frequency

Division Ratio	FG Divider	Clock Frequency (MHz)					Unit
		2.05	4.1	6.15	8.2	10.25	
20	OFF	50	100	150	200	250	Hz
10		100	200	300	400	500	
6		167	333	500	667	833	
3		333	667	1000	1333	1667	
2		500	1000	1500	2000	2500	
	ON	1000	2000	3000	4000	5000	

2. Servo Controller

The servo controller compares the reference clock and the motor input frequency signal on pin FGI with control motor speed. FGI is a Schmitt-trigger input. The frequency control output FO and the phase control output PO are output via the 8-bit DA converters. The LOCK output indicates that the motor is within the lock range.

(1) Servo action

Servo action is divided into drive, tracking and braking operation. Tracking operation takes place when motor speed is within 6% of the desired speed. FO and PO act to bring the motor into sync. If the motor is underspeed, both FO and PO go HIGH to accelerate the motor. If the motor is overspeed, FO and PO both go LOW to break the motor.

Servo action and the operation of the LOCK, FO and PO outputs for the three modes of operation is summarized in Table 3. The lock frequency $f_{FG Lock}$ is defined as

$$f_{FG Lock} = \frac{f_{Xtal}}{DIV \times 2050} \quad ; \text{FG divider off}$$

$$f_{FG Lock} = \frac{f_{Xtal}}{DIV \times 1025} \quad ; \text{FG divider on}$$

where DIV is the variable divider ratio, and f_{Xtal} is the crystal oscillator or external input clock frequency.

Table 3. Servo Action

FG Input Frequency	Mode	LOCK Output	FO Output	PO Output
Overspeed : $> f_{FG Lock} + 6\%$	Braking	HIGH	LOW	LOW
Tracking range : $f_{FG Lock} \pm 6\%$	Tracking	LOW	Analog frequency output	Analog phase output
Underspeed $< f_{FG Lock} - 6\%$	Drive	HIGH	HIGH	HIGH

(2) Phase and frequency control

When the motor frequency comes within 6% of the target frequency, FO and PO are switched to the outputs of the internal 8-bit DACs. Each DAC has 256 steps between logic-LOW and logic-HIGH. FO is controlled by the motor speed, and PO by the difference in phase between the internal reference clock and FGI input signal (the motor signal input phase). The output characteristics are shown in Figs. 3 and 4.

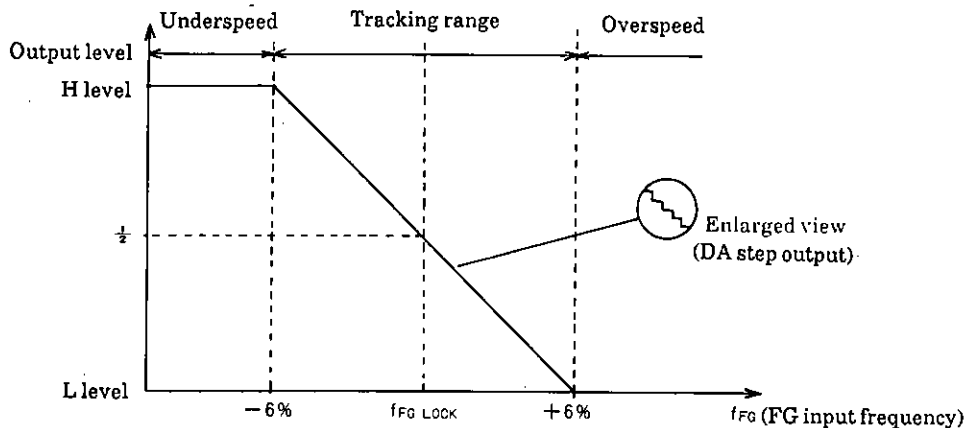


Fig.3 FO Output Characteristic

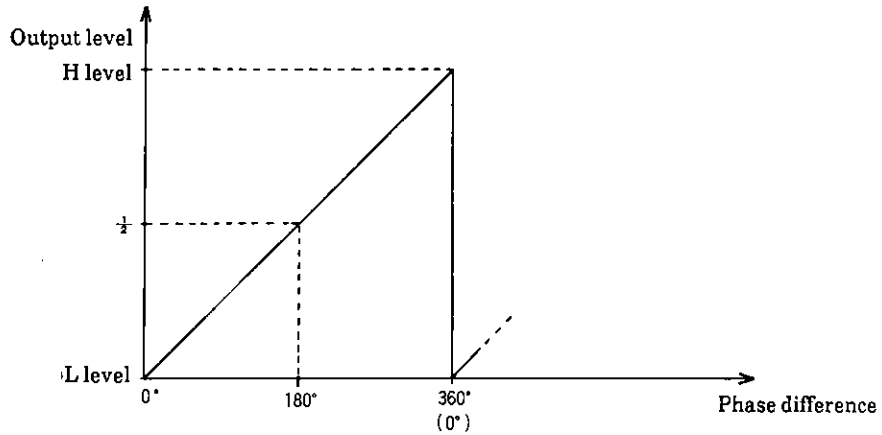


Fig.4 PO Output Characteristic, ×2 Range

3. Rotate Control & Brake Timing Output

The \overline{ROT} active-LOW input may be used to control the motor. When \overline{ROT} is HIGH, both FO and PO are forced LOW.

The motor will take some time to stop following removal of motor drive. The \overline{BREV} output provides the timing required to brake the motor by shorting the windings or applying a reverse voltage. \overline{BREV} goes LOW on the rising edge of \overline{ROT} , and goes HIGH again when the motor frequency drops to 1/8 of lock frequency.

\overline{ROT} and \overline{BREV} timing is shown below in Fig.5.

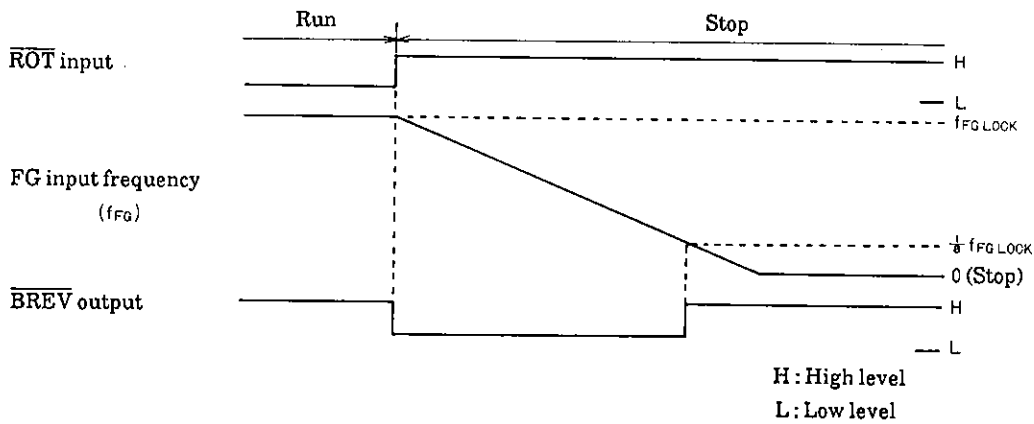


Fig.5 Motor Brake Timing

4. Phase Range Select

The PRS1 and PRS2 inputs select the phase comparator range, as shown in Table 4. The 6π and 14π ranges have a hysteresis region beyond the normal 2π phase comparison region, as shown in Fig.6.

Table 4. Phase Range Selection

PRS2	PRS1	Range
L	L	2π
L	H	Test mode
H	L	6π
H	H	14π

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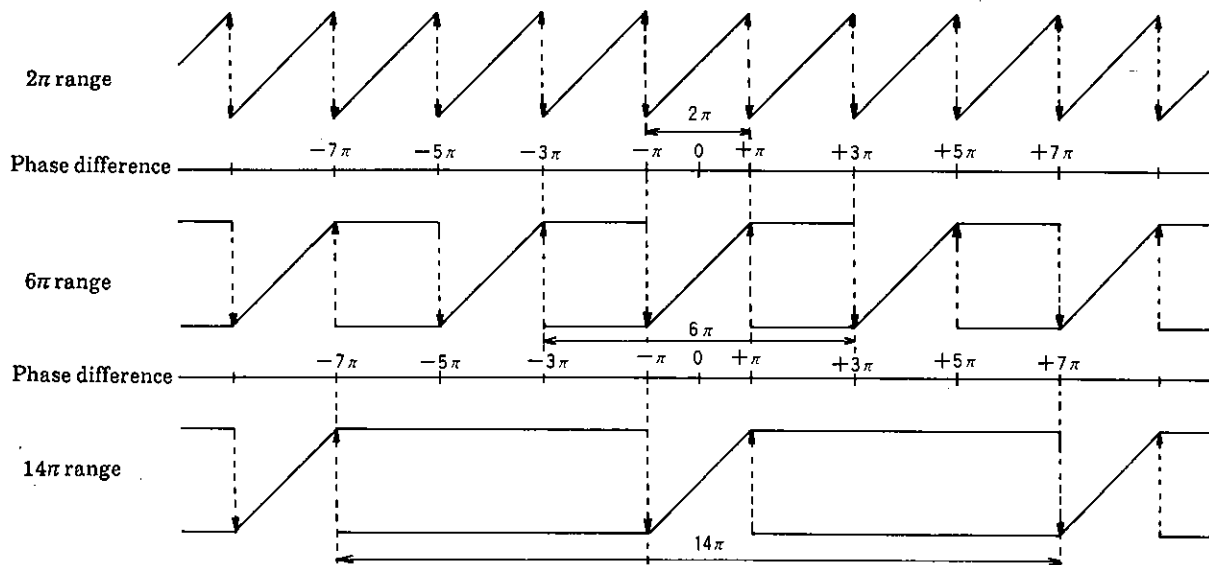
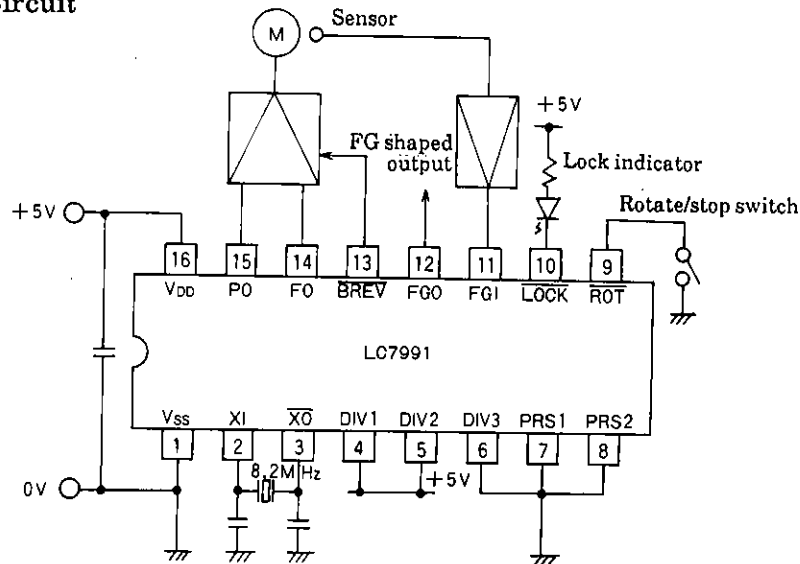


Fig.6 Phase Comparison Ranges

Sample Application Circuit



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