Ordering number : ENN7350

CMOS IC

LC78684E

MP3 Decoder for Compact Disc Players

Overview

The LC78684E integrates, on a single chip, CD-ROM signal-processing functions, MP3 signal-processing functions, and CD-DA shockproof signal-processing functions. The LC78684E achieves significant power savings by implementing signal-processing functions using hard-wired structures.

A CD player that supports playback of MPEG audio (MP3) recorded on CD media as well as CD-DA shockproof playback can be implemented by combining this IC with a CD DSP, DRAM, and audio D/A converter, and other circuits.

Features

- MP3 Decoding Functions (MPEG audio standard [ISO/IEC 11172-3] layer 3)
  - Decodes to a digital audio signal MP3 data decoded by the CD-ROM decoder and outputs that audio signal.
  - Supports all bit rates, including variable bit rate operation.
  - Supports the following sampling rates.
    MPEG1 (Fs = 32 K, 44.1 K, 48 K)
    MPEG2 (Fs = 16 K, 22.05 K, 24 K)
    MPEG2.5 (Fs = 8 K, 11.025 K, 12 K)
  - Can read out the MPEG header and ancillary data.
  - Automatically mutes the signal on CRC errors using an MP3 CRC check function.
  - External MPEG serial data input function supports memory card playback.
- CD-ROM Decoding Functions
  - Supports CD-ROM modes 1 and 2 (forms 1 and 2)
  - Faithfully reproduces data stored on CD-ROM discs using CD-ROM error correction functions.
  - Header and sector management
  - Supports playback speeds up to 4×.
  - In addition to data buffering also supports C2 error flag buffering.
  - Provides external serial output of decoded CD-ROM data.
- CD-DA Playback Functions (Shockproof support)
  - Shockproof operation for about 180 seconds (compressed mode) when 64M DRAM is used.
  - Shockproof function supports compressed, uncompressed, and data through modes.
  - VCEC (variable speed) supports up to 4×-speed playback.
- Audio Signal Processing
  - Serial audio signal output using LRCK, BCK, and DATA signals.
    (I²S format, either 16-bit or 20-bit precision PCM output, data-slot supports 16-bit, 24-bit, and 32-bit modes)
  - Digital bass boost function (4 modes), attenuator function, and muting (–∞, –12 dB)
  - Provides a base clock (384 fs) output pin for use with external digital filters and D/A converters.
- DRAM Interface
  - Supports the use of from 1M to 64M of external DRAM (EDO, 2CAS, 16-bit data bus memory)
  - Supports allocation of a user area in DRAM during CD-ROM (MP3) playback.

Continued on next page.

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Continued from preceding page.

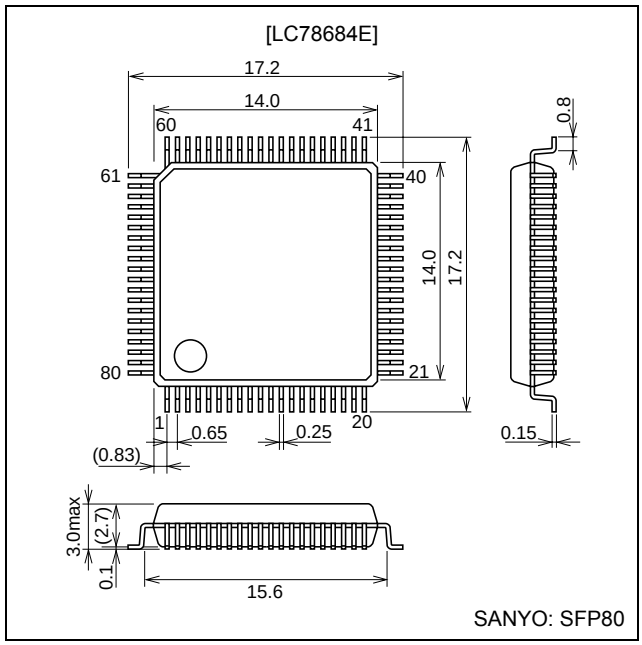
- Package and Power Supply Voltage Specifications
  – Package: Sanyo QFP80 (14 × 14) (unit: mm)
  – Supply voltage
    Internal power supply: 1.8 V (typical)
    I/O power supply: 3.3 V (typical)
    Analog system power supply: 3.3 V (typical)

MPEG Layer3 audio coding technology licensed from Fraunhofer IIS and THOMSON multimedia

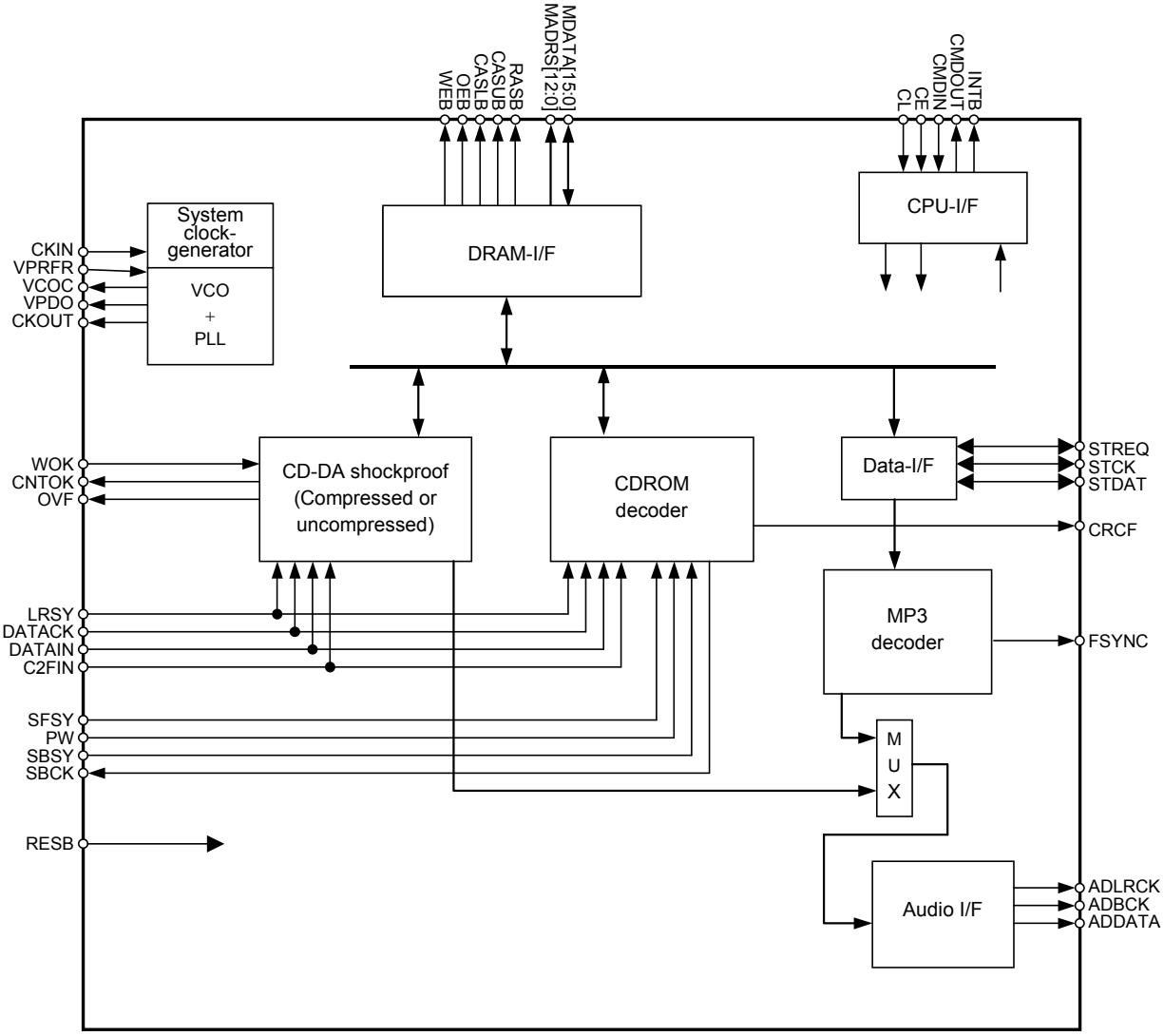
Package Dimensions

Unit: mm

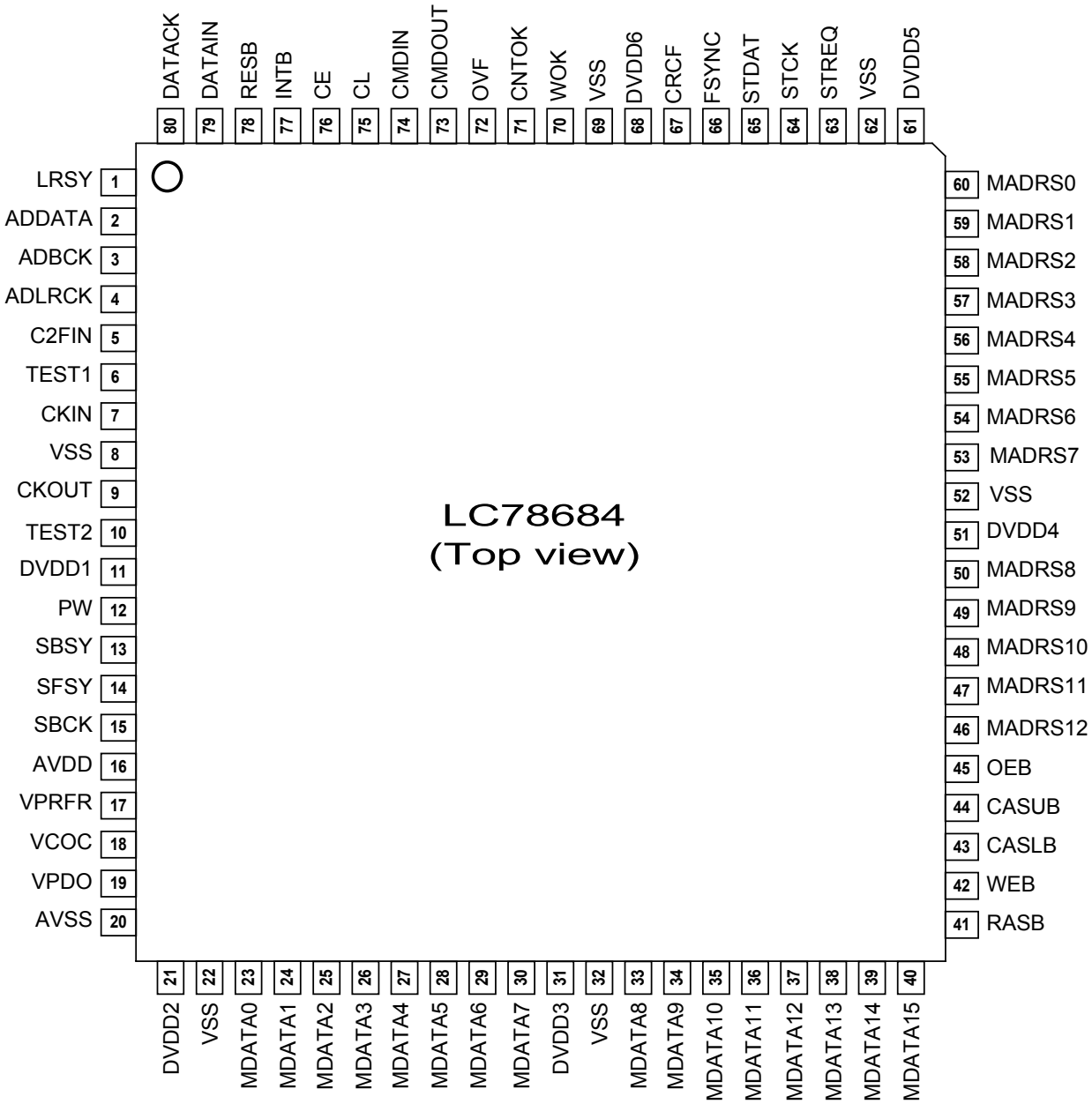
3255-QFP80 (14 × 14)



Block Diagram



Pin Assignment



Pin Functions

Absolute Maximum Ratings at V_{SS} = 0 V, AV_{SS} = 0 V

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V_{DD} max		−0.3 to V_{SS} + 4.0	V
Input voltage	V_{IN}		−0.3 to V_{DD}1 + 0.3	V
Output voltage	V_{OUT}		−0.3 to V_{DD}1 + 0.3	V
Allowable power dissipation	Pdmax		400	mW
Operating temperature	Topr		−30 to +75	°C
Storage temperature	Tstg		−40 to +125	°C

Allowable Operating Ranges at Ta = –30 to +75°C, V_{SS} = 0 V, AV_{SS} = 0V

Parameter	Symbol	Pin name	Conditions	Ratings			Unit
				min	typ	max	
Supply voltage	V_{DD}1	DV_{DD}1, DV_{DD}3, DV_{DD}4, DV_{DD}6, AV_{DD}		3.0	3.3	3.6	V
	V_{DD}2	DV_{DD}2, DV_{DD}5		1.62	1.8	1.98	V
High-level input voltage	V_{IH}	MDATA0 to 15, LRSY, DATAIN, DATACK, C2FIN, PW, SBSY, SFSY, STREQ, STCK, STDAT, WOK, CKIN, CE, CL, CMDIN, RESB		0.8 V_{DD}1		V_{DD}1	V
Low-level input voltage	V_{IL}	MDATA0 to 15, LRSY, DATAIN, DATACK, C2FIN, PW, SBSY, SFSY, STREQ, STCK, STDAT, WOK, CKIN, CE, CL, CMDIN, RESB, TEST1, TEST2		0		0.2 V_{DD}1	V
Operating frequency range	Fop	CKIN			16.9344		MHz

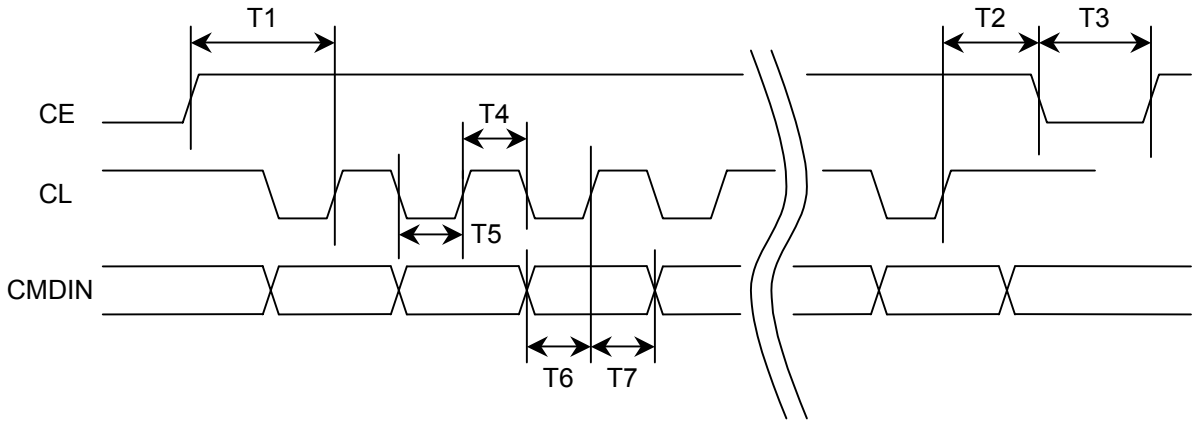
Electrical Characteristics at Ta = –30 to + 75°C, $V_{DD}1$ = 3.0V to 3.6 V, $V_{DD}2$ = 1.62 V to 1.98 V, V_{SS} = 0 V, AV_{SS} = 0 V

Parameter	Symbol	Pin name	Conditions	Ratings			Unit
				min	typ	max	
Current drain	I_{DD} (1)	$DV_{DD}1$, $DV_{DD}3$, $DV_{DD}4$, $DV_{DD}6$, AV_{DD}	$V_{DD}1$ = 3.0 to 3.6 V		10.0	20.0	mA
	I_{DD} (2)	$DV_{DD}2$, $DV_{DD}5$	$V_{DD}2$ = 1.62 to 1.98 V		4.5	10.0	mA
High-level input current	I_{IH}	MDATA0 to 15, LRSY, DATAIN, DATACK, C2FIN, PW, SBSY, SFSY, STREQ, STCK, STDAT, WOK, CKIN, CE, CL, CMDIN, RESB	$V_{IN} = V_{DD}1$			10	μA
Low-level input current	I_{IL}	MDATA0 to 15, LRSY, DATAIN, DATACK, C2FIN, PW, SBSY, SFSY, STREQ, STCK, STDAT, WOK, CKIN, CE, CL, CMDIN, RESB, TEST1, TES2	V_{IN} = 0 V	–10			μA
High-level output voltage	V_{OH} (1)	MDATA0 to 15, STREQ, STCK, STDAT, MADRS0 to 12, RASB, CASUB, CASLB, OEB, WEB SBCK, ADDATA, ADLRCK, ADBCK, INTB, FSYNC, CRCF, CNTOK, OVF	I_{OH} = –2 mA	$V_{DD}1$ –0.6			V
	V_{OH} (2)	CKOUT	I_{OH} = –4 mA	$V_{DD}1$–0.6			V
	V_{OH} (3)	VPDO	I_{OH} = –0.2 mA	$V_{DD}1$–0.6			•
Low-level output voltage	V_{OL} (1)	MDATA0 to 15 STREQ, STCK, STDAT, MADRS0 to 12, RASB, CASUB, CASLB, OEB, WEB SBCK, ADDATA, ADLRCK, ADBCK, INTB, FSYNC, CRCF, CNTOK, OVF, CMDOUT	I_{OL} = 2 mA			0.4	V
	V_{OL} (2)	CKOUT	I_{OL} = 4 mA			0.4	V
	V_{OL} (3)	VPDO	I_{OL} = 0.2 mA			0.4	•
Output off leakage current	I_{OFF} (1)	MDATA0 to 15, STREQ, STCK, STDAT, CMDOUT	$V_{OUT} = V_{DD}1$			10	μA
	I_{OFF} (2)	MDATA0 to 15, STREQ, STCK, STDAT, CMDOUT	V_{OUT} = 0 V	–10			μA

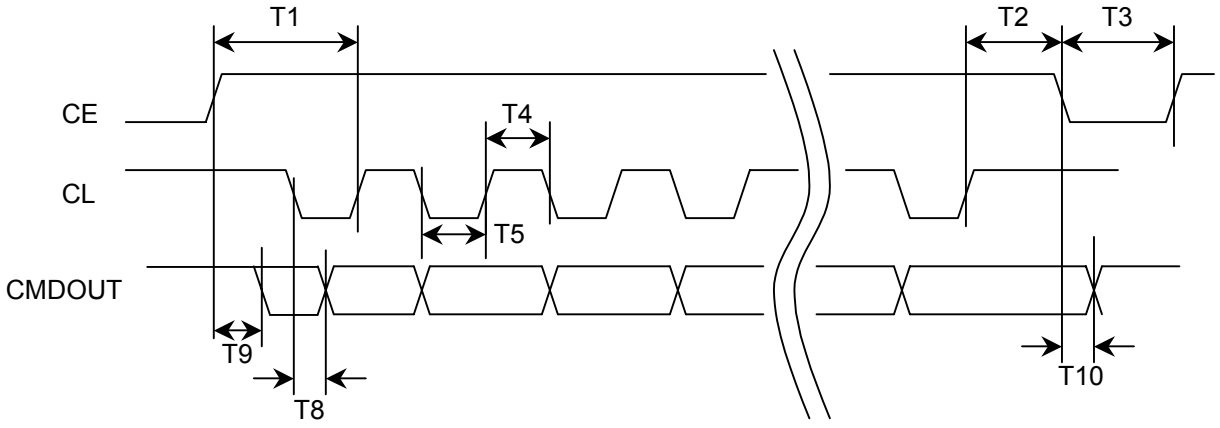
Microcontroller Interface

Microcontroller Interface Timing

Write Cycle



Read Cycle



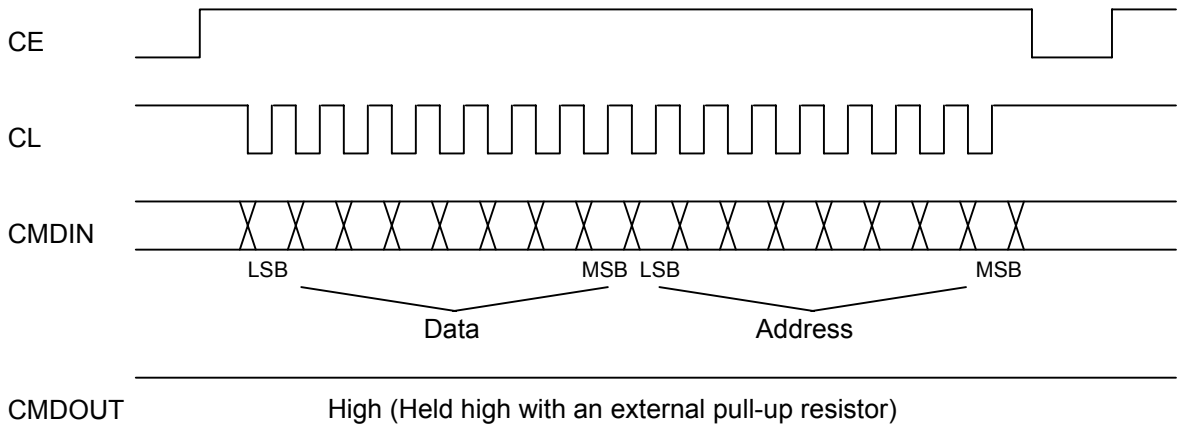
Parameter	Symbol	Ratings			Unit
		min	typ	max	
CE/CL setup time	T1	500			ns
CE/CL hold time	T2	250			ns
Command wait time	T3	1000			ns
CL H-level pulse width	T4	250			ns
CL L-level pulse width	T5	250			ns
Data/CL setup time	T6	150			ns
Data/CL hold time	T7	150			ns
Data-read access time ∗	T8	0		240	ns
Data-read turn-on time ∗	T9	0		150	ns
Data-read turn-off time ∗	T10	0		240	ns

∗: Pull-up resistor = 1 KΩ, Output load = 30 pF

Command Input/Data Output Interface

Input commands (i.e. write data to the LC78684E) in the order data first and then address. The data and address are LSB first. Output data is output (i.e. read data from the LC78684E) by first issuing a read mode setup command and then performing read access operations.

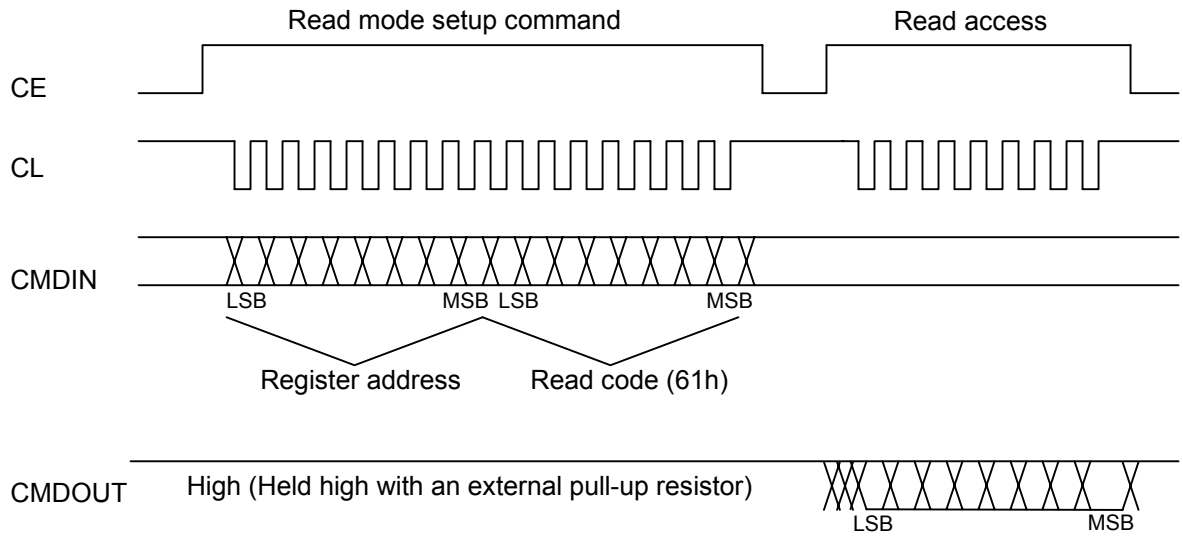
Data write



Data read

Data is read by first writing the register address to be read to location $61h and then setting up read mode by setting CE low temporarily. When CE is set high again, and the CL signal is issued, the contents of the specified register are output from CMDOUT, LSB first.

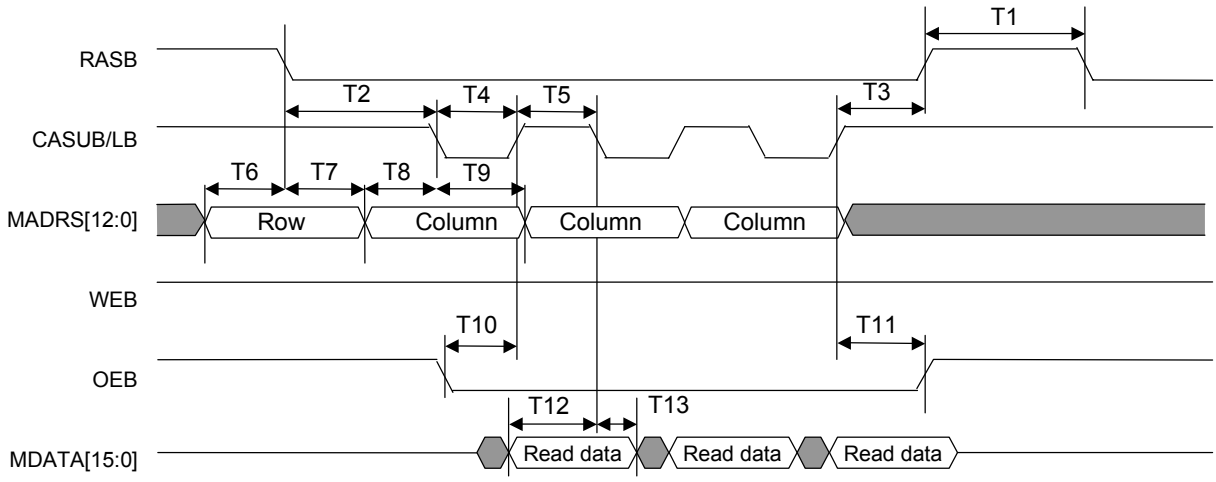
The microcontroller must perform a read access if it sets up read mode.



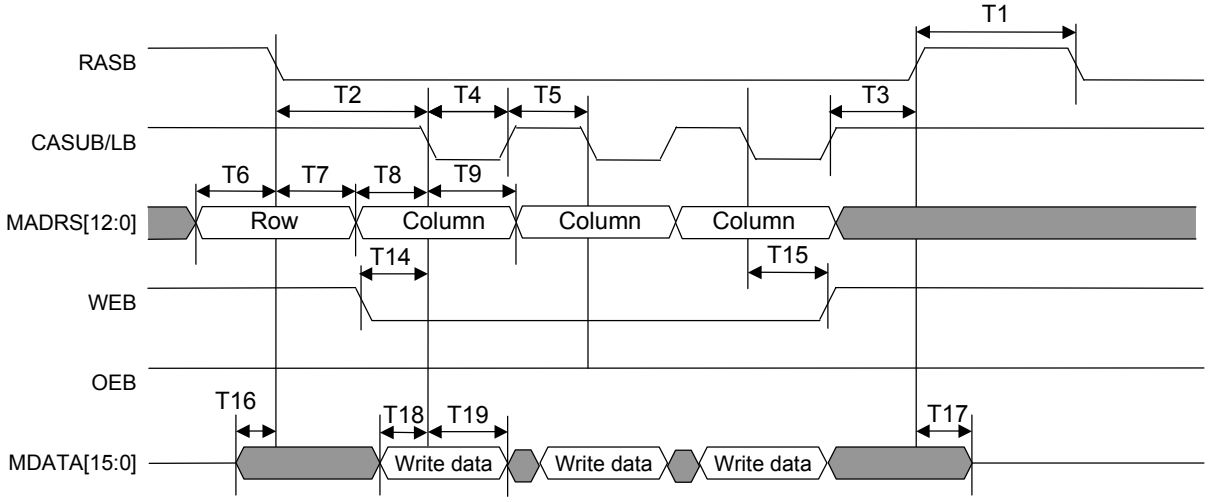
Memory Interface

Memory Interface Timing

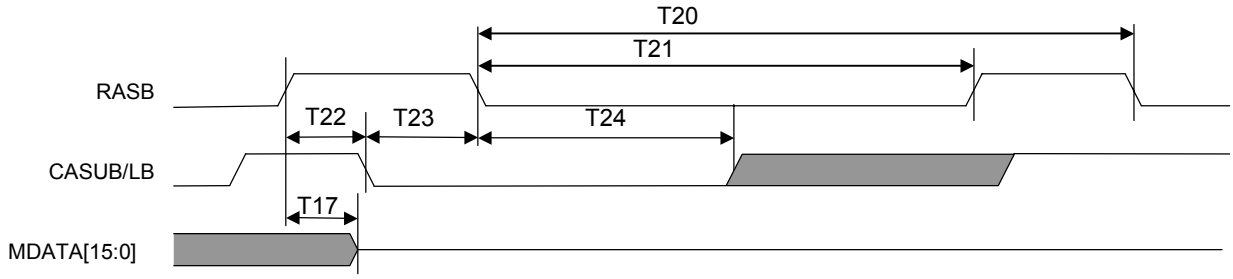
Read Cycle



Write Cycle



Refresh Cycle (CAS before RAS)

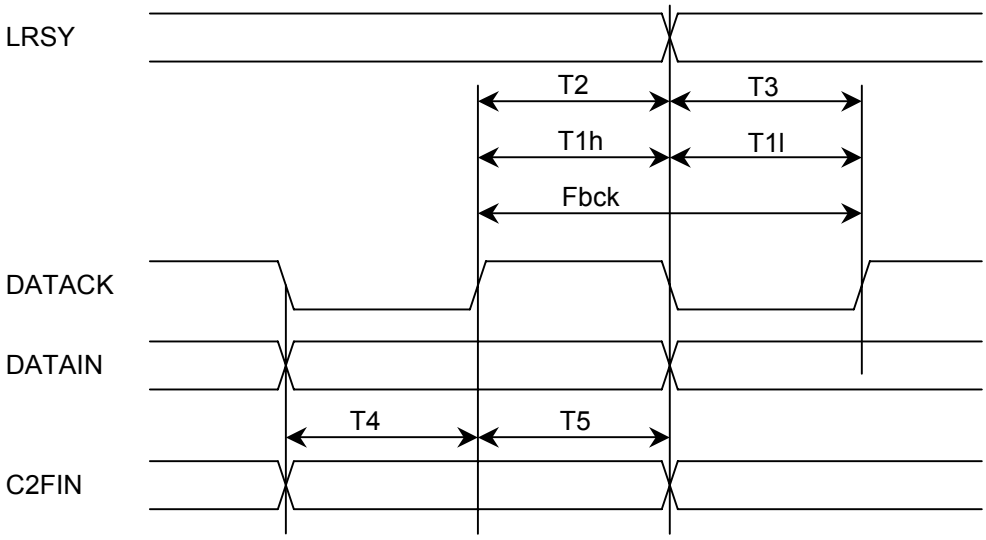


Parameter	Symbol	Ratings			Unit
		min	typ	max	
RASB width high	T1	100			ns
RASB CASB delay	T2	80			ns
CASB RASB delay	T3	40			ns
CASB width low	T4	40			ns
CASB width high	T5	40			ns
Row address setup time	T6	15			ns
Row address hold time	T7	40			ns
Column address setup time	T8	15			ns
Column address hold time	T9	40			ns
OEB ready time	T10	30			ns
OEB hold time	T11	10			ns
Read data setup time	T12	30			ns
Read data hold time	T13	0			ns
WEB ready time	T14	30			ns
WEB hold time	T15	40			ns
Write data turn on time	T16			60	ns
Write data turn off time	T17			80	ns
Write data setup time	T18	15			ns
Write data hold time	T19	40			ns
Refresh cycle	T20	300			ns
RASB low width (refresh)	T21	200			ns
RASB CASB delay (refresh)	T22	50			ns
CASB setup time (refresh)	T23	40			ns
CASB hold time (refresh)	T24	100			ns

∗: These values apply when the frequency of the clock input to the CKIN pin is 16.9344 MHz.

CD DSP Interface

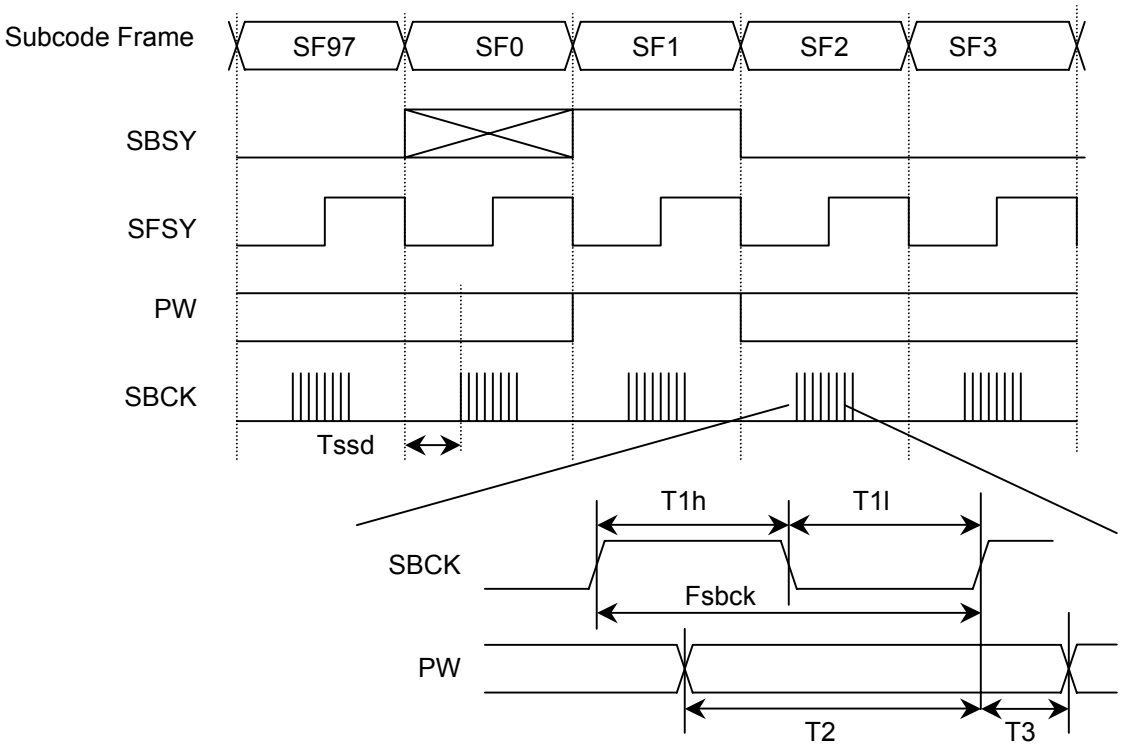
CD DSP Interface Timing



Parameter	Symbol	Ratings			Unit
		min	typ	max	
DATACK frequency	Fbck			14.5	MHz
DATACK H-level pulse width	T1h	30			ns
DATACK L-level pulse width	T1l	30			ns
LRSY setup time	T2	30			ns
LRSY hold time	T3	30			ns
DATA, C2FIN setup time	T4	30			ns
DATA, C2FIN hold time	T5	25			ns

∗: The figure above shows the timings when DATACK rising edge latch is used.
If DATACLK falling edge latch is used, the timings are the same as those for the corresponding setup and hold signal.

Subcode Interface Timing

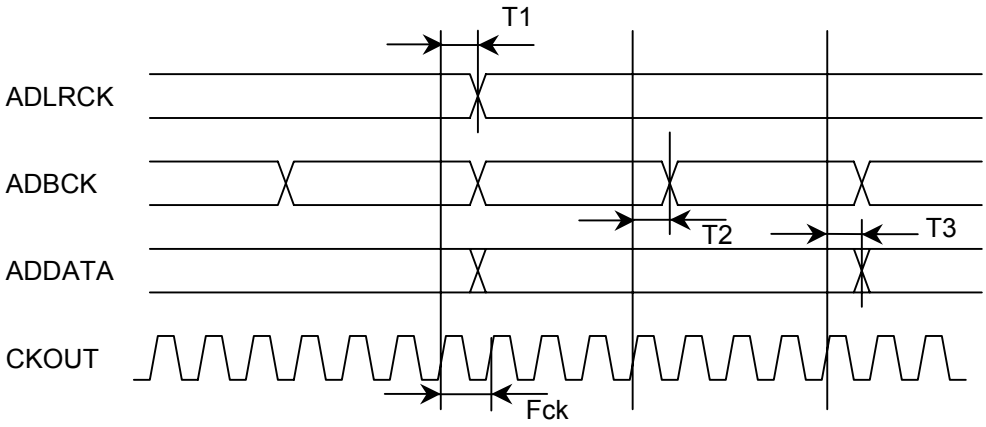


Parameter	Symbol	Ratings			Unit
		min	typ	max	
SFSY – SBCK delay time	Tssd	235		7150	ns
SBCK frequency	Fsbck		1.0584		MHz
SBCK H-level pulse width	T1h	450			ns
SBCK L-level pulse width	T1l	450			ns
PW setup time	T2	50			ns
PW hold time	T3	0			ns

∗: These values apply when the frequency of the clock input to the CKIN pin is 16.9344 MHz.

Audio Output Interface

Audio Output Interface Timing

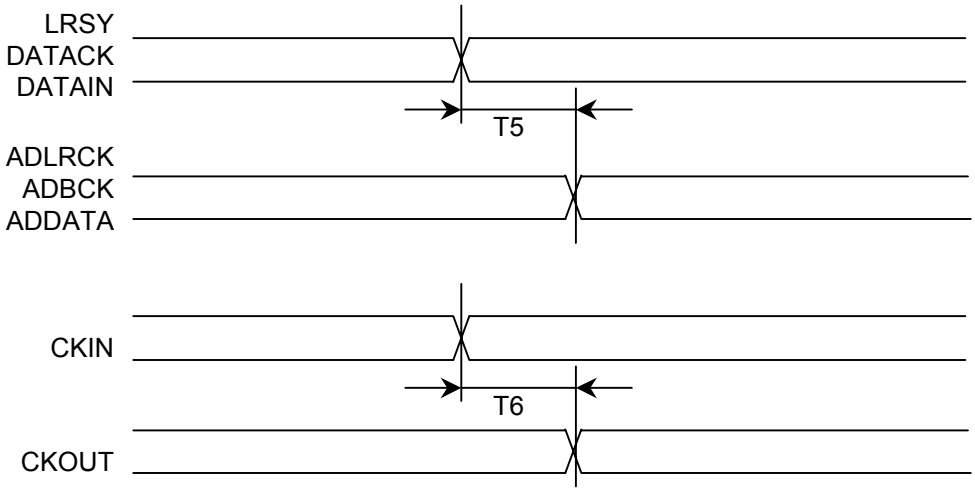


The figure above applies when the 48-bit slot is used for the audio data output slot.

Parameter	Symbol	Ratings			Unit
		min	typ	max	
CKOUT → ADLRCK delay time	T1	0		35	ns
CKOUT → ADBCK delay time	T2	0		35	ns
CKOUT → ADDATA delay time	T3	0		35	ns
CKOUT frequency ∗	Fck		16.9344		MHz

∗: These values apply during MPEG1 data playback (fs = 44.1 kHz) when the PLL circuit is locked normally.
These values depend on the playback sampling frequency (fs). (CKOUT frequency = fs × 384)

Supplement: Output Timing for Full Through Mode Playback



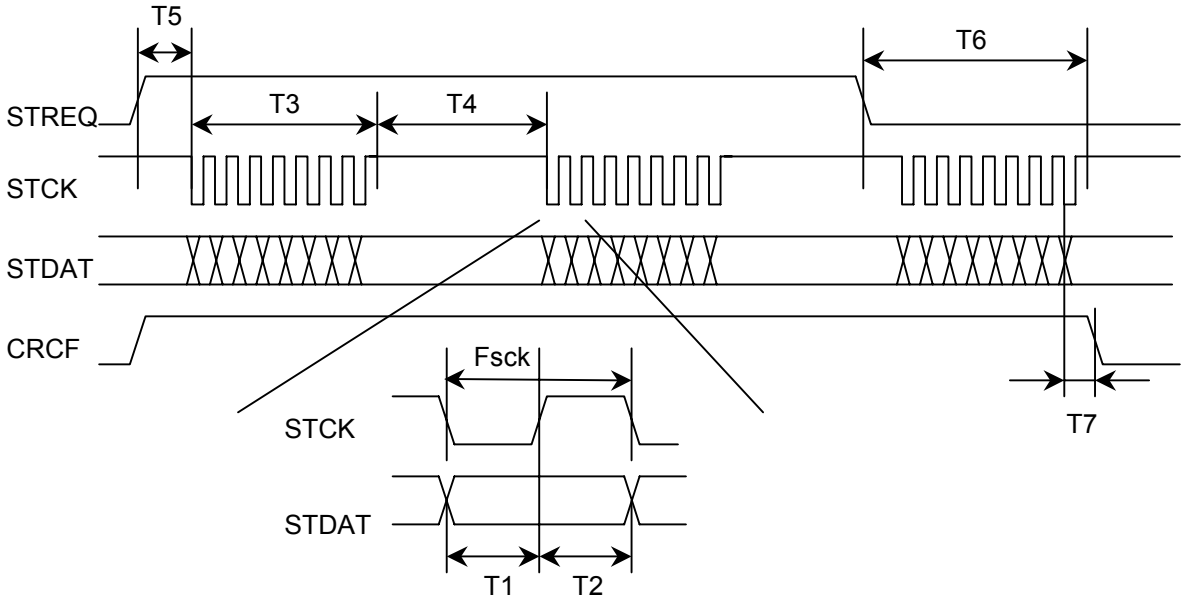
∗: Full through mode is the state where the THROUGH bit (60h: bit 6) is set to 1.

Parameter	Symbol	Ratings			Unit
		min	typ	max	
INPUT → OUTPUT delay time	T5	0		35	ns
CKIN → CKOUT delay time ∗	T6	0		35	ns

∗: These values apply when the signal input to the CKIN pin is directly output from the CKOUT pin.

Serial Data I/O Interface

DRAM Serial Data Output Timing



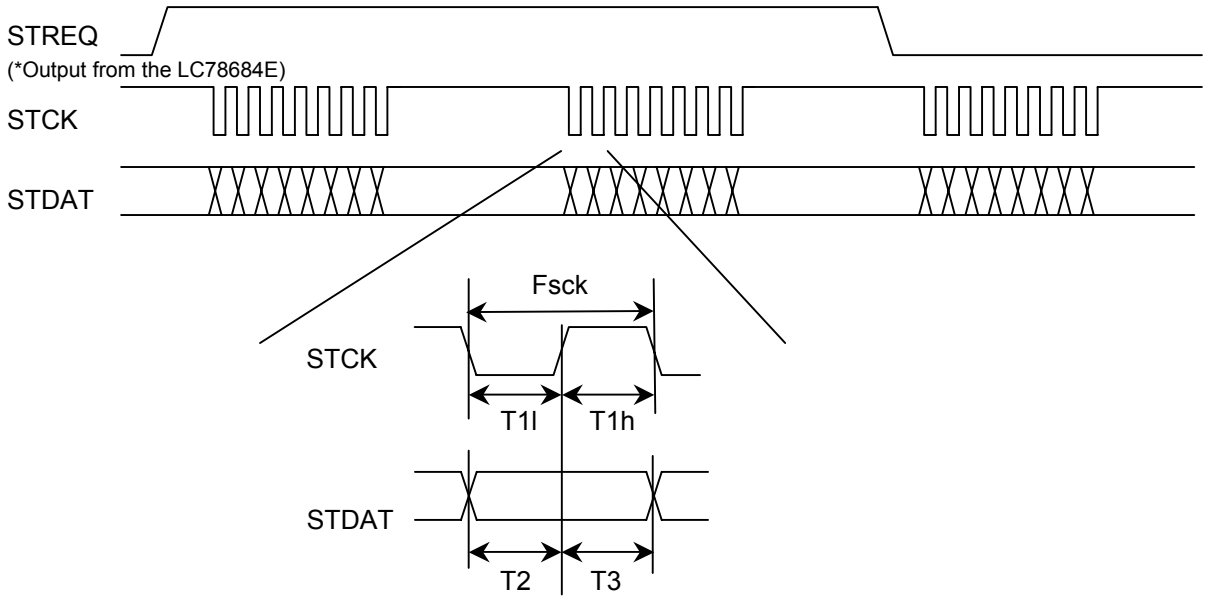
∗: Performing a serial data output operation requires that a command to transfer data from DRAM be issued.
If this command has not been issued, the STCK and STDAT pins will not output the clock and data signals, even if the STREQ goes high.

Parameter	Symbol	Ratings			Unit
		min	typ	max	
Transfer clock frequency	Fsck		4.2336		MHz
STDAT/STCK setup time	T1	30			ns
STDAT/STCK hold time	T2	30			ns
Data (1byte) transfer time	T3		1.89		μs
Data transfer wait time	T4		1.89		μs
Data transfer start time	T5	1.89		15.2	μs
Data transfer stop time	T6	0		15.2	μs
Enable flag turn off time	T7	210	236.2	270	ns

Notes: The typical values shown apply when the frequency of the clock input to the CKIN pin is 16.9344 MHz.

- The fsck clock frequency can also be set to 2.1168 or 1.0584 MHz (typical). The values of T3 to T7 will be, in that case, 2 or 4 times the values shown.
- When the STREQ pin is in input mode, the WOK, OVF, and CNTOK pins can be used instead of the STREQ, STCK, and SDAT pins. The timing specifications in this case are the same as those shown above.

MP3 Serial Data Input Timing



∗ Performing a serial data input operation requires that a serial input command be issued.
If this command has not been issued, the MP3 decoder will not operate, even if clock and data signals are applied to the STCK and STDAT pins.

Parameter	Symbol	Ratings			Unit
		min	typ	max	
Transfer clock frequency ∗	Fsck			9.216	MHz
STCK H-level pulse width	T1h	45			ns
STCK L-level pulse width	T1l	45			ns
STDAT/STCK setup time	T2	30			ns
STDAT/STCK hold time	T3	30			ns

∗: The table below lists the maximum frequencies for the transfer clock during serial input operations.

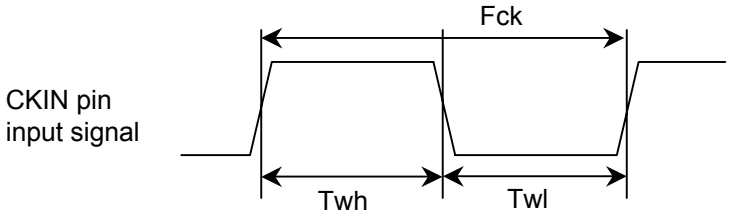
MODE	Fs (KHz)	Maximum serial transfer clock frequency (MHz) ∗
MPEG1	48	9.216
	44.1	8.4672
	32	6.144
MPEG2 (MPEG2.5)	24 (12)	4.608
	22.05 (11.025)	4.2336
	16 (8)	3.072

The transfer clock rate must be set to a speed less than or equal to the speed shown in the table so that the MP3 decoding processing will complete in time.

Note that the table above applies when MP3DSET (register 41h, bit 0) is set to 1 (high-speed transfer mode).
The timings shown below apply when MP3DSET is set to 0 (low-speed transfer mode).

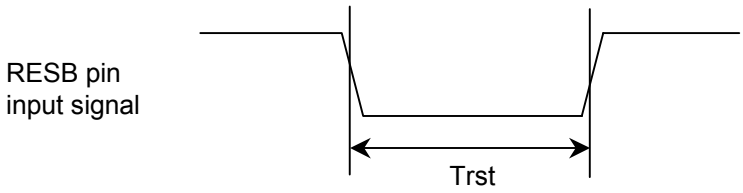
Parameter	Symbol	Ratings			Unit
		min	typ	max	
Transfer clock frequency	Fsck			3.072	MHz
STCK H-level pulse width	T1h	150			ns
STCK L-level pulse width	T1l	150			ns
STDAT / STCK setup time	T2	125			ns
STDAT / STCK hold time	T3	125			ns

System Clock Input



Parameter	Symbol	Ratings			Unit
		min	typ	max	
CKIN Input frequency	Fck		16.9344	18.0	MHz
CKIN H-Level pulse width	Twh	20			ns
CKIN L-Level pulse width	Twl	20			ns

System Reset Input



Parameter	Symbol	Ratings			Unit
		min	typ	max	
System reset pulse width	Trst	1			μs

∗: A system reset must be performed immediately after power is first applied.
Design the system so that no noise appears on the reset line.

Pin Functions

Pin No.	Pin Name	I/O	Block	Function
1	LRSY	I	CD IF	CD left/right clock input
2	ADDATA	O	Audio interface	Audio data output
3	ADBCK	O		Audio bit clock output
4	ADLRCK	O		Audio left/right clock output
5	C2FIN	I	CD IF	CD C2 error flag input
6	TEST1	I	Test	Test input 1 (This pin must be connected to ground during normal operation.)
7	CKIN	I	CLOCK	System clock input (16.9344 MHz)
8	VSS	–	Power supply	Ground
9	CKOUT	O	CLOCK	External digital filter and D/A converter clock (384 fs) output
10	TEST2	I	Test	Test input 2 (This pin must be connected to ground during normal operation.)
11	$DV_{DD}1$	–	Power supply	Digital I/O system power supply
12	PW	I	Subcode interface	CD subcode data serial input
13	SBSY	I		CD subcode block sync signal input
14	SFSY	I		CD subcode frame sync signal input
15	SBCK	O		CD subcode transfer serial clock output
16	AV_{DD}	–	Power supply	Analog system (PLL) power supply
17	VPRFR	–	PLL	VCO oscillator range setting
18	VCOC	I		VCO control voltage input
19	VPDO	O		VCO charge pump output
20	AVSS	–	Power supply	Analog system ground
21	$DV_{DD}2$	–		Internal logic system power supply
22	VSS	–		GND
23	MDATA0	I/O	Memory interface	DRAM data bus 0
24	MDATA1	I/O		DRAM data bus 1
25	MDATA2	I/O		DRAM data bus 2
26	MDATA3	I/O		DRAM data bus 3
27	MDATA4	I/O		DRAM data bus 4
28	MDATA5	I/O		DRAM data bus 5
29	MDATA6	I/O		DRAM data bus 6
30	MDATA7	I/O		DRAM data bus 7
31	$DV_{DD}3$	–	Power supply	Digital I/O system power supply
32	VSS	–		GND
33	MDATA8	I/O	Memory interface	DRAM data bus 8
34	MDATA9	I/O		DRAM data bus 9
35	MDATA10	I/O		DRAM data bus 10
36	MDATA11	I/O		DRAM data bus 11
37	MDATA12	I/O		DRAM data bus 12
38	MDATA13	I/O		DRAM data bus 13
39	MDATA14	I/O		DRAM data bus 14
40	MDATA15	I/O		DRAM data bus 15
41	RASB	O		RAS output (active low)
42	WEB	O		WE output (active low)
43	CASLB	O		CAS output (lower byte, active low)
44	CASUB	O		CAS output (upper byte, active low)
45	OEB	O		OE output (active low)
46	MADRS12	O		DRAM address output 12
47	MADRS11	O		DRAM address output 11
48	MADRS10	O		DRAM address output 10
49	MADRS9	O		DRAM address output 9
50	MADRS8	O		DRAM address output 8

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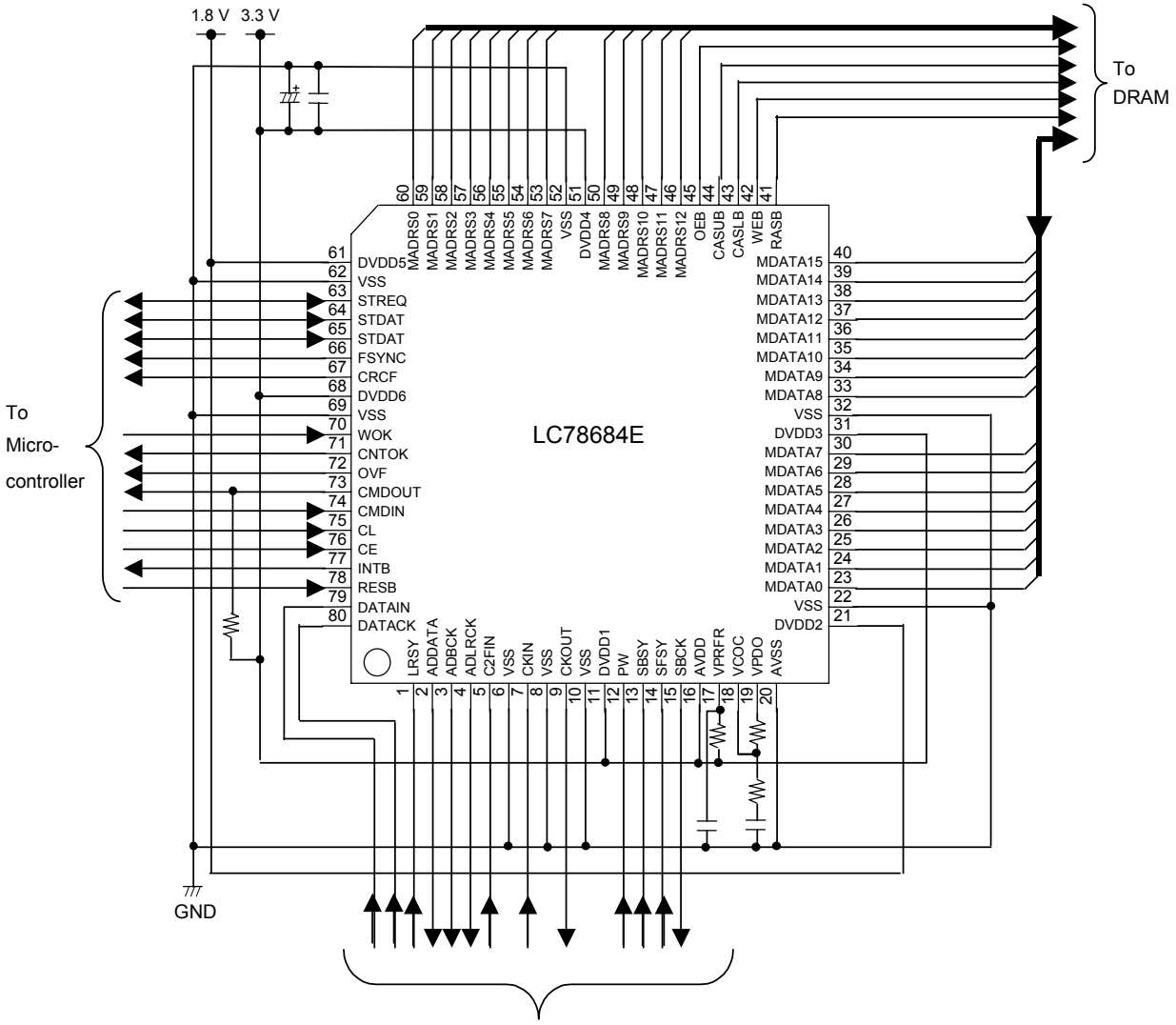
Pin No.	Pin Name	I/O	Block	Function
51	$DV_{DD}4$	–	Power supply	Digital I/O system power supply
52	V_{SS}	–		Ground
53	MADRS7	O	Memory interface	DRAM address output 7
54	MADRS6	O		DRAM address output 6
55	MADRS5	O		DRAM address output 5
56	MADRS4	O		DRAM address output 4
57	MADRS3	O		DRAM address output 3
58	MADRS2	O		DRAM address output 2
59	MADRS1	O		DRAM address output 1
60	MADRS0	O		DRAM address output 0
61	$DV_{DD}5$	–	Power supply	Internal logic system power supply
62	V_{SS}	–		GND
63	STREQ	I/O	MP3 stream I/O	MP3 data request flag output (active high) /DRAM data request flag input (CD-ROM mode, active high)
64	STCK	I/O		MP3 data transfer clock input /DRAM data transfer clock output
65	STDAT	I/O		MP3 serial data input /DRAM serial data output
66	FSYNC	O	MP3-dec	MP3 frame sync signal (active high) /Data continuity point detection complete flag (CD-DA mode, active high)
67	CRCF	O	CD monitor	CRC check result output (CD-ROM data/CD-DA subcode data) /DRAM data output enable signal output (active high)
68	$DV_{DD}6$	–	Power supply	Digital I/O system power supply
69	V_{SS}	–		GND
70	WOK	I	CD-DA shockproof and MP3 I/O	DRAM write enable input (CD-DA mode, active high) /DRAM data request flag input
71	CNTOK	O		Data continuity point detection complete flag (CD-DA mode, active high) /SYNC error monitor flag (MP3 mode, active high)/DRAM serial data output
72	OVF	O		DRAM write interrupt flag (CD-DA mode, active high) /Emphasis output flag (CD-DA and MP3 modes, active high) /DRAM data transfer clock output
73	CMDOUT	O	Microcontroller interface	Serial command data output (n-channel open-drain output)
74	CMDIN	I		Serial command data input
75	CL	I		Serial command clock input
76	CE	I		Command enable input (active high)
77	INTB	O		Interrupt signal output (active low) /DRAM write interrupt flag (CD-DA mode, active high)
78	RESB	I		System reset (active low)
79	DATAIN	I	CD IF	Serial CD data input
80	DATACK	I		CD bit clock input

Notes: 1. Notes on unused pins.
Unused input pins must be connected to the ground level (0 V).
Unused output pins must be left open. Do not connect anything to these pins.
Unused I/O pins may either be connected to the ground level (0 V) or set to output mode and left open.

2. The corresponding power supply levels must be provided to all of the $DV_{DD}1$, $DV_{DD}3$, $DV_{DD}4$, $DV_{DD}6$, and AV_{DD} pins. The corresponding power supply level must also be provided to $DV_{DD}2$ and $DV_{DD}5$. (See the Allowable Operating Ranges specifications for the supply levels.)
3. The TEST1 and TEST2 input pins must be connected to ground (0 V).
4. The I/O pins (MDAT0:15, STREQ, STCK, and STDAT) go to input mode after a reset.
5. After first applying the power supply levels, the RESB pin must be held low for at least 1 μs.
6. A 16.9344 MHz clock signal must be supplied to the CKIN pin by the CD DSP.
The LC78684E does not support the implementation of an oscillator circuit using an oscillator element.

Sample Application Circuit



∗: The CKOUT, ADLRCK, ADBCK, and ADDATA pins must be connected to a CD DSP that supports external D/A converter input.
An external D/A converter is required if the CD DSP does not provide that functionality.

Application Design Notes

While it goes without saying that strictly observing the absolute maximum ratings and allowable operating ranges (recommended operation conditions) stipulated for this IC is necessary to achieve reliability of the overall system, it is also necessary to take adequate care with respect to the mounting conditions and the operating environment, including the ambient temperature and the possibility of electrostatic discharges (ESD). This section presents notes on aspects of design and mounting that require special attention.

Handling Unused Pins

If this IC is operated with unused input pins left open, certain internal circuit operations may become unstable. Unused pins that are mentioned in the IC documentation must be handled as specified. Also, do not allow output pins to come in contact with any circuit lines, including power supply lines, ground lines, or other outputs.

Latchup Prevention

- The voltages stipulated in the IC specifications must be provided to the corresponding power supply pins. When the same voltage is stipulated for multiple pins, those pins all must be connected to the same potential.
- Do not set I/O voltage levels to be either higher than the peripheral 3 V system block voltage, or lower than the ground level. This relationship must also be maintained during the power-on sequence.
- Do not apply overvoltages or abnormal noise to this IC.
- While in general, latchup is prevented by holding unused input pins at either the VDD or VSS potential, input pins to this IC must be handled as described in the pin descriptions.
- Do not short the outputs.

Interface

Incorrect operation may result when different devices are connected if the input VIL/VIH and the output VOH and VOH levels do not match. Level shifters must be inserted between devices with differing supply voltages, such as those often used in dual power supply systems, to prevent destruction of the devices.

Load Capacitance and Output Current

- If a large load capacitance is connected, the resulting effective short of the outputs may continue for an extended period and lead to fusing of lines. Also, larger charge and discharge currents can cause noise, degrade device performance, and cause incorrect operation. The recommended load capacitance ratings must be observed.
- Excessive output sink or source currents can lead to the same problems described in the preceding item. Once the allowable power dissipation rating has been met, the recommended current values must be observed as well.

Notes on Power Application and Reset

- There are several aspects that require care when power is first applied, during a reset, and when the reset state is cleared. Refer to the device specifications and design applications to match the product specifications.
- In this IC, the register contents, pin output states, and pin I/O settings are not guaranteed after power is first applied. Items that are defined by the reset operation or mode setting operations are guaranteed after these operations are performed. After power is first applied to this IC, the application must first perform a reset operation. Pin states and register values that are not defined are subject to change, both due to sample-to-sample variations in the product over the long term, and due to changes in device design from the initial design states.

Thermal Design

- Semiconductor device failure rates are greatly accelerated by inappropriate ambient temperature and power consumption conditions. To assure the highest possible reliability, the thermal design should provide ample margins considering all possible changes in the ambient conditions.

Notes on PWB Pattern Design

- In an ideal design, power supply and ground lines will be provided separately for each system to minimize the influence of shared impedances.
- Power supply and ground lines must be made as wide and as short as possible, and the impedance to high frequencies must be made as low as possible. Decoupling capacitors (consisting of two capacitors: one about 0.01 to 1.0 μF and another about 100 to 220 μF) should be inserted between each power supply pin and ground. Note, however, that if this capacitance is too large, it may result in latchup problems.

Other Notes

If you have any questions or if anything is even slightly unclear, please contact your SANYO sales or technical representative during the design phase. This IC is a special-purpose device for use in CD players, and its specifications differ from those of standard logic ICs and other general-purpose products. Also note that, depending on the application, failsafe measures and/or system level debugging of the total system may be required as well.