

**ITU CO/PABX SLIC with Low Power Standby**

The HC5515 is a subscriber line interface circuit which is interchangeable with Ericsson's PBL3860 for distributed central office applications. Enhancements include immunity to circuit latch-up during hot plug and absence of false signaling in the presence of longitudinal currents.

The HC5515 is fabricated in a High Voltage Dielectrically Isolated (DI) Bipolar Process that eliminates leakage currents and device latch-up problems normally associated with junction isolated ICs. The elimination of the leakage currents results in improved circuit performance for wide temperature extremes. The latch free benefit of the DI process guarantees operation under adverse transient conditions. This process feature makes the HC5515 ideally suited for use in harsh outdoor environments.

**Ordering Information**

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
HC5515CM	0 to 70	28 Ld PLCC	N28.45
HC5515CP	0 to 70	22 Ld PDIP	E22.4
HC5515IM	-40 to 85	28 Ld PLCC	N28.45
HC5515IP	-40 to 85	22 Ld PDIP	E22.4

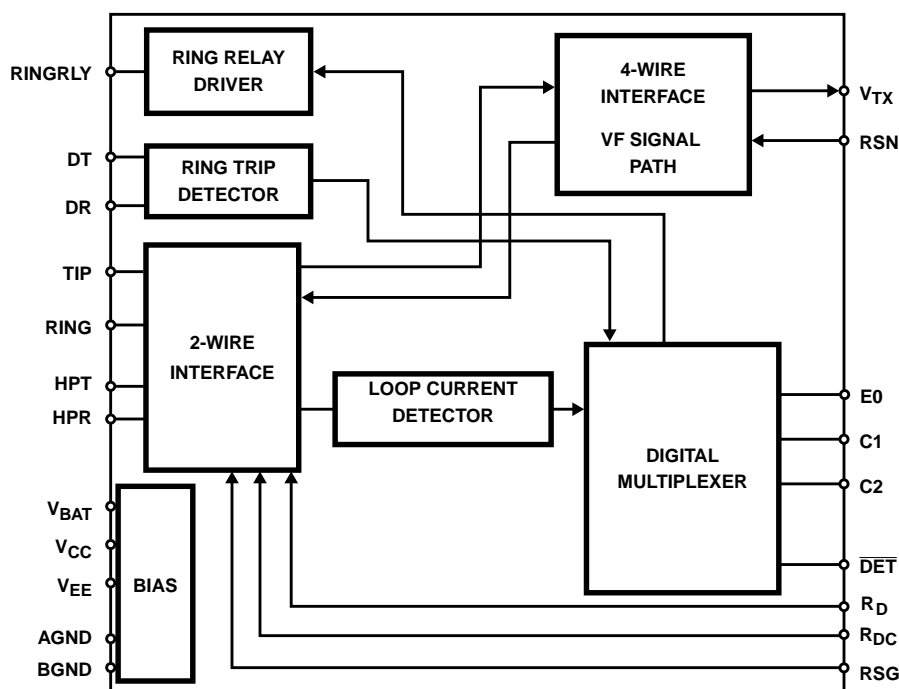
**Features**

- DI Monolithic High Voltage Process
- Programmable Current Feed (20mA to 60mA)
- Programmable Loop Current Detector Threshold and Battery Feed Characteristics
- Ring Trip Detection
- Compatible with Ericsson's PBL3860
- Thermal Shutdown
- On-Hook Transmission
- Wide Battery Voltage Range (-24V to -58V)
- Low Standby Power
- -40°C to 85°C Ambient Temperature Range

**Applications**

- Digital Loop Carrier Systems
- Fiber-In-The-Loop ONUs
- Wireless Local Loop
- Hybrid Fiber Coax
- Related Literature
  - AN9632, Operation of the HC5523/15 Evaluation Board
- Pair Gain
- POTS
- PABX

**Block Diagram**



**Absolute Maximum Ratings**

Temperature, Humidity	
Storage Temperature Range	-65°C to 150°C
Operating Temperature Range	-40°C to 110°C
Operating Junction Temperature Range	-40°C to 150°C
Power Supply (-40°C ≤ T <sub>A</sub> ≤ 85°C)	
Supply Voltage V <sub>CC</sub> to GND	0.5V to 7V
Supply Voltage V <sub>EE</sub> to GND	-7V to 0.5V
Supply Voltage V <sub>BAT</sub> to GND	-80V to 0.5V
Ground	
Voltage between AGND and BGND	-0.3V to 0.3V
Relay Driver	
Ring Relay Supply Voltage	0V to V <sub>BAT</sub> +75V
Ring Relay Current	50mA
Ring Trip Comparator	
Input Voltage	V <sub>BAT</sub> to 0V
Input Current	-5mA to 5mA
Digital Inputs, Outputs (C1, C2, E0, DET)	
Input Voltage	0V to V <sub>CC</sub>
Output Voltage (DET Not Active)	0V to V <sub>CC</sub>
Output Current (DET)	5mA
Tipx and Ringx Terminals (-40°C ≤ T <sub>A</sub> ≤ 85°C)	
Tipx or Ringx Voltage, Continuous (Referenced to GND)	V <sub>BAT</sub> to +2V
Tipx or Ringx, Pulse < 10ms, T <sub>REP</sub> > 10s	V <sub>BAT</sub> -20V to +5V
Tipx or Ringx, Pulse < 10μs, T <sub>REP</sub> > 10s	V <sub>BAT</sub> -40V to +10V
Tipx or Ringx, Pulse < 250ns, T <sub>REP</sub> > 10s	V <sub>BAT</sub> -70V to +15V
Tipx or Ringx Current	70mA
ESD Rating	.500V

**Thermal Information**

Thermal Resistance (Typical, Note 1)	θ <sub>JA</sub> (°C/W)
22 Lead PDIP Package	53
28 Lead PLCC Package	53
Continuous Power Dissipation at 70°C	
22 Lead PDIP Package	1.5W
28 Lead PLCC Package	1.5W
Package Power Dissipation at 70°C, t < 100ms, t <sub>REP</sub> > 1s	
22 Lead PDIP Package	4W
28 Lead PLCC Package	4W
Derate above	
PDIP Package	18.8mW/°C
PLCC Package	18.8mW/°C
Maximum Junction Temperature Range	-40°C to 150°C
Maximum Storage Temperature Range	-65°C to 150°C
Maximum Lead Temperature (Soldering 10s)	300°C (PLCC - Lead Tips Only)

**Die Characteristics**

Gate Count . . . . .543 Transistors, 51 Diodes

*CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.*

**NOTE:**

1. θ<sub>JA</sub> is measured with the component mounted on an evaluation PC board in free air.

**Typical Operating Conditions**

These represent the conditions under which the part was developed and are suggested as guidelines.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Case Temperature		-40	-	100	°C
V <sub>CC</sub> with Respect to AGND	-40°C to 85°C	4.75	-	5.25	V
V <sub>EE</sub> with Respect to AGND	-40°C to 85°C	-5.25	-	-4.75	V
V <sub>BAT</sub> with Respect to BGND	-40°C to 85°C	-58	-	-24	V

**Electrical Specifications**

T<sub>A</sub> = -40°C to 85°C, V<sub>CC</sub> = +5V ±5%, V<sub>EE</sub> = -5V ±5%, V<sub>BAT</sub> = -48V, AGND = BGND = 0V, R<sub>DC1</sub> = R<sub>DC2</sub> = 41.2kΩ, R<sub>D</sub> = 39kΩ, R<sub>SG</sub> = 0Ω, R<sub>F1</sub> = R<sub>F2</sub> = 0Ω, C<sub>HP</sub> = 10nF, C<sub>DC</sub> = 1.5μF, Z<sub>L</sub> = 600Ω, Unless Otherwise Specified. All pin number references in the figures refer to the 28 lead PLCC package.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Overload Level	1% THD, Z <sub>L</sub> = 600Ω, (Note 2, Figure 1)	3.1	-	-	V <sub>PEAK</sub>
Longitudinal Impedance (Tip/Ring)	0 < f < 100Hz (Note 3, Figure 2)	-	20	35	Ω/Wire

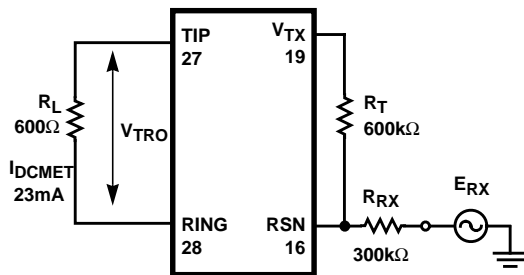


FIGURE 1. OVERLOAD LEVEL (TWO-WIRE PORT)

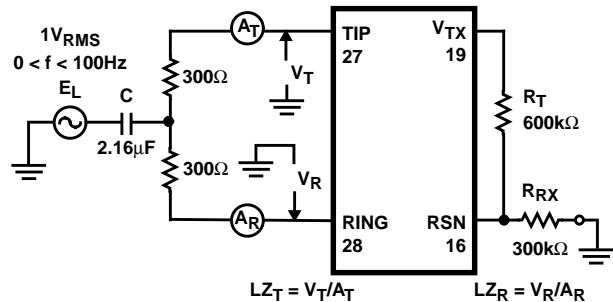


FIGURE 2. LONGITUDINAL IMPEDANCE

**Electrical Specifications**

$T_A = -40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ ,  $V_{CC} = +5\text{V} \pm 5\%$ ,  $V_{EE} = -5\text{V} \pm 5\%$ ,  $V_{BAT} = -48\text{V}$ ,  $\text{AGND} = \text{BGND} = 0\text{V}$ ,  $R_{DC1} = R_{DC2} = 41.2\text{k}\Omega$ ,  $R_D = 39\text{k}\Omega$ ,  $R_{SG} = 0\Omega$ ,  $R_{F1} = R_{F2} = 0\Omega$ ,  $C_{HP} = 10\text{nF}$ ,  $C_{DC} = 1.5\mu\text{F}$ ,  $Z_L = 600\Omega$ , Unless Otherwise Specified. All pin number references in the figures refer to the 28 lead PLCC package. **(Continued)**

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
<b>LONGITUDINAL CURRENT LIMIT (TIP/RING)</b>					
Off-Hook (Active)	No False Detections, (Loop Current), $\text{LB} > 45\text{dB}$ (Note 4, Figure 3A)	20	-	-	$\text{mA}_{\text{PEAK}}/\text{Wire}$
On-Hook (Standby), $R_L = \infty$	No False Detections (Loop Current) (Note 5, Figure 3B)	5	-	-	$\text{mA}_{\text{PEAK}}/\text{Wire}$

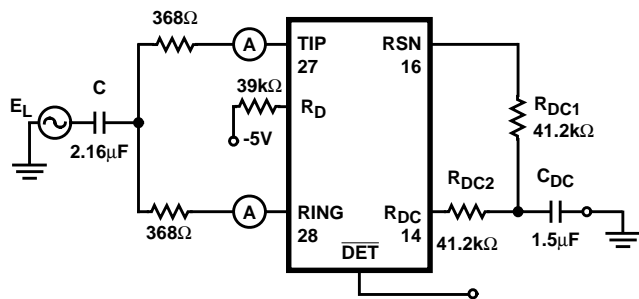


FIGURE 3A. OFF-HOOK

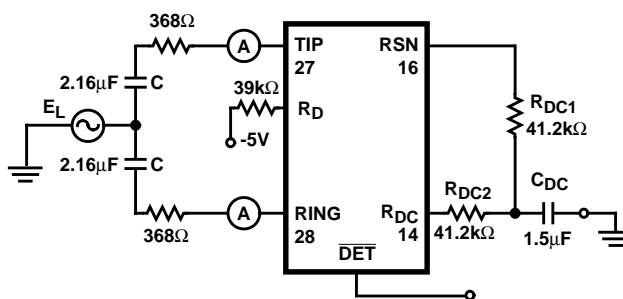


FIGURE 3B. ON-HOOK

FIGURE 3. LONGITUDINAL CURRENT LIMIT

<b>OFF-HOOK LONGITUDINAL BALANCE</b>					
Longitudinal to Metallic	IEEE 455 - 1985, $R_{LR}, R_{LT} = 368\Omega$ , $0.2\text{kHz} < f < 4.0\text{kHz}$ (Note 6, Figure 4)	53	70	-	dB
Longitudinal to Metallic	$R_{LR}, R_{LT} = 300\Omega$ , $0.2\text{kHz} < f < 4.0\text{kHz}$ (Note 6, Figure 4)	53	70	-	dB
Metallic to Longitudinal	FCC Part 68, Para 68.310, $0.2\text{kHz} < f < 1.0\text{kHz}$	50	55	-	dB
	$1.0\text{kHz} < f < 4.0\text{kHz}$ (Note 7)	50	55	-	dB
Longitudinal to 4-Wire	$0.2\text{kHz} < f < 4.0\text{kHz}$ (Note 8, Figure 4)	53	70	-	dB
Metallic to Longitudinal	$R_{LR}, R_{LT} = 300\Omega$ , $0.2\text{kHz} < f < 4.0\text{kHz}$ (Note 9, Figure 5)	50	55	-	dB
4-Wire to Longitudinal	$0.2\text{kHz} < f < 4.0\text{kHz}$ (Note 10, Figure 5)	50	55	-	dB

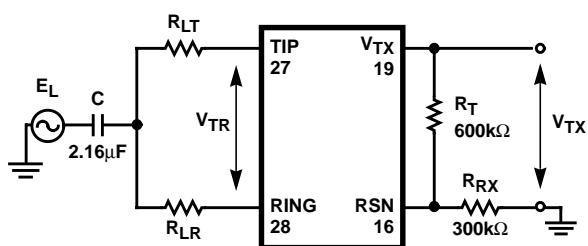


FIGURE 4. LONGITUDINAL TO METALLIC AND LONGITUDINAL TO 4-WIRE BALANCE

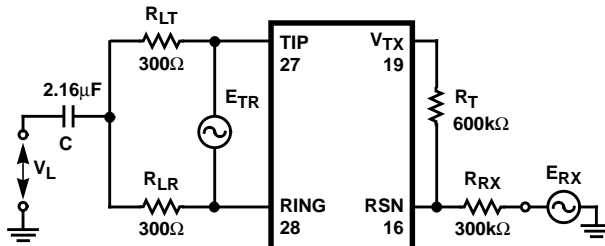


FIGURE 5. METALLIC TO LONGITUDINAL AND 4-WIRE TO LONGITUDINAL BALANCE

2-Wire Return Loss $C_{HP} = 20\text{nF}$	$0.2\text{kHz}$ to $0.5\text{kHz}$ (Note 11, Figure 6)	25	-	-	dB
	$0.5\text{kHz}$ to $1.0\text{kHz}$ (Note 11, Figure 6)	27	-	-	dB
	$1.0\text{kHz}$ to $3.4\text{kHz}$ (Note 11, Figure 6)	23	-	-	dB

<b>TIP IDLE VOLTAGE</b>					
Active, $I_L = 0$		-	-1.5	-	V
Standby, $I_L = 0$		-	<0	-	V
<b>RING IDLE VOLTAGE</b>					
Active, $I_L = 0$		-	-46.5	-	V

**Electrical Specifications**

$T_A = -40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ ,  $V_{CC} = +5\text{V} \pm 5\%$ ,  $V_{EE} = -5\text{V} \pm 5\%$ ,  $V_{BAT} = -48\text{V}$ ,  $AGND = BGND = 0\text{V}$ ,  $R_{DC1} = R_{DC2} = 41.2\text{k}\Omega$ ,  $R_D = 39\text{k}\Omega$ ,  $R_{SG} = 0\Omega$ ,  $R_{F1} = R_{F2} = 0\Omega$ ,  $C_{HP} = 10\text{nF}$ ,  $C_{DC} = 1.5\mu\text{F}$ ,  $Z_L = 600\Omega$ , Unless Otherwise Specified. All pin number references in the figures refer to the 28 lead PLCC package. **(Continued)**

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Standby, $I_L = 0$		-	>-48	-	V
TIP-RING Open Loop Metallic Voltage, $V_{TR}$	$V_{BAT} = -52\text{V}$ , $R_{SG} = 0\Omega$	43	-	47	V
<b>4-WIRE TRANSMIT PORT (<math>V_{TX}</math>)</b>					
Overload Level	$Z_L > 20\text{k}\Omega$ , 1% THD (Note 12, Figure 7)	3.1	-	-	$V_{PEAK}$
Output Offset Voltage	$E_G = 0$ , $Z_L = \infty$ (Note 13, Figure 7)	-60	-	60	mV
Output Impedance (Guaranteed by Design)	$0.2\text{kHz} < f < 03.4\text{kHz}$	-	5	20	$\Omega$
2-Wire to 4-Wire (Metallic to $V_{TX}$ ) Voltage Gain	$0.3\text{kHz} < f < 03.4\text{kHz}$ (Note 14, Figure 7)	0.98	1.0	1.02	V/V

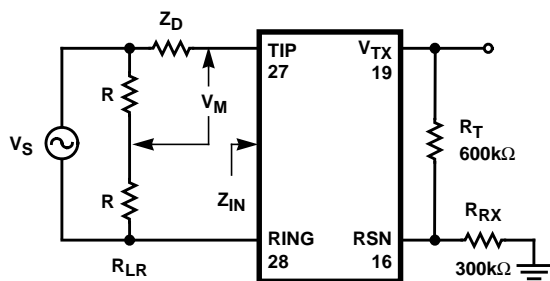


FIGURE 6. TWO-WIRE RETURN LOSS

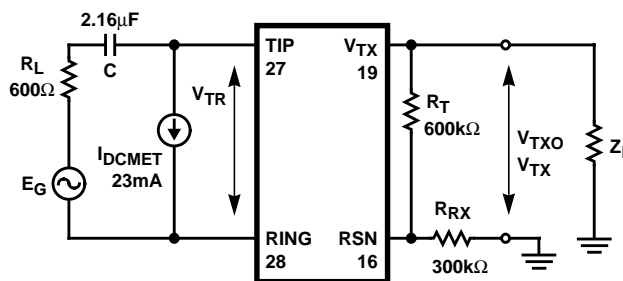


FIGURE 7. OVERLOAD LEVEL (4-WIRE TRANSMIT PORT), OUTPUT OFFSET VOLTAGE, 2-WIRE TO 4-WIRE VOLTAGE GAIN AND HARMONIC DISTORTION

<b>4-WIRE RECEIVE PORT (RSN)</b>					
DC Voltage	$I_{RSN} = 0\text{mA}$	-	0	-	V
$R_X$ Sum Node Impedance (Gtd by Design)	$0.2\text{kHz} < f < 3.4\text{kHz}$	-	-	20	$\Omega$
Current Gain-RSN to Metallic	$0.3\text{kHz} < f < 3.4\text{kHz}$ (Note 15, Figure 8)	900	1000	1100	Ratio
<b>FREQUENCY RESPONSE (OFF-HOOK)</b>					
2-Wire to 4-Wire	0dBm at 1.0kHz, $E_{RX} = 0\text{V}$ $0.3\text{kHz} < f < 3.4\text{kHz}$ (Note 16, Figure 9)	-0.2	-	0.2	dB
4-Wire to 2-Wire	0dBm at 1.0kHz, $E_G = 0\text{V}$ $0.3\text{kHz} < f < 3.4\text{kHz}$ (Note 17, Figure 9)	-0.2	-	0.2	dB
4-Wire to 4-Wire	0dBm at 1.0kHz, $E_G = 0\text{V}$ $0.3\text{kHz} < f < 3.4\text{kHz}$ (Note 18, Figure 9)	-0.2	-	0.2	dB
<b>INSERTION LOSS</b>					
2-Wire to 4-Wire	0dBm, 1kHz (Note 19, Figure 9)	-0.2	-	0.2	dB
4-Wire to 2-Wire	0dBm, 1kHz (Note 20, Figure 9)	-0.2	-	0.2	dB
<b>GAIN TRACKING (Ref = -10dBm, at 1.0kHz)</b>					
2-Wire to 4-Wire	+3dBm to +7dBm (Note 21, Figure 9)	-0.15	-	0.15	dB
2-Wire to 4-Wire	-40dBm to +3dBm (Note 21, Figure 9)	-0.1	-	0.1	dB
2-Wire to 4-Wire	-55dBm to -40dBm (Note 21, Figure 9)	-0.2	-	0.2	dB
4-Wire to 2-Wire	-40dBm to +7dBm (Note 22, Figure 9)	-0.1	-	0.1	dB

**Electrical Specifications**

$T_A = -40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ ,  $V_{CC} = +5\text{V} \pm 5\%$ ,  $V_{EE} = -5\text{V} \pm 5\%$ ,  $V_{BAT} = -48\text{V}$ ,  $\text{AGND} = \text{BGND} = 0\text{V}$ ,  $R_{DC1} = R_{DC2} = 41.2\text{k}\Omega$ ,  $R_D = 39\text{k}\Omega$ ,  $R_{SG} = 0\Omega$ ,  $R_{F1} = R_{F2} = 0\Omega$ ,  $C_{HP} = 10\text{nF}$ ,  $C_{DC} = 1.5\mu\text{F}$ ,  $Z_L = 600\Omega$ , Unless Otherwise Specified. All pin number references in the figures refer to the 28 lead PLCC package. **(Continued)**

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
4-Wire to 2-Wire	-55dBm to -40dBm (Note 22, Figure 9)	-0.2	-	0.2	dB

$$GRX = ((V_{TR1} - V_{TR2})(300k))/(-3)(600)$$

Where:  $V_{TR1}$  is the Tip to Ring Voltage with  $V_{RSN} = 0\text{V}$   
and  $V_{TR2}$  is the Tip to Ring Voltage with  $V_{RSN} = -3\text{V}$

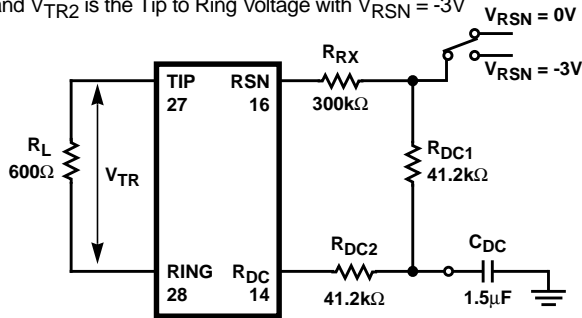


FIGURE 8. CURRENT GAIN-RSN TO METALLIC

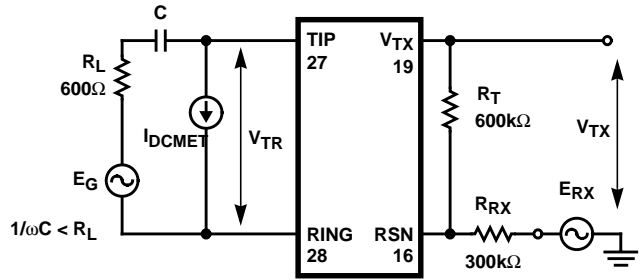


FIGURE 9. FREQUENCY RESPONSE, INSERTION LOSS, GAIN TRACKING AND HARMONIC DISTORTION

**NOISE**

Idle Channel Noise at 2-Wire	C-Message Weighting (Note 23, Figure 10)	-	8.5	-	dBrnC
	Psophometrical Weighting (Note 23, Figure 10)	-	-81.5	-	dBrnp
Idle Channel Noise at 4-Wire	C-Message Weighting (Note 24, Figure 10)	-	8.5	-	dBrnC
	Psophometrical Weighting (Note 23, Figure 10)	-	-81.5	-	dBrnp

**HARMONIC DISTORTION**

2-Wire to 4-Wire	0dBm, 1kHz (Note 25, Figure 7)	-	-65	-54	dB
4-Wire to 2-Wire	0dBm, 0.3kHz to 3.4kHz (Note 26, Figure 9)	-	-65	-54	dB

**BATTERY FEED CHARACTERISTICS**

Constant Loop Current Tolerance $R_{DCX} = 41.2\text{k}\Omega$	$I_L = 2500/(R_{DC1} + R_{DC2})$ , -40°C to 85°C (Note 27)	$0.85I_L$	$I_L$	$1.15I_L$	mA
Loop Current Tolerance (Standby)	$I_L = (V_{BAT}-3)/(R_L + 1800)$ , -40°C to 85°C (Note 28)	$0.75I_L$	$I_L$	$1.25I_L$	mA
Open Circuit Voltage ( $V_{TIP} - V_{RING}$ )	-40°C to 85°C, (Active) $R_{SG} = \infty$	14	16.67	20	V

**LOOP CURRENT DETECTOR**

On-Hook to Off-Hook	$R_D = 33\text{k}\Omega$ , -40°C to 85°C	11	$465/R_D$	17.2	mA
Off-Hook to On-Hook	$R_D = 33\text{k}\Omega$ , -40°C to 85°C	9.5	$405/R_D$	15.0	mA
Loop Current Hysteresis	$R_D = 33\text{k}\Omega$ , -40°C to 85°C	-	$60/R_D$	-	mA

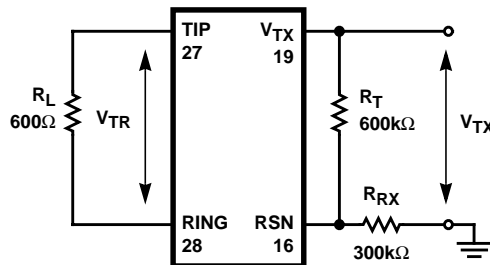


FIGURE 10. IDLE CHANNEL NOISE

## HC5515

### Electrical Specifications

$T_A = -40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ ,  $V_{CC} = +5\text{V} \pm 5\%$ ,  $V_{EE} = -5\text{V} \pm 5\%$ ,  $V_{BAT} = -48\text{V}$ ,  $AGND = BGND = 0\text{V}$ ,  $R_{DC1} = R_{DC2} = 41.2\text{k}\Omega$ ,  $R_D = 39\text{k}\Omega$ ,  $R_{SG} = 0\Omega$ ,  $R_{F1} = R_{F2} = 0\Omega$ ,  $C_{HP} = 10\text{nF}$ ,  $C_{DC} = 1.5\mu\text{F}$ ,  $Z_L = 600\Omega$ , Unless Otherwise Specified. All pin number references in the figures refer to the 28 lead PLCC package. **(Continued)**

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
<b>RING TRIP DETECTOR (DT, DR)</b>					
Offset Voltage	Source Res = 0	-20	-	20	mV
Input Bias Current	Source Res = 0	-360	-	360	nA
Input Common-Mode Range	Source Res = 0	$V_{BAT} + 1$	-	0	V
Input Resistance	Source Res = 0, Unbalanced	1	-	-	M $\Omega$
	Source Res = 0, Balanced	3	-	-	M $\Omega$
<b>RING RELAY DRIVER</b>					
$V_{SAT}$ at 25mA	$I_{OL} = 25\text{mA}$	-	0.2	0.6	V
Off-State Leakage Current	$V_{OH} = 12\text{V}$	-	-	10	$\mu\text{A}$
<b>DIGITAL INPUTS (E0, C1, C2)</b>					
Input Low Voltage, $V_{IL}$		0	-	0.8	V
Input High Voltage, $V_{IH}$		2	-	$V_{CC}$	V
Input Low Current, $I_{IL}$ : C1, C2	$V_{IL} = 0.4\text{V}$	-200	-	-	$\mu\text{A}$
Input Low Current, $I_{IL}$ : E0	$V_{IL} = 0.4\text{V}$	-100	-	-	$\mu\text{A}$
Input High Current	$V_{IH} = 2.4\text{V}$	-	-	40	$\mu\text{A}$
<b>DETECTOR OUTPUT (<math>\overline{\text{DET}}</math>)</b>					
Output Low Voltage, $V_{OL}$	$I_{OL} = 2\text{mA}$	-	-	0.45	V
Output High Voltage, $V_{OH}$	$I_{OH} = 100\mu\text{A}$	2.7	-	-	V
Internal Pull-Up Resistor		8	15	25	k $\Omega$
<b>POWER DISSIPATION (<math>V_{BAT} = -48\text{V}</math>)</b>					
Open Circuit State	$C1 = C2 = 0$	-	26.3	70	mW
On-Hook, Standby	$C1 = C2 = 1$	-	37.5	85	mW
On-Hook, Active	$C1 = 0, C2 = 1, R_L = \text{High Impedance}$	-	110	300	mW
Off-Hook, Active	$C1 = 0, C2 = 1, R_L = 600\Omega$	-	1.1	1.4	W
<b>TEMPERATURE GUARD</b>					
Thermal Shutdown		150	-	180	$^{\circ}\text{C}$
<b>SUPPLY CURRENTS (<math>V_{BAT} = -28\text{V}</math>)</b>					
Open Circuit State ( $C1, 2 = 0, 0$ ) On-Hook	$I_{CC}$	-	1.3	2.8	mA
	$I_{EE}$	-	0.6	2.0	mA
	$I_{BAT}$	-	0.35	1.2	mA
Standby State ( $C1, 2 = 1, 1$ ) On-Hook	$I_{CC}$	-	1.6	3.5	mA
	$I_{EE}$	-	0.62	2.0	mA
	$I_{BAT}$	-	0.55	1.6	mA
Active State ( $C1, 2 = 0, 1$ ) On-Hook	$I_{CC}$	-	3.7	9.5	mA
	$I_{EE}$	-	1.1	4.0	mA
	$I_{BAT}$	-	2.2	5.2	mA
<b>PSRR</b>					
$V_{CC}$ to 2 or 4-Wire Port	(Note 29, Figure 11)	-	40	-	dB
$V_{EE}$ to 2 or 4-Wire Port	(Note 29, Figure 11)	-	40	-	dB

**Electrical Specifications**  $T_A = -40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ ,  $V_{CC} = +5\text{V} \pm 5\%$ ,  $V_{EE} = -5\text{V} \pm 5\%$ ,  $V_{BAT} = -48\text{V}$ ,  $AGND = BGND = 0\text{V}$ ,  $R_{DC1} = R_{DC2} = 41.2\text{k}\Omega$ ,  $R_D = 39\text{k}\Omega$ ,  $R_{SG} = 0\Omega$ ,  $R_{F1} = R_{F2} = 0\Omega$ ,  $C_{HP} = 10\text{nF}$ ,  $C_{DC} = 1.5\mu\text{F}$ ,  $Z_L = 600\Omega$ , Unless Otherwise Specified. All pin number references in the figures refer to the 28 lead PLCC package. **(Continued)**

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
$V_{BAT}$ to 2 or 4-Wire Port	(Note 29, Figure 11)	-	40	-	dB

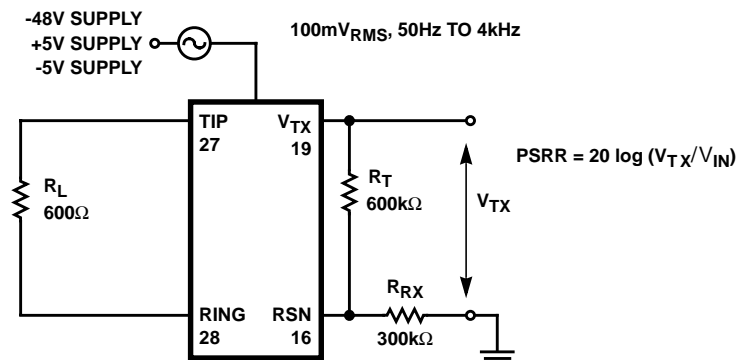


FIGURE 11. POWER SUPPLY REJECTION RATIO

## Circuit Operation and Design Information

The HC5515 is a current feed voltage sense Subscriber Line Interface Circuit (SLIC). This means that for short loop applications the SLIC provides a programed constant current to the tip and ring terminals while sensing the tip to ring voltage.

The following discussion separates the SLIC's operation into its DC and AC paths, then follows up with additional circuit and design information.

### Constant Loop Current (DC) Path

#### SLIC in the Active Mode

The DC path establishes a constant loop current that flows out of tip and into the ring terminal. The loop current is programmed by resistors  $R_{DC1}$ ,  $R_{DC2}$  and the voltage on the  $R_{DC}$  pin (Figure 12). The  $R_{DC}$  voltage is determined by the voltage across  $R_1$  in the saturation guard circuit. Under constant current feed conditions, the voltage drop across  $R_1$  sets the  $R_{DC}$  voltage to  $-2.5\text{V}$ . This occurs when current flows through  $R_1$  into the current source  $I_2$ . The  $R_{DC}$  voltage establishes a current ( $I_{RSN}$ ) that is equal to  $V_{RDC}/(R_{DC1} + R_{DC2})$ . This current is then multiplied by 1000, in the loop current circuit, to become the tip and ring loop currents.

For the purpose of the following discussion, the saturation guard voltage is defined as the maximum tip to ring voltage at which the SLIC can provide a constant current for a given battery and overhead voltage.

For loop resistances that result in a tip to ring voltage less than the saturation guard voltage the loop current is defined as:

$$I_L = \frac{2.5\text{V}}{R_{DC1} + R_{DC2}} \times 1000 \quad (\text{EQ. 1})$$

where:  $I_L$  = Constant loop current, and

$R_{DC1}$  and  $R_{DC2}$  = Loop current programming resistors.

Capacitor  $C_{DC}$  between  $R_{DC1}$  and  $R_{DC2}$  removes the VF signals from the battery feed control loop. The value of  $C_{DC}$  is determined by Equation 2:

$$C_{DC} = T \times \left( \frac{1}{R_{DC1}} + \frac{1}{R_{DC2}} \right) \quad (\text{EQ. 2})$$

where  $T = 30\text{ms}$ .

NOTE: The minimum  $C_{DC}$  value is obtained if  $R_{DC1} = R_{DC2}$ .

Figure 13 illustrates the relationship between the tip to ring voltage and the loop resistance. For a  $0\Omega$  loop resistance both tip and ring are at  $V_{BAT}/2$ . As the loop resistance increases, so does the voltage differential between tip and ring. When this differential voltage becomes equal to the saturation guard voltage, the operation of the SLIC's loop feed changes from a constant current feed to a resistive feed. The loop current in the resistive feed region is no longer constant but varies as a function of the loop resistance.

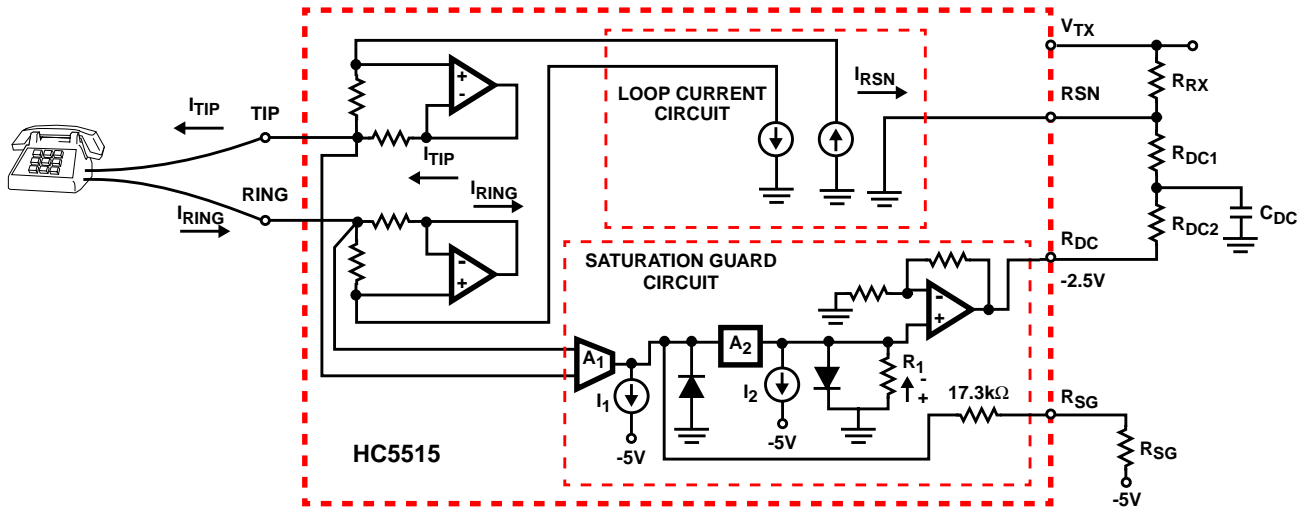


FIGURE 12. DC LOOP CURRENT

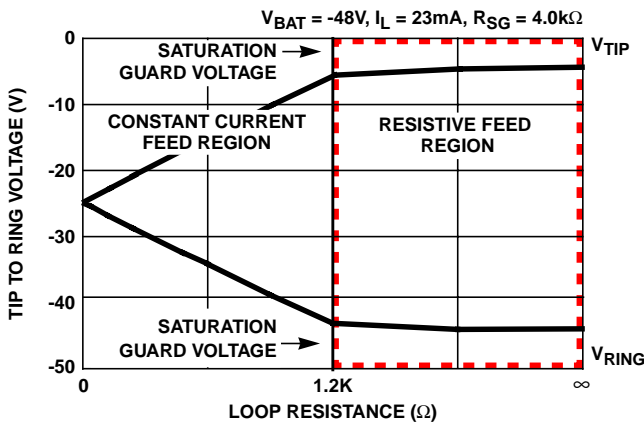
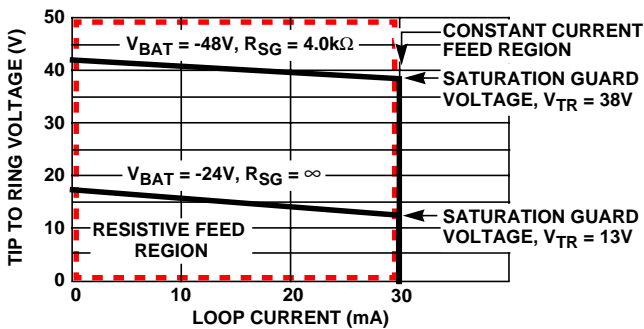


FIGURE 13.  $V_{TR}$  vs  $R_L$

Figure 14 shows the relationship between the saturation guard voltage, the loop current and the loop resistance. Notice from Figure 14 that for a loop resistance  $< 1.2k\Omega$  ( $R_{SG} = 4.0k\Omega$ ) the SLIC is operating in the constant current feed region and for resistances  $> 1.2k\Omega$  the SLIC is operating in the resistive feed region. Operation in the resistive feed region allows long loop and off-hook transmission by keeping the tip and ring voltages off the rails. Operation in this region is transparent to the customer.



$R_L$	100kΩ	4kΩ	2kΩ	$< 1.2k\Omega$	$R_{SG} = 4.0k\Omega$
$R_L$	100kΩ	1.5kΩ	700Ω	$< 400\Omega$	$R_{SG} = \infty\Omega$

FIGURE 14.  $V_{TR}$  vs  $I_L$  and  $R_L$

The Saturation Guard circuit (Figure 12) monitors the tip to ring voltage via the transconductance amplifier  $A_1$ .  $A_1$  generates a current that is proportional to the tip to ring voltage difference.  $I_1$  is internally set to sink all of  $A_1$ 's current until the tip to ring voltage exceeds 12.5V. When the tip to ring voltage exceeds 12.5V (with no  $R_{SG}$  resistor)  $A_1$  supplies more current than  $I_1$  can sink. When this happens  $A_2$  amplifies its input current by a factor of 12 and the current through  $R_1$  becomes the difference between  $I_2$  and the output current from  $A_2$ . As the current from  $A_2$  increases, the voltage across  $R_1$  decreases and the output voltage on  $R_{DC}$  decreases. This results in a corresponding decrease in the loop current. The  $R_{SG}$  pin provides the ability to increase the saturation guard reference voltage beyond 12.5V. Equation 3 gives the relationship between the  $R_{SG}$  resistor value and the programmable saturation guard reference voltage:

$$V_{SGREF} = 12.5 + \frac{5 \cdot 10^5}{R_{SG} + 17300} \quad (\text{EQ. 3})$$

where:

$V_{SGREF}$  = Saturation Guard reference voltage, and  
 $R_{SG}$  = Saturation Guard programming resistor.

When the Saturation guard reference voltage is exceeded, the tip to ring voltage is calculated using Equation 4:

$$V_{TR} = R_L \times \frac{16.66 + 5 \cdot 10^5 / (R_{SG} + 17300)}{R_L + (R_{DC1} + R_{DC2}) / 600} \quad (\text{EQ. 4})$$

where:

$V_{TR}$  = Voltage differential between tip and ring, and  
 $R_L$  = Loop resistance.

For on-hook transmission  $R_L = \infty$ , Equation 4 reduces to:

$$V_{TR} = 16.66 + \frac{5 \cdot 10^5}{R_{SG} + 17300} \quad (\text{EQ. 5})$$

The value of  $R_{SG}$  should be calculated to allow maximum loop length operation. This requires that the saturation guard reference voltage be set as high as possible without clipping the incoming or outgoing VF signal. A voltage margin of -4V



on tip and -4V on ring, for a total of -8V margin, is recommended as a general guideline. The value of  $R_{SG}$  is calculated using Equation 6:

$$R_{SG} = \left( \frac{5 \cdot 10^5}{(|V_{BAT}| - V_{MAR}) \times \left( 1 + \frac{(R_{DC1} + R_{DC2})}{600R_L} \right)} - 17300 \right) \quad (\text{EQ. 6})$$

where:

$V_{BAT}$  = Battery voltage, and

$V_{MAR}$  = Voltage Margin. Recommended value of -8V to allow a maximum overload level of  $3.1V_{PEAK}$ .

For on-hook transmission  $R_L = \infty$ , Equation 6 reduces to:

$$R_{SG} = \frac{5 \cdot 10^5}{|V_{BAT}| - V_{MAR} - 16.66V} - 17300 \quad (\text{EQ. 7})$$

### SLIC in the Standby Mode

Overall system power is saved by configuring the SLIC in the standby state when not in use. In the standby state the tip and ring amplifiers are disabled and internal resistors are connected between tip to ground and ring to  $V_{BAT}$ . This connection enables a loop current to flow when the phone goes off-hook. The loop current detector then detects this current and the SLIC is configured in the active mode for voice transmission. The loop current in standby state is calculated as follows:

$$I_L \approx \frac{|V_{BAT}| - 3V}{R_L + 1800\Omega} \quad (\text{EQ. 8})$$

where:

$I_L$  = Loop current in the standby state,

$R_L$  = Loop resistance, and

$V_{BAT}$  = Battery voltage.

### (AC) Transmission Path

#### SLIC in the Active Mode

Figure 15 shows a simplified AC transmission model. Circuit analysis yields the following design equations:

$$V_{TR} = V_{TX} + I_M \cdot 2R_F \quad (\text{EQ. 9})$$

$$\frac{V_{TX}}{Z_T} + \frac{V_{RX}}{Z_{RX}} = \frac{I_M}{1000} \quad (\text{EQ. 10})$$

$$V_{TR} = E_G - I_M \cdot Z_L \quad (\text{EQ. 11})$$

where:

$V_{TR}$  = Is the AC metallic voltage between tip and ring, including the voltage drop across the fuse resistors  $R_F$ ,

$V_{TX}$  = Is the AC metallic voltage. Either at the ground referenced 4-wire side or the SLIC tip and ring terminals,

$I_M$  = Is the AC metallic current,

$R_F$  = Is a fuse resistor,

$Z_T$  = Is used to set the SLIC's 2-wire impedance,

$V_{RX}$  = Is the analog ground referenced receive signal,

$Z_{RX}$  = Is used to set the 4-wire to 2-wire gain,

$E_G$  = Is the AC open circuit voltage, and

$Z_L$  = Is the line impedance.

#### (AC) 2-Wire Impedance

The AC 2-wire impedance ( $Z_{TR}$ ) is the impedance looking into the SLIC, including the fuse resistors, and is calculated as follows:

Let  $V_{RX} = 0$ . Then from Equation 10:

$$V_{TX} = Z_T \cdot \frac{I_M}{1000} \quad (\text{EQ. 12})$$

$Z_{TR}$  is defined as:

$$Z_{TR} = \frac{V_{TR}}{I_M} \quad (\text{EQ. 13})$$

Substituting in Equation 9 for  $V_{TR}$ :

$$Z_{TR} = \frac{V_{TX}}{I_M} + \frac{2R_F \cdot I_M}{I_M} \quad (\text{EQ. 14})$$

Substituting in Equation 12 for  $V_{TX}$ :

$$Z_{TR} = \frac{Z_T}{1000} + 2R_F \quad (\text{EQ. 15})$$

Therefore:

$$Z_T = 1000 \cdot (Z_{TR} - 2R_F) \quad (\text{EQ. 16})$$

Equation 16 can now be used to match the SLIC's impedance to any known line impedance ( $Z_{TR}$ ).

#### Example:

Calculate  $Z_T$  to make  $Z_{TR} = 600\Omega$  in series with  $2.16\mu F$ .  
 $R_F = 20\Omega$ .

$$Z_T = 1000 \cdot \left( 600 + \frac{1}{j\omega \cdot 2.16 \cdot 10^{-6}} - 2 \cdot 20 \right)$$

$Z_T = 560k\Omega$  in series with  $2.16nF$ .

#### (AC) 2-Wire to 4-Wire Gain

The 2-wire to 4-wire gain is equal to  $V_{TX}/V_{TR}$ .

From Equations 9 and 10 with  $V_{RX} = 0$ :

$$A_{2-4} = \frac{V_{TX}}{V_{TR}} = \frac{Z_T/1000}{Z_T/1000 + 2R_F} \quad (\text{EQ. 17})$$

#### (AC) 4-Wire to 2-Wire Gain

The 4-wire to 2-wire gain is equal to  $V_{TR}/V_{RX}$ .

From Equations 9, 10 and 11 with  $E_G = 0$ :

$$A_{4-2} = \frac{V_{TR}}{V_{RX}} = -\frac{Z_T}{Z_{RX}} \cdot \frac{Z_L}{\frac{Z_T}{1000} + 2R_F + Z_L} \quad (\text{EQ. 18})$$



Cases 2 and 3 illustrate the longitudinal loop current. The definition of a longitudinal loop current is a common mode current, that flows either out of or into tip and ring simultaneously. Longitudinal currents in the on-hook state result in **equal** currents flowing through the sense resistors  $R_1$  and  $R_2$  (Figure 17). And longitudinal currents in the off-hook state result in **unequal** currents flowing through the sense resistors  $R_1$  and  $R_2$ . Notice that for case 2, longitudinal currents flowing away from the SLIC, the current through  $R_1$  is the metallic loop current plus the longitudinal current; whereas the current through  $R_2$  is the metallic loop current minus the longitudinal current. Longitudinal currents are generated when the phone line is influenced by magnetic fields (e.g. power lines).

**Loop Current Detector**

Figure 17 shows a simplified schematic of the loop current detector. The loop current detector works by sensing the metallic current flowing through resistors  $R_1$  and  $R_2$ . This results in a current ( $I_{RD}$ ) out of the transconductance amplifier ( $gm_1$ ) that is equal to the product of  $gm_1$  and the metallic loop current.  $I_{RD}$  then flows out the  $R_D$  pin and through resistor  $R_D$  to  $V_{EE}$ . The value of  $I_{RD}$  is equal to:

$$I_{RD} = \frac{|I_{TIP} - I_{RING}|}{600} = \frac{I_L}{300} \tag{EQ. 24}$$

The  $I_{RD}$  current results in a voltage drop across  $R_D$  that is compared to an internal 1.25V reference voltage. When the voltage drop across  $R_D$  exceeds 1.25V, and the logic is configured for loop current detection, the  $\overline{DET}$  pin goes low.

The hysteresis resistor  $R_H$  adds an additional voltage effectively across  $R_D$ , causing the on-hook to off-hook threshold to be slightly higher than the off-hook to on-hook threshold.

Taking into account the hysteresis voltage, the typical value of  $R_D$  for the on-hook to off-hook condition is:

$$R_D = \frac{465}{\text{ON-HOOK to OFF-HOOK}} \tag{EQ. 25}$$

Taking into account the hysteresis voltage, the typical value of  $R_D$  for the off-hook to on-hook condition is:

$$R_D = \frac{375}{\text{OFF-HOOK to ON-HOOK}} \tag{EQ. 26}$$

A filter capacitor ( $C_D$ ) in parallel with  $R_D$  will improve the accuracy of the trip point in a noisy environment. The value of this capacitor is calculated using the following Equation:

$$C_D = \frac{T}{R_D} \tag{EQ. 27}$$

where:  $T = 0.5\text{ms}$ .

**Ring Trip Detector**

Ring trip detection is accomplished with the internal ring trip comparator and the external circuitry shown in Figure 18. The process of ring trip is initiated when the logic input pins are in the following states:  $E0 = 0$ ,  $C1 = 1$  and  $C2 = 0$ . This logic condition connects the ring trip comparator to the  $\overline{DET}$  output, and causes the Ringing pin to energize the ring relay. The ring relay connects the tip and ring of the phone to the external circuitry in Figure 18. When the phone is on-hook the DT pin is more positive than the DR pin and the  $\overline{DET}$  output is high. For off-hook conditions DR is more positive than DT and  $\overline{DET}$  goes low. When  $\overline{DET}$  goes low, indicating that the phone has gone off-hook, the SLIC is commanded by the logic inputs to go into the active state. In the active state, tip and ring are once again connected to the phone and normal operation ensues.

Figure 18 illustrates battery backed unbalanced ring injected ringing. For tip injected ringing just reverse the leads to the phone. The ringing source could also be balanced.

NOTE: The  $\overline{DET}$  output will toggle at 20Hz because the DT input is not completely filtered by  $C_{RT}$ . Software can examine the duty cycle and determine if the  $\overline{DET}$  pin is low for more that half the time, if so the off-hook condition is indicated.

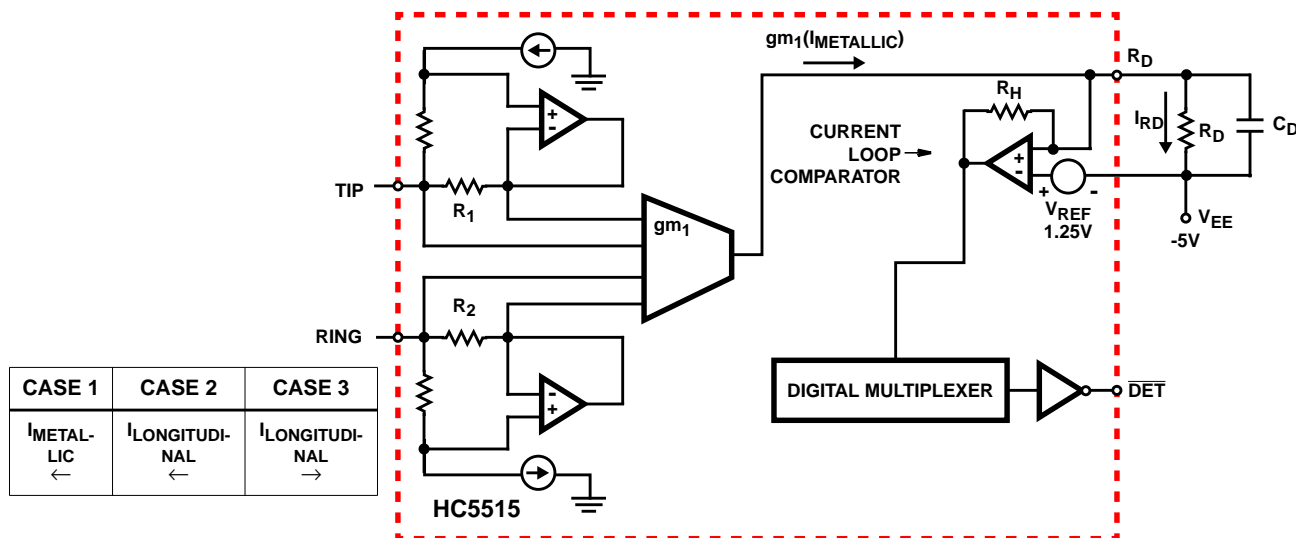


FIGURE 17. LOOP CURRENT DETECTOR

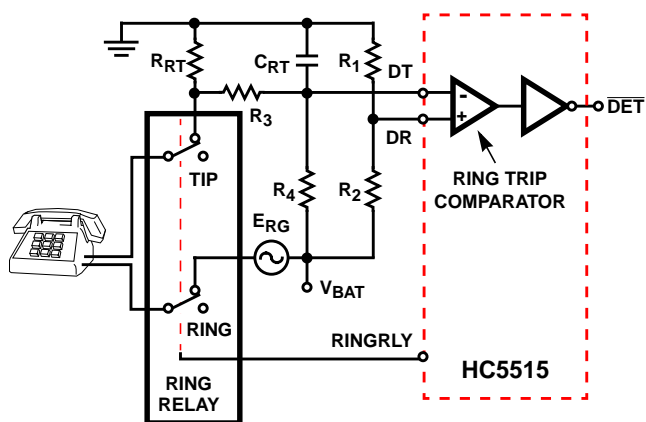


FIGURE 18. RING TRIP CIRCUIT FOR BATTERY BACKED RINGING

### Longitudinal Impedance

The feedback loop described in Figure 19(A, B) realizes the desired longitudinal impedances from tip to ground and from ring to ground. Nominal longitudinal impedance is resistive and in the order of  $22\Omega$ .

In the presence of longitudinal currents this circuit attenuates the voltages that would otherwise appear at the tip and ring terminals, to levels well within the common mode range of the SLIC. In fact, longitudinal currents may exceed the programmed DC loop current without disturbing the SLIC's VF transmission capabilities.

The function of this circuit is to maintain the tip and ring voltages symmetrically around  $V_{BAT}/2$ , in the presence of longitudinal currents. The differential transconductance amplifiers  $G_T$  and  $G_R$  accomplish this by sourcing or sinking the required current to maintain  $V_C$  at  $V_{BAT}/2$ .

When a longitudinal current is injected onto the tip and ring inputs, the voltage at  $V_C$  moves from its equilibrium value  $V_{BAT}/2$ . When  $V_C$  changes by the amount  $\Delta V_C$ , this change appears between the input terminals of the differential

transconductance amplifiers  $G_T$  and  $G_R$ . The output of  $G_T$  and  $G_R$  are the differential currents  $\Delta I_1$  and  $\Delta I_2$ , which in turn feed the differential inputs of current sources  $I_T$  and  $I_R$  respectively.  $I_T$  and  $I_R$  have current gains of 250 single ended and 500 differentially, thus leading to a change in  $I_T$  and  $I_R$  that is equal to  $500(\Delta I_1)$  and  $500(\Delta I_2)$ .

The circuit shown in Figure 19(B) illustrates the tip side of the longitudinal network. The advantages of a differential input current source are: improved noise since the noise due to current source  $2I_0$  is now correlated, power savings due to differential current gain and minimized offset error at the Operational Amplifier inputs via the two  $5k\Omega$  resistors.

### Digital Logic Inputs

Table 1 is the logic truth table for the TTL compatible logic input pins. The HC5515 has an enable input pin (E0) and two control inputs pins (C1, C2).

The enable pin E0 is used to enable or disable the  $\overline{DET}$  output pin. The  $\overline{DET}$  pin is enabled if E0 is at a logic level 0 and disabled if E0 is at a logic level 1.

A combination of the control pins C1 and C2 is used to select 1 of the 4 possible operating states. A description of each operating state and the control logic follow:

#### Open Circuit State (C1 = 0, C2 = 0)

In this state the SLIC is effectively off. All detectors and both the tip and ring line drive amplifiers are powered down, presenting a high impedance to the line. Power dissipation is at a minimum.

#### Active State (C1 = 0, C2 = 1)

The tip output is capable of sourcing loop current and for open circuit conditions is about  $-4V$  from ground. The ring output is capable of sinking loop current and for open circuit conditions is about  $V_{BAT} + 4V$ . VF signal transmission is normal. The loop current detector is active, E0 determines if the detector is gated to the  $\overline{DET}$  output.

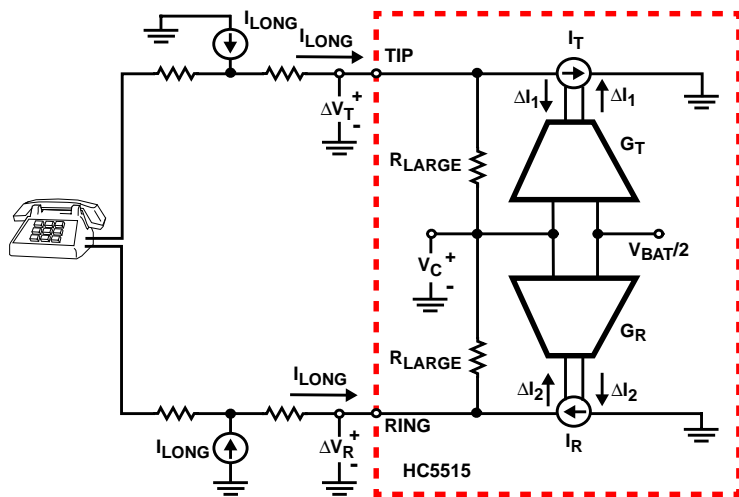


FIGURE 19A.

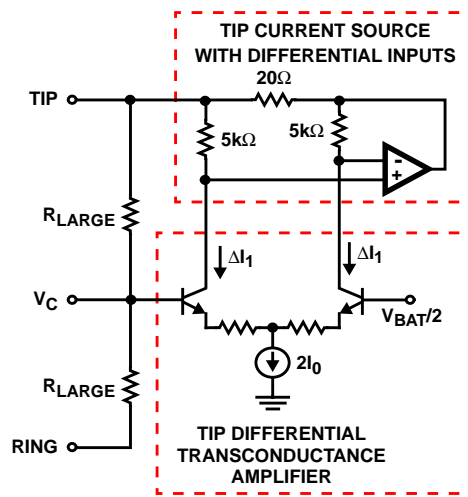


FIGURE 19B.

FIGURE 19. LONGITUDINAL IMPEDANCE NETWORK

**Ringing State (C1 = 1, C2 = 0)**

The ring relay driver and the ring trip detector are activated. Both the tip and ring line drive amplifiers are powered down. Both tip and ring are disconnected from the line via the external ring relay.

**Standby State (C1 = 1, C2 = 1)**

Both the tip and ring line drive amplifiers are powered down. Internal resistors are connected between tip to ground and ring to V<sub>BAT</sub> to allow loop current detect in an off-hook condition. The loop current and ground key detectors are both active, E0 determines if the detector is gated to the  $\overline{DET}$  output.

**AC Transmission Circuit Stability**

To ensure stability of the AC transmission feedback loop two compensation capacitors C<sub>TC</sub> and C<sub>RC</sub> are required. Figure 20 (Application Circuit) illustrates their use. Recommended value is 2200pF.

**AC-DC Separation Capacitor, C<sub>HP</sub>**

The high pass filter capacitor connected between pins HPT and HPR provides the separation between circuits sensing tip to ring DC conditions and circuits processing AC signals. A 10nf C<sub>HP</sub> will position the low end frequency response 3dB break point at 48Hz. Where:

$$f_{3dB} = \frac{1}{(2 \cdot \pi \cdot R_{HP} \cdot C_{HP})} \quad (EQ. 28)$$

where R<sub>HP</sub> = 330kΩ.

**Thermal Shutdown Protection**

The HC5515's thermal shutdown protection is invoked if a fault condition on the tip or ring causes the temperature of the die to exceed 160°C. If this happens, the SLIC goes into a high impedance state and will remain there until the temperature of the die cools down by about 20°C. The SLIC will return back to its normal operating mode, providing the fault condition has been removed.

**SLIC Operating States**

TABLE 1. LOGIC TRUTH TABLE

E0	C1	C2	SLIC OPERATING STATE	ACTIVE DETECTOR	$\overline{DET}$ OUTPUT
0	0	0	Open Circuit	No Active Detector	Logic Level High
0	0	1	Active	Loop Current Detector	Loop Current Status
0	1	0	Ringing	Ring Trip Detector	Ring Trip Status
0	1	1	Standby	Loop Current Detector	Loop Current Status
1	0	0	Open Circuit	No Active Detector	} Logic Level High
1	0	1	Active	Loop Current Detector	
1	1	0	Ringing	Ring Trip Detector	
1	1	1	Standby	Loop Current Detector	

**Surge Voltage Protection**

The HC5515 must be protected against surge voltages and power crosses. Refer to “Maximum Ratings” TIPX and RINGX terminals for maximum allowable transient tip and ring voltages. The protection circuit shown in Figure 20 utilizes diodes together with a clamping device to protect tip and ring against high voltage transients.

Positive transients on tip or ring are clamped to within a couple of volts above ground via diodes D<sub>1</sub> and D<sub>2</sub>. Under normal operating conditions D<sub>1</sub> and D<sub>2</sub> are reverse biased and out of the circuit.

Negative transients on tip and ring are clamped to within a couple of volts below ground via diodes D<sub>3</sub> and D<sub>4</sub> with the help of a Surgector. The Surgector is required to block conduction through diodes D<sub>3</sub> and D<sub>4</sub> under normal operating conditions and allows negative surges to be returned to system ground.

The fuse resistors (R<sub>F</sub>) serve a dual purpose of being nondestructive power dissipaters during surge and fuses when the line in exposed to a power cross.

**Power-Up Sequence**

The HC5515 has **no** required power-up sequence. This is a result of the Dielectrically Isolated (DI) process used in the fabrication of the part. By using the DI process, care is no longer required to insure that the substrate be kept at the most negative potential as with junction isolated ICs.

**Printed Circuit Board Layout**

Care in the printed circuit board layout is essential for proper operation. All connections to the RSN pin should be made as close to the device pin as possible, to limit the interference that might be injected into the RSN terminal. It is good practice to surround the RSN pin with a ground plane.

The analog and digital grounds should be tied together at the device.

**Notes**

2. **Overload Level (Two-Wire port)** - The overload level is specified at the 2-wire port ( $V_{TRO}$ ) with the signal source at the 4-wire receive port ( $E_{RX}$ ).  $I_{DCMET} = 30\text{mA}$ ,  $R_{SG} = 4\text{k}\Omega$ , increase the amplitude of  $E_{RX}$  until 1% THD is measured at  $V_{TRO}$ . Reference Figure 1.
3. **Longitudinal Impedance** - The longitudinal impedance is computed using the following equations, where TIP and RING voltages are referenced to ground.  $L_{ZT}$ ,  $L_{ZR}$ ,  $V_T$ ,  $V_R$ ,  $A_R$  and  $A_T$  are defined in Figure 2.  
 $(TIP) L_{ZT} = V_T/A_T$ ,  
 $(RING) L_{ZR} = V_R/A_R$ ,  
 where:  $E_L = 1V_{RMS}$  (0Hz to 100Hz).
4. **Longitudinal Current Limit (Off-Hook Active)** - Off-Hook (Active,  $C_1 = 1$ ,  $C_2 = 0$ ) longitudinal current limit is determined by increasing the amplitude of  $E_L$  (Figure 3A) until the 2-wire longitudinal balance drops below 45dB.  $\overline{DET}$  pin remains low (no false detection).
5. **Longitudinal Current Limit (On-Hook Standby)** - On-Hook (Active,  $C_1 = 1$ ,  $C_2 = 1$ ) longitudinal current limit is determined by increasing the amplitude of  $E_L$  (Figure 3B) until the 2-wire longitudinal balance drops below 45dB.  $DET$  pin remains high (no false detection).
6. **Longitudinal to Metallic Balance** - The longitudinal to metallic balance is computed using the following equation:  
 $BLME = 20 \cdot \log (E_L/V_{TR})$ , where:  $E_L$  and  $V_{TR}$  are defined in Figure 4.
7. **Metallic to Longitudinal FCC Part 68, Para 68.310** - The metallic to longitudinal balance is defined in this spec.
8. **Longitudinal to Four-Wire Balance** - The longitudinal to 4-wire balance is computed using the following equation:  
 $BLFE = 20 \cdot \log (E_L/V_{TX})$ ;  $E_L$  and  $V_{TX}$  are defined in Figure 4.
9. **Metallic to Longitudinal Balance** - The metallic to longitudinal balance is computed using the following equation:  
 $BMLE = 20 \cdot \log (E_{TR}/V_L)$ ,  $E_{RX} = 0$ ,  
 where:  $E_{TR}$ ,  $V_L$  and  $E_{RX}$  are defined in Figure 5.
10. **Four-Wire to Longitudinal Balance** - The 4-wire to longitudinal balance is computed using the following equation:  
 $BFLE = 20 \cdot \log (E_{RX}/V_L)$ ,  $E_{TR} = \text{source is removed}$ .  
 where:  $E_{RX}$ ,  $V_L$  and  $E_{TR}$  are defined in Figure 5.
11. **Two-Wire Return Loss** - The 2-wire return loss is computed using the following equation:  
 $r = -20 \cdot \log (2V_M/V_S)$ .  
 where:  $Z_D =$  The desired impedance; e.g., the characteristic impedance of the line, nominally  $600\Omega$ . (Reference Figure 6).
12. **Overload Level (4-Wire port)** - The overload level is specified at the 4-wire transmit port ( $V_{TXO}$ ) with the signal source ( $E_G$ ) at the 2-wire port,  $I_{DCMET} = 23\text{mA}$ ,  $Z_L = 20\text{k}\Omega$ ,  $R_{SG} = 4\text{k}\Omega$  (Reference Figure 7). Increase the amplitude of  $E_G$  until 1% THD is measured at  $V_{TXO}$ . Note that the gain from the 2-wire port to the 4-wire port is equal to 1.
13. **Output Offset Voltage** - The output offset voltage is specified with the following conditions:  $E_G = 0$ ,  $I_{DCMET} = 23\text{mA}$ ,  $Z_L = \infty$  and is measured at  $V_{TX}$ .  $E_G$ ,  $I_{DCMET}$ ,  $V_{TX}$  and  $Z_L$  are defined

in Figure 7. Note:  $I_{DCMET}$  is established with a series  $600\Omega$  resistor between tip and ring.

14. **Two-Wire to Four-Wire (Metallic to  $V_{TX}$ ) Voltage Gain** - The 2-wire to 4-wire (metallic to  $V_{TX}$ ) voltage gain is computed using the following equation.  
 $G_{2-4} = (V_{TX}/V_{TR})$ ,  $E_G = 0\text{dBm0}$ ,  $V_{TX}$ ,  $V_{TR}$ , and  $E_G$  are defined in Figure 7.
15. **Current Gain RSN to Metallic** - The current gain RSN to Metallic is computed using the following equation:  
 $K = I_M [(R_{DC1} + R_{DC2})/(V_{RDC} - V_{RSN})]$   $K$ ,  $I_M$ ,  $R_{DC1}$ ,  $R_{DC2}$ ,  $V_{RDC}$  and  $V_{RSN}$  are defined in Figure 8.
16. **Two-Wire to Four-Wire Frequency Response** - The 2-wire to 4-wire frequency response is measured with respect to  $E_G = 0\text{dBm}$  at 1.0kHz,  $E_{RX} = 0\text{V}$ ,  $I_{DCMET} = 23\text{mA}$ . The frequency response is computed using the following equation:  
 $F_{2-4} = 20 \cdot \log (V_{TX}/V_{TR})$ , vary frequency from 300Hz to 3.4kHz and compare to 1kHz reading.  
 $V_{TX}$ ,  $V_{TR}$ , and  $E_G$  are defined in Figure 9.
17. **Four-Wire to Two-Wire Frequency Response** - The 4-wire to 2-wire frequency response is measured with respect to  $E_{RX} = 0\text{dBm}$  at 1.0kHz,  $E_G = 0\text{V}$ ,  $I_{DCMET} = 23\text{mA}$ . The frequency response is computed using the following equation:  
 $F_{4-2} = 20 \cdot \log (V_{TR}/E_{RX})$ , vary frequency from 300Hz to 3.4kHz and compare to 1kHz reading.  
 $V_{TR}$  and  $E_{RX}$  are defined in Figure 9.
18. **Four-Wire to Four-Wire Frequency Response** - The 4-wire to 4-wire frequency response is measured with respect to  $E_{RX} = 0\text{dBm}$  at 1.0kHz,  $E_G = 0\text{V}$ ,  $I_{DCMET} = 23\text{mA}$ . The frequency response is computed using the following equation:  
 $F_{4-4} = 20 \cdot \log (V_{TX}/E_{RX})$ , vary frequency from 300Hz to 3.4kHz and compare to 1kHz reading.  
 $V_{TX}$  and  $E_{RX}$  are defined in Figure 9.
19. **Two-Wire to Four-Wire Insertion Loss** - The 2-wire to 4-wire insertion loss is measured with respect to  $E_G = 0\text{dBm}$  at 1.0kHz input signal,  $E_{RX} = 0$ ,  $I_{DCMET} = 23\text{mA}$  and is computed using the following equation:  
 $L_{2-4} = 20 \cdot \log (V_{TX}/V_{TR})$   
 where:  $V_{TX}$ ,  $V_{TR}$ , and  $E_G$  are defined in Figure 9. (Note: The fuse resistors,  $R_F$ , impact the insertion loss. The specified insertion loss is for  $R_F = 0$ ).
20. **Four-Wire to Two-Wire Insertion Loss** - The 4-wire to 2-wire insertion loss is measured based upon  $E_{RX} = 0\text{dBm}$ , 1.0kHz input signal,  $E_G = 0$ ,  $I_{DCMET} = 23\text{mA}$  and is computed using the following equation:  
 $L_{4-2} = 20 \cdot \log (V_{TR}/E_{RX})$ ,  
 where:  $V_{TR}$  and  $E_{RX}$  are defined in Figure 9.
21. **Two-Wire to Four-Wire Gain Tracking** - The 2-wire to 4-wire gain tracking is referenced to measurements taken for  $E_G = -10\text{dBm}$ , 1.0kHz signal,  $E_{RX} = 0$ ,  $I_{DCMET} = 23\text{mA}$  and is computed using the following equation.  
 $G_{2-4} = 20 \cdot \log (V_{TX}/V_{TR})$  vary amplitude -40dBm to +3dBm, or -55dBm to -40dBm and compare to -10dBm reading.  
 $V_{TX}$  and  $V_{TR}$  are defined in Figure 9.
22. **Four-Wire to Two-Wire Gain Tracking** - The 4-wire to 2-wire gain tracking is referenced to measurements taken for

$E_{RX} = -10\text{dBm}$ , 1.0kHz signal,  $E_G = 0$ ,  $I_{DCMET} = 23\text{mA}$  and is computed using the following equation:

$G_{4-2} = 20 \cdot \log(V_{TR}/E_{RX})$  vary amplitude -40dBm to +3dBm, or -55dBm to -40dBm and compare to -10dBm reading.

$V_{TR}$  and  $E_{RX}$  are defined in Figure 9. The level is specified at the 4-wire receive port and referenced to a 600Ω impedance level.

**23. Two-Wire Idle Channel Noise** - The 2-wire idle channel noise at  $V_{TX}$  is specified with the 2-wire port terminated in 600Ω ( $R_L$ ) and with the 4-wire receive port grounded (Reference Figure 10).

**24. Four-Wire Idle Channel Noise** - The 4-wire idle channel noise at  $V_{TX}$  is specified with the 2-wire port terminated in 600Ω ( $R_L$ ). The noise specification is with respect to a 600Ω impedance level at  $V_{TX}$ . The 4-wire receive port is grounded (Reference Figure 10).

**25. Harmonic Distortion (2-Wire to 4-Wire)** - The harmonic distortion is measured with the following conditions.  $E_G = 0\text{dBm}$

at 1kHz,  $I_{DCMET} = 23\text{mA}$ . Measurement taken at  $V_{TX}$ . (Reference Figure 7).

**26. Harmonic Distortion (4-Wire to 2-Wire)** - The harmonic distortion is measured with the following conditions.  $E_{RX} = 0\text{dBm}$ . Vary frequency between 300Hz and 3.4kHz,  $I_{DCMET} = 23\text{mA}$ . Measurement taken at  $V_{TR}$ . (Reference Figure 9).

**27. Constant Loop Current** - The constant loop current is calculated using the following equation:

$$I_L = 2500 / (R_{DC1} + R_{DC2}).$$

**28. Standby State Loop Current** - The standby state loop current is calculated using the following equation:

$$I_L = [|V_{BAT}| - 3] / [R_L + 1800], T_A = 25^\circ\text{C}.$$

**29. Power Supply Rejection Ratio** - Inject a 100mV<sub>RMS</sub> signal (50Hz to 4kHz) on  $V_{BAT}$ ,  $V_{CC}$  and  $V_{EE}$  supplies. PSRR is computed using the following equation:

$$\text{PSRR} = 20 \cdot \log(V_{TX}/V_{IN}). V_{TX} \text{ and } V_{IN} \text{ are defined in Figure 11.}$$

### Pin Descriptions

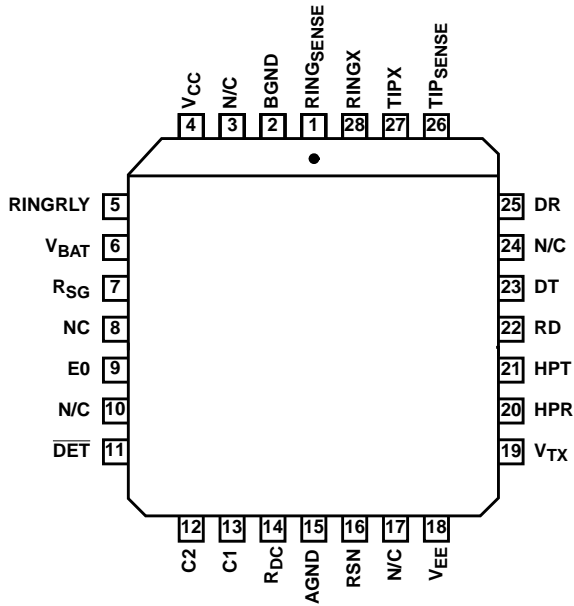
PLCC	PDIP	SYMBOL	DESCRIPTION
1		RINGSENSE	Internally connected to output of RING power amplifier.
2	7	BGND	Battery Ground - To be connected to zero potential. All loop current and longitudinal current flow from this ground. Internally separate from AGND but it is recommended that it is connected to the same potential as AGND.
4	8	V <sub>CC</sub>	+5V power supply.
5	9	RINGRLY	Ring relay driver output.
6	10	V <sub>BAT</sub>	Battery supply voltage, -24V to -56V.
7	11	R <sub>SG</sub>	Saturation guard programming resistor pin.
8	12	NC	This pin is used during manufacturing. This pin is to be left open for proper SLIC operation .
9	13	E0	TTL compatible logic input. Enables the $\overline{\text{DET}}$ output when set to logic level zero and disables $\overline{\text{DET}}$ output when set to a logic level one.
11	14	$\overline{\text{DET}}$	Detector output. TTL compatible logic output. A zero logic level indicates that the selected detector was triggered (see Truth Table for selection of Ground Key detector, Loop Current detector or the Ring Trip detector). The $\overline{\text{DET}}$ output is an open collector with an internal pull-up of approximately 15kΩ to V <sub>CC</sub> .
12	15	C2	TTL compatible logic input. The logic states of C1 and C2 determine the operating states (Open Circuit, Active, Ringing or Standby) of the SLIC.
13	16	C1	TTL compatible logic input. The logic states of C1 and C2 determine the operating states (Open Circuit, Active, Ringing or Standby) of the SLIC.
14	17	R <sub>DC</sub>	DC feed current programming resistor pin. Constant current feed is programmed by resistors R <sub>DC1</sub> and R <sub>DC2</sub> connected in series from this pin to the receive summing node (RSN). The resistor junction point is decoupled to AGND to isolate the AC signal components.
15	18	AGND	Analog ground.
16	19	RSN	Receive Summing Node. The AC and DC current flowing into this pin establishes the metallic loop current that flows between tip and ring. The magnitude of the metallic loop current is 1000 times greater than the current into the RSN pin. The constant current programming resistors and the networks for program receive gain and 2-wire impedance all connect to this pin.
18	20	V <sub>EE</sub>	-5V power supply.
19	21	V <sub>TX</sub>	Transmit audio output. This output is equivalent to the TIP to RING metallic voltage. The network for programming the 2-wire input impedance connects between this pin and RSN.

**Pin Descriptions** (Continued)

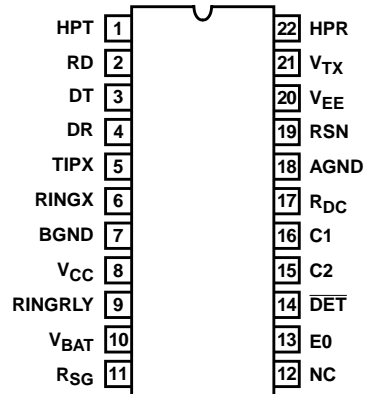
PLCC	PDIP	SYMBOL	DESCRIPTION
20	22	HPR	RING side of AC/DC separation capacitor $C_{HP}$ . $C_{HP}$ is required to properly separate the ring AC current from the DC loop current. The other end of $C_{HP}$ is connected to HPT.
21	1	HPT	TIP side of AC/DC separation capacitor $C_{HP}$ . $C_{HP}$ is required to properly separate the tip AC current from the DC loop current. The other end of $C_{HP}$ is connected to HPR.
22	2	RD	Loop current programming resistor. Resistor $R_D$ sets the trigger level for the loop current detect circuit. A filter capacitor $C_D$ is also connected between this pin and $V_{EE}$ .
23	3	DT	Input to ring trip comparator. Ring trip detection is accomplished by connecting an external network to a comparator in the SLIC with inputs DT and DR.
25	4	DR	Input to ring trip comparator. Ring trip detection is accomplished by connecting an external network to a comparator in the SLIC with inputs DT and DR.
26		TIPSENSE	Internally connected to output of tip power amplifier.
27	5	TIPX	Output of tip power amplifier.
28	6	RINGX	Output of ring power amplifier.
3, 10 17, 24		N/C	No internal connection.

**Pinouts**

HC5515  
(PLCC)  
TOP VIEW

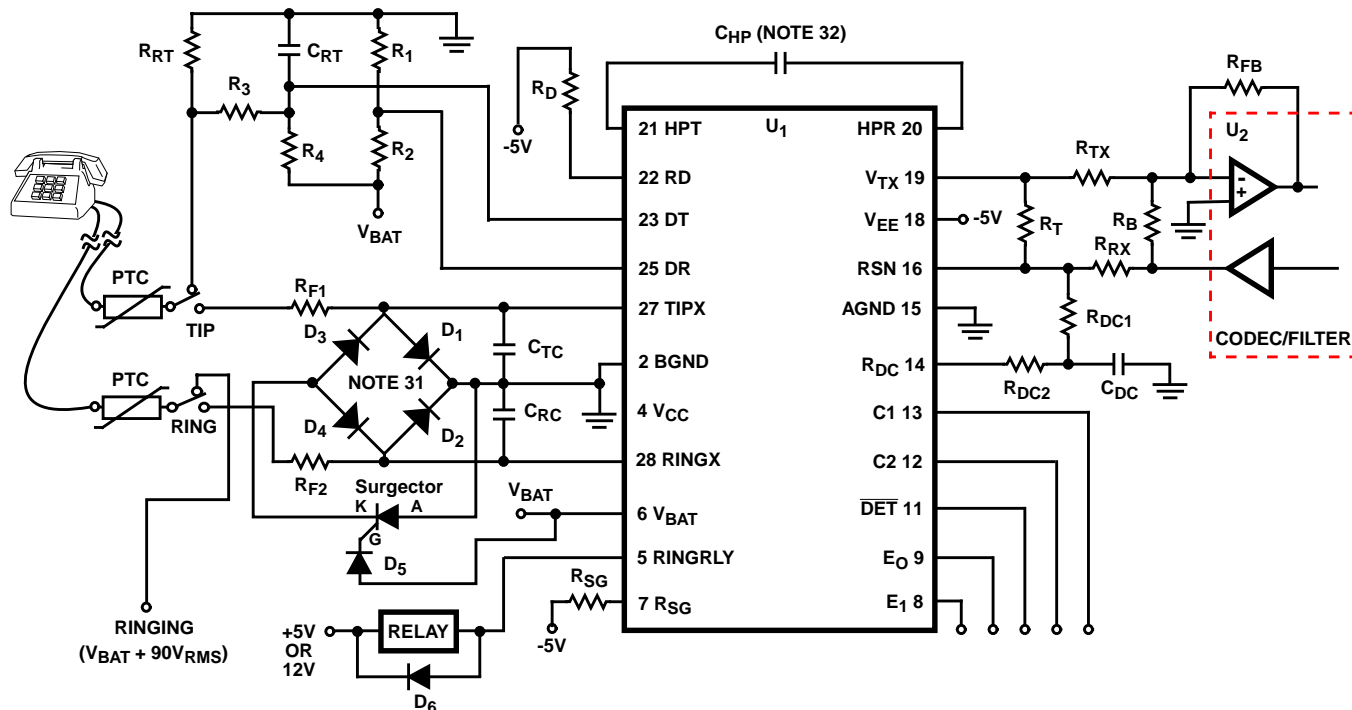


HC5515  
(PDIP)  
TOP VIEW





Application Circuit



- |                                   |   |                                     |   |
|-----------------------------------|---|-------------------------------------|---|
| U1                                | SLIC (Subscriber Line Interface Circuit)<br>HC5515                                      | R <sub>1</sub> , R <sub>3</sub>     | 200kΩ, 5%, 1/4W   |
| U2                                | Combination CODEC/Filter e.g.<br>CD22354A or Programmable CODEC/<br>Filter, e.g. SLAC   | R <sub>2</sub>                      | 910kΩ, 5%, 1/4W   |
| C <sub>DC</sub>                   | 1.5μF, 20%, 10V   | R <sub>4</sub>                      | 1.2MΩ, 5%, 1/4W   |
| C <sub>HP</sub>                   | 10nF, 20%, 100V (Note 2)  | R <sub>B</sub>                      | 18.7kΩ, 1%, 1/4W  |
| C <sub>RT</sub>                   | 0.39μF, 20%, 100V   | R <sub>D</sub>                      | 39kΩ, 5%, 1/4W  |
| C <sub>TC</sub> , C <sub>RC</sub> | 2200pF, 20%, 100V   | R <sub>DC1</sub> , R <sub>DC2</sub> | 41.2kΩ, 5%, 1/4W  |
| Relay                             | Relay, 2C Contacts, 5V or 12V Coil  | R <sub>FB</sub>                     | 20.0kΩ, 1%, 1/4W  |
| D <sub>1</sub> - D <sub>5</sub>   | 1N4007 Diode  | R <sub>RX</sub>                     | 280kΩ, 1%, 1/4W   |
| Surgeprot                         | SGT27S10  | R <sub>T</sub>                      | 562kΩ, 1%, 1/4W   |
| PTC                               | Polyswitch TR600-150  | R <sub>TX</sub>                     | 20kΩ, 1%, 1/4W  |
| D <sub>6</sub>                    | Diode, 1N4454   | R <sub>RT</sub>                     | 150Ω, 5%, 2W  |
| R <sub>F1</sub> , R <sub>F2</sub> | Line Resistor, 20Ω, 1% Match, 2 W<br>Carbon column resistor or thick film on<br>ceramic | R <sub>SG</sub>                     | V <sub>BAT</sub> = -28V, R <sub>SG</sub> = ∞<br>V <sub>BAT</sub> = -48V, R <sub>SG</sub> = 4.0kΩ, 1/4W 5% |

NOTES:

30. It is recommended that the anodes of D<sub>3</sub> and D<sub>4</sub> be shorted to ground through a battery referenced surgeprot (SGT27S10).  
 31. To meet the specified 25dB 2-wire return loss at 200Hz, C<sub>HP</sub> needs to be 20nF, 20%, 100V.

FIGURE 20. APPLICATION CIRCUIT

All Intersil semiconductor products are manufactured, assembled and tested under ISO9000 quality systems certification.

Intersil semiconductor products are sold by description only. Intersil Corporation reserves the right to make changes in circuit design and/or specifications at any time without notice. Accordingly, the reader is cautioned to verify that data sheets are current before placing orders. Information furnished by Intersil is believed to be accurate and reliable. However, no responsibility is assumed by Intersil or its subsidiaries for its use; nor for any infringements of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of Intersil or its subsidiaries.

For information regarding Intersil Corporation and its products, see web site <http://www.intersil.com>