NEC

MOS INTEGRATED CIRCUIT
μPD75P218

4-BIT SINGLE-CHIP MICROCOMPUTER

The μPD75P218 is a one-time PROM version that can be written to only once or an EPROM version that allows program writing, erasing, and rewriting, of the μPD75218 **Note**.

Since the program can be written by the user, the μPD75P218 is suitable for preproduction use during system development, or limited production.

Read this material together with the μPD75218 materials.

Note Under development

FEATURES

- μPD75218 compatible
- On-chip 16K-byte mode/32K-byte mode switching function
- Operates at the same power supply voltage range (2.7 to 6.0 V) as the mask ROM version μPD75218.
- 32640 × 8 bits of PROM
- 1024 × 4 bits of RAM
- No pull-down resistor for Port 6
- High breakdown voltage display output
  - S0 to S8, T0 to T9 : On-chip pull-down resistor
  - S9, T10 to T15 : Open drain
- No power-on reset circuit

Caution No mask-option pull-down resistor is provided.

ORDERING INFORMATION

Part Number	Package	Quality Grade
μPD75P218CW	64-pin plastic shrink DIP (750 mil)	Standard
μPD75P218GF-3BR	64-pin plastic QFP (14 × 20 mm)	Standard
μPD75P218KB	64-pin ceramic LCC with window (14 × 20 mm)	Standard

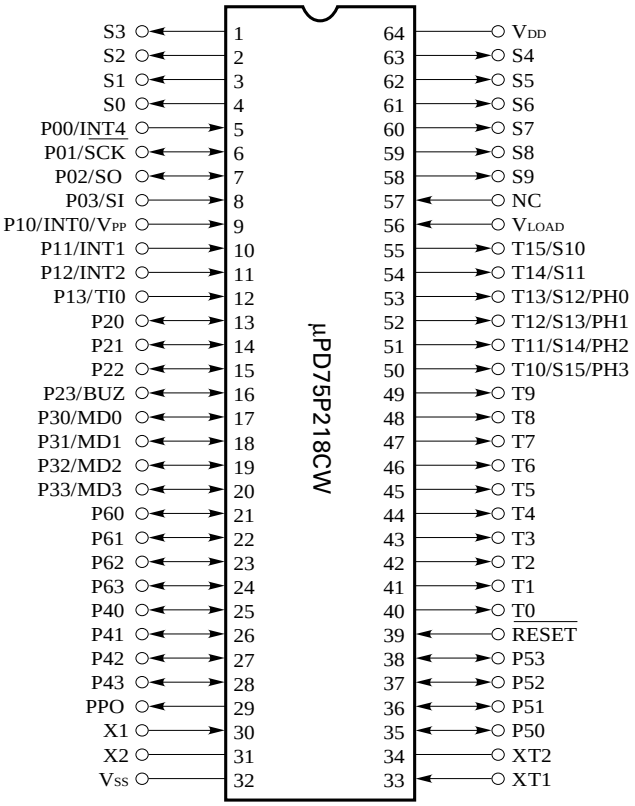
Please refer to "Quality grade on NEC Semiconductor Devices" (Document number IEI-1209) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

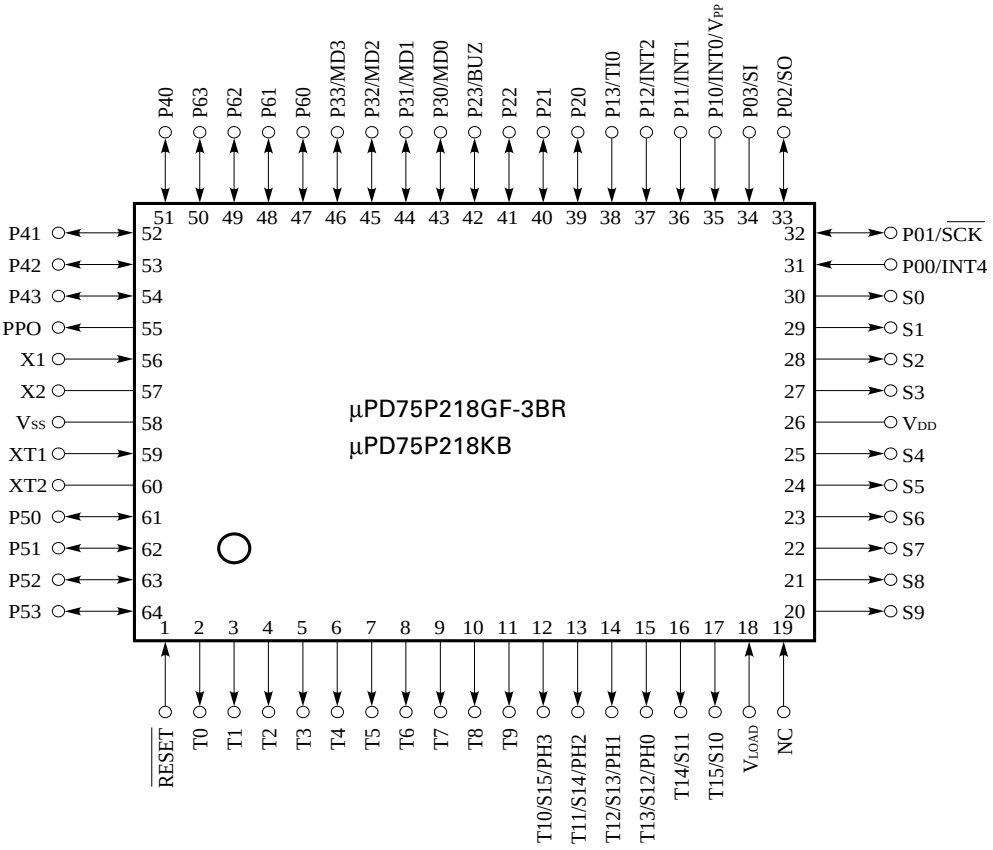
The word "PROM" in this document refers to the common parts of the one-time PROM products and EPROM products.

The information in this document is subject to change without notice.

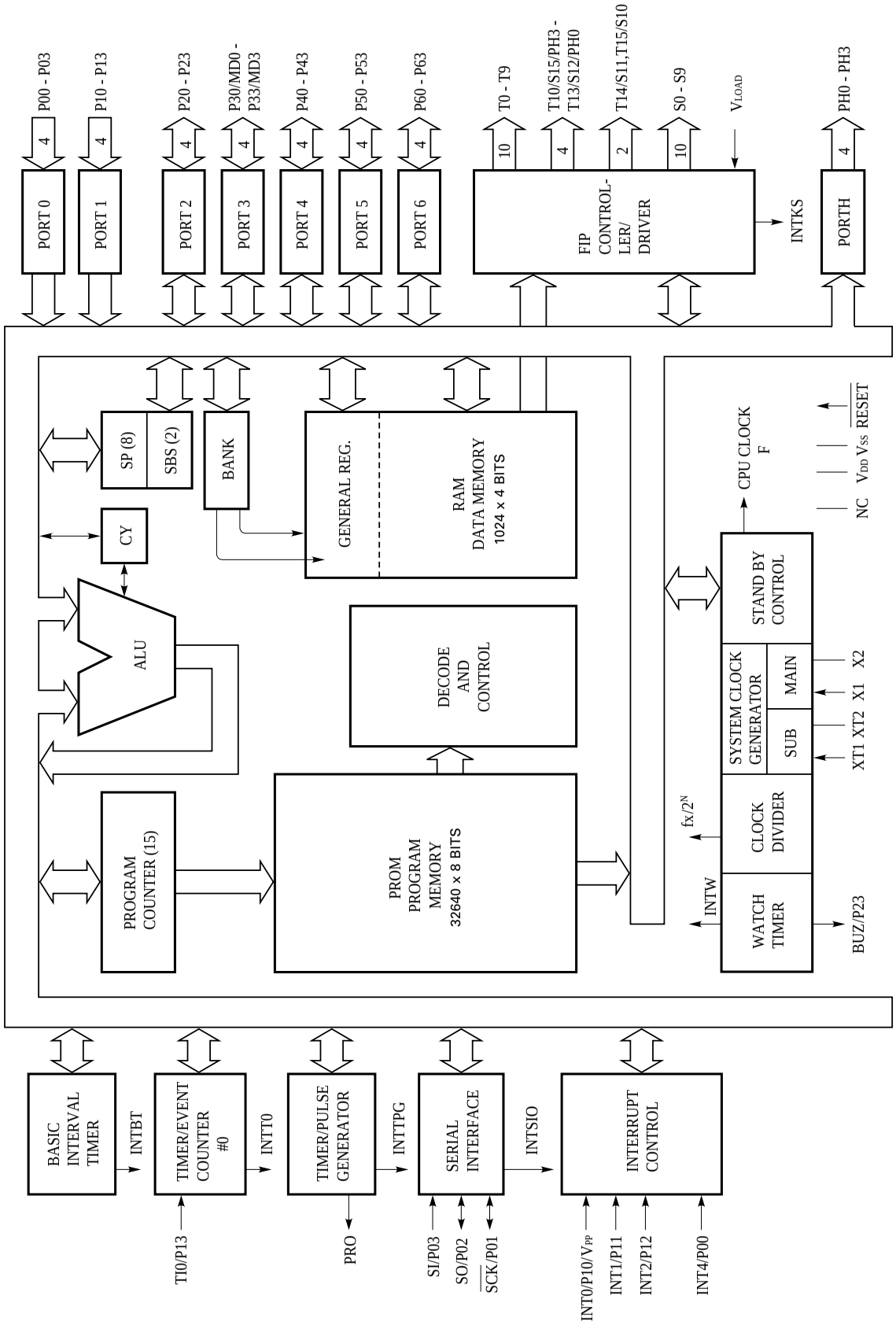
Document No. IC-2541A
(O.D. No. IC-7962A)
Date Published March 1993 P
Printed in Japan

PIN CONFIGURATION (Top View)





BLOCK DIAGRAM



1. PIN FUNCTIONS

1.1 PORT PINS

Pin name	Input/ output	Shared pin	Function		8-bit I/O	When reset
P00	Input	INT4	4-bit input port (PORT0).		×	Input
P01	I/O	$\overline{SCK}$				
P02	I/O	SO				
P03	Input	SI				
P10	Input	INT0/V_{PP}	4-bit input port (PORT1).	With noise elimination function		Input
P11		INT1				
P12		INT2				
P13		TI0				
P20	I/O	–	4-bit I/O port (PORT2).		×	Input
P21		–				
P22		–				
P23		BUZ				
P30 - P33	I/O	MD0 - MD3	Programmable 4-bit I/O port (PORT3). I/O can be specified bit by bit.			Input
P40 - P43	I/O	–	4-bit I/O port (PORT4). Can directly drive LEDs.	Data input/output pins for the PROM write and verify (Four low-order bits).	○	Input
P50 - P53	I/O	–	4-bit I/O port (PORT5). Can directly drive LEDs.	Data input/output pins for the PROM write and verify (Four high-order bits).		Input
P60 - P63	I/O	–	Programmable 4-bit I/O port (PORT6). I/O can be specified bit by bit. Suitable for key input.		×	Input
PH0	Output	T13/S12	4-bit P-ch open drain high breakdown voltage large current output port (PORTH). Can directly drive LEDs.		×	High impedance
PH1		T12/S13				
PH2		T11/S14				
PH3		T10/S15				

1.2 NON-PORT PINS

Pin name	Input/ output	Shared pin	Function		When reset
T0 - T9		–	**Note 1**	High breakdown voltage large current output pin for digit output	Low level
T10/S15 - T13/S12	Output	PH3 - PH0	**Note 2**	High breakdown voltage large current output pin for digit/segment output The remainder of the pins can be used as PORTH.	High impedance
T14/S11, T15/S10		–		High breakdown voltage large current output pin for digit/segment output Static output is also available.	
S9				High breakdown voltage output pin for segment output Static output is also available.	
S0 - S8			**Note 1**	High breakdown voltage output pin for segment output	Low level
PPO	Output	–	Output for receiving pulse signal for timer/pulse generator		High impedance
TI0	Input	P13	Input for receiving external event pulse signal for timer/ event counter		
$\overline{SCK}$	I/O	P01	Serial clock I/O		Input
SO	I/O	P02	Serial data output or serial data I/O		Input
SI	Input	P03	Serial data input or normal input		Input
INT4	Input	P00	Edge detection vectored interrupt input (either rising edge or falling edge detection)		
INT0	Input	P10/V_{PP}	Edge detection vectored interrupt input with noise elimination (detection edge selectable)		
INT1		P11			
INT2	Input	P12	Edge detection testable input (rising edge detection)		
BUZ	I/O	P23	Fixed frequency output pin (for buzzer or system clock trimming)		Input
X1, X2		–	Crystal/ceramic resonator connection for main system clock generation. When external clock is used, it is applied to X1, and its reserve phase signal is applied to X2.		
XT1, XT2		–	Crystal connection for subsystem clock generation. When external clock is used, it is applied to XT1, and XT2 is open.		
$\overline{RESET}$	Input	–	System reset input (low level active)		
MD0 - MD3	I/O	P30 - P33	Operation mode selection pins during the PROM write/verify cycles		
V_{PP}		P10/INT0	+12.5 V is applied as the programming voltage during the PROM write/verify cycles		
V_{LOAD}		–	Pull-down resistor connection pin of FIP® controller/driver		
V_{DD}		–	Positive power supply. +6 V is applied as the programming voltage during the PROM write/verify cycles		
V_{SS}		–	GND potential		
NC **Note 3**		–	No connection		

Note 1. On-chip pull-down resistor

2. Open drain output

3. When using a printed board with a μPD75216A, 75217, or 75218, connect the NC pin to the V_{PRE}.

1.3 PIN INPUT/OUTPUT CIRCUITS

The input/output circuit diagram for each μPD75P218 pin is shown in Fig. 1-1 in a simplified manner.

For the correspondence of the each pin and input/output type number, refer to Table 1-1.

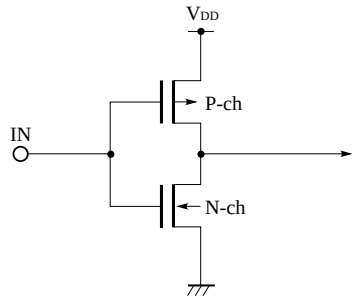
Table 1-1 Pins and Input/Output Type Numbers

Pin name	I/O type	Pin name	I/O type
P00/INT4	Ⓑ	P50 - P53	E
P01/$\overline{SCK}$	Ⓕ	P60 - P63	E
P02/SO	Ⓖ	T0 - T9	I-E
P03 - SI	Ⓑ	T10/S15/PH3 - T13/S12/PH0	I-D
P10/INT0/V_{PP}	Ⓑ	T14/S11, T15/S10	I-D
P11/INT1, P12/INT2		S0 - S8	I-E
P13 - TI0		S9	I-D
P20 - P22	E	PPO	D
P23/BUZ		$\overline{RESET}$	Ⓑ
P30/MD0 - P33/MD3	E	V_{LOAD}	I-E
P40 - P43	E		

Remark I/O type enclosed with a circle indicates Schmitt triggered input.

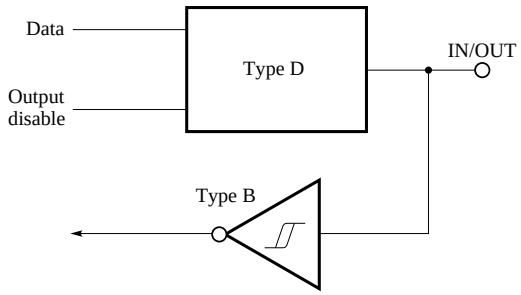
Fig. 1-1 Pin Input/Output Circuit

TYPE A



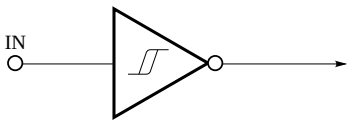
CMOS input buffer

TYPE F



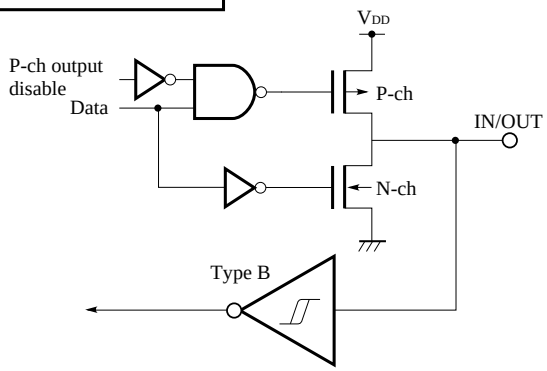
I/O circuit consisting of push-pull output of Type D and Schmitt trigger of Type B

TYPE B



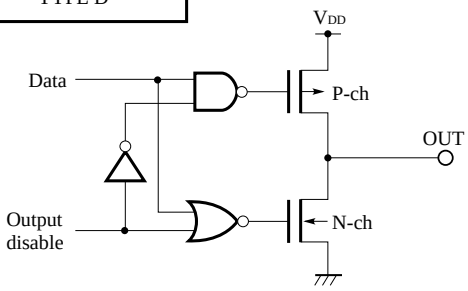
Schmitt trigger input with hysteresis

TYPE G



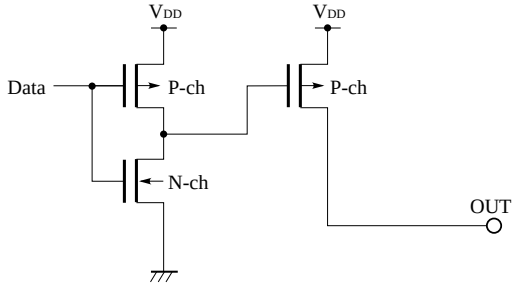
I/O circuit that can switch the push-pull output or N-ch open drain output (off for P-ch)

TYPE D

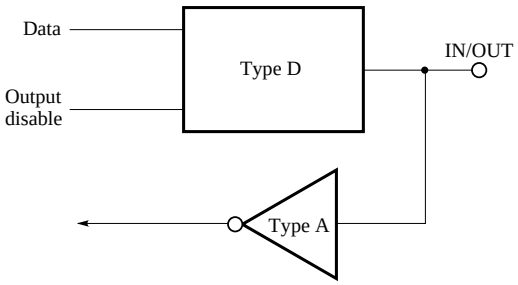


Push-pull output which can be set to high-impedance output (off for both P-ch and N-ch)

TYPE I-D

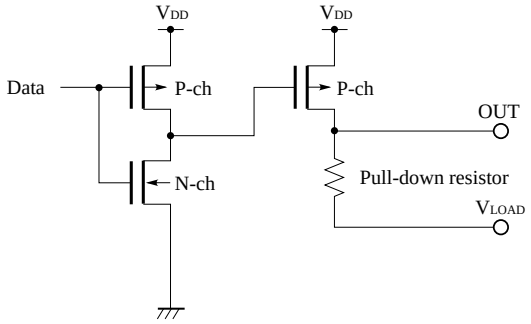


TYPE E



I/O circuit consisting of push-pull output of Type D and input buffer of Type A

TYPE I-E



1.4 PROCESSING OF UNUSED PINS

Table 1-2 Recommended Connection of Unused Pins

Pin name	Recommended connection
P00/INT4	Connect to V_{SS}
P01/$\overline{SCK}$	Connect to V_{SS} or V_{DD}
P02/SO	
P03/SI	
P10/INT0/V_{PP}	Connect to V_{SS}
P11/INT1, P12/INT2	
P13/T10	
P20 - P22	Input state: Connect to V_{SS} or V_{DD}
P23/BUZ	Output state: Open
P30/MD0 - P33/MD3	
P40 - P43	
P50 - P53	
P60 - P63	
PPO	Open
S0 - S9	
T15/S10, T14/S11	
T0 - T9	
T10/S15/PH3 - T13/S12/PH0	
XT1	Connect to V_{SS} or V_{DD}
XT2	Open
V_{LOAD} when no on-chip load resistor	Connect to V_{SS} or V_{DD}

2. DIFFERENCES BETWEEN THE μPD75P218 AND THE μPD75P216A, 75217, 75218

Item \ Part number		μPD75P216A	μPD75217	μPD75218 Note	μPD75P218
ROM		One-time PROM 16K × 8	Mask ROM 24K × 8	Mask ROM 32K × 8	PROM 32K × 8
RAM		512 × 4	768 × 4	1024 × 4	
FIP controller/driver	segments	9 - 16 segments			
	digits	9 - 16 digits			
Pull-down resistors	P60 - P63	Not available	Mask-option		Not available
	S0 - S8, T0 - T9	On-chip	Mask-option		On-chip
	SD9, T10 - T15	Not available (open drain)	Mask-option		Not available (open drain)
Pin connection	P10	INT0/V_{PP} (common use)	INT0 (common use)		INT0/V_{PP} (common use)
	P30 - P33	MD0 - MD3 (common use)	No common use		MD0 - MD3 (common use)
	V_{PRE}	Not available (NC)	Available		Not available (NC)
Operating ambient temperature		–10 to +70 ˚C	–40 to +85 ˚C		–40 to +70 ˚C
Power supply voltage		5 V ± 10 %	2.7 - 6.0 V		
Stack area		Bank 0	Bank 0 - 2	Bank 0 - 3	
16K-byte mode/32K-byte mode switching function		Not available			Available
Package		64-pin plastic shrink DIP	64-pin plastic shrink DIP 64-pin plastic QFP		64-pin plastic shrink DIP 64-pin plastic QFP 64-pin ceramic LCC with window

Note Under development

3. 16K-BYTE MODE/32K-BYTE MODE SWITCHING FUNCTION

16K-byte mode or 32K-byte mode can be selected by setting the stack bank selection register (SBS). The μPD75P218 can then be used to evaluate the μPD75216A, μPD75217, and μPD75218.

3.1 DIFFERENCES BETWEEN 16K-BYTE MODE AND 32K-BYTE MODE

Table 3-1 16K-byte Mode and 32K-byte Mode Differences

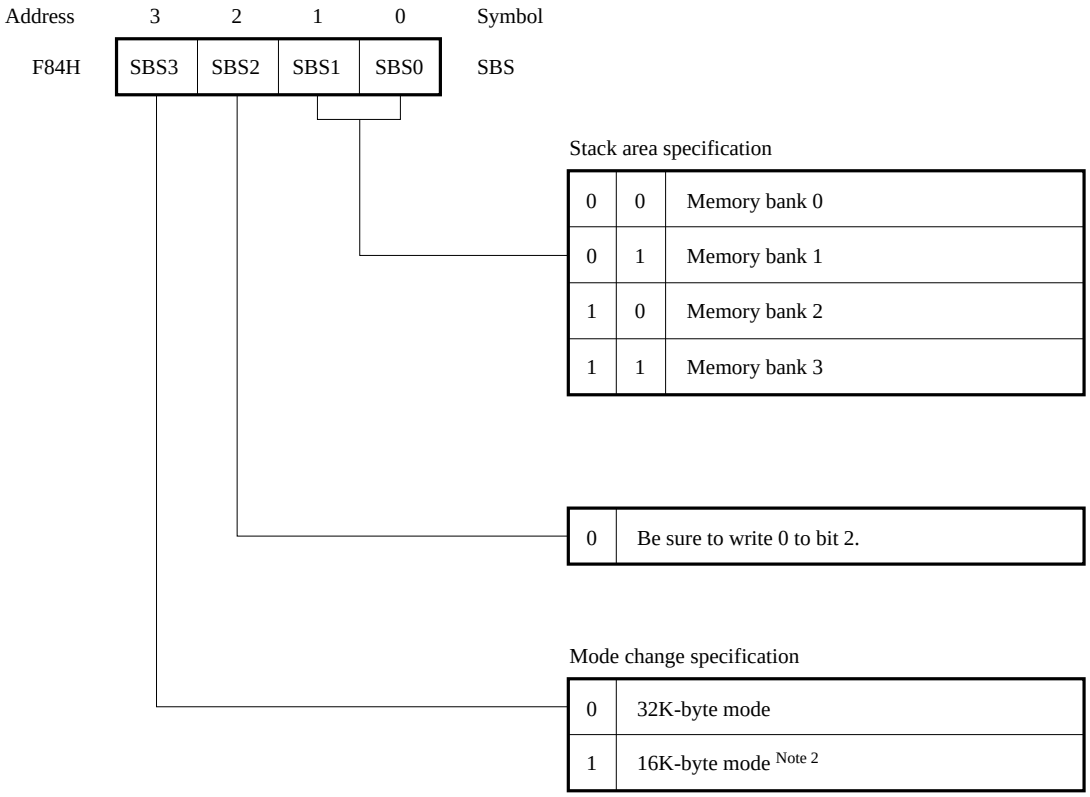
Item	16K-byte Mode	32K-byte Mode
Stack operation at subroutine call instruction execution	2-byte stack	3-byte stack
Stack area	Bank 0	Bank 0 to bank 3
CALL instruction	3 machine cycles	4 machine cycles
TCALL instruction by GETI		
CALLF instruction	2 machine cycles	3 machine cycles
BRA instruction	Undefined operation	Normal operation
CALLA instruction		
Program counter bit 14	0 fixed	Corresponds to branch instruction, call instruction
Corresponding mask ROM version	μPD75216A (S-DIP, QFP)	μPD75217 (S-DIP, QFP) μPD75218 (S-DIP, QFP)

3.2 16K-BYTE MODE AND 32K-BYTE MODE SWITCHING

16K-byte mode and 32K-byte mode are switched by the stack bank selection register. The stack bank selection register format is shown in Fig. 3-1.

The stack bank selection register is set by 4-bit memory manipulation instruction. $\overline{\text{RESET}}$ input sets bit 3 of the stack bank selection register to "1" and changes from 32K-byte mode to 16K-byte mode. When 16K-byte mode is used, manipulating the stack bank selection register is unnecessary. When 32K-byte mode is used, the stack bank selection register must always be initialized to 00××B **Note 1** at the beginning of the program.

Fig. 3-1 Stack Bank Selection Register Format



Caution When using 32K-byte mode, execute a subroutine call instruction and an interrupt enable instruction after the stack bank selection register is set after $\overline{\text{RESET}}$ input.

Notes 1. Set the desired value in ××.

2. When the 16K-byte mode is used after $\overline{\text{RESET}}$ input, the stack bank selection register does not have to be manipulated.

4. PROM (PROGRAM MEMORY) WRITE AND VERIFY

The PROM contained in the μPD75P218 is one-time PROM or EPROM for writing, erasing, and rewriting. Table 4-1 shows the pin functions during the write and verify cycles. Note that it is not necessary to enter an address, because the address is updated by pulsing the X1 clock pins.

Table 4-1 PROM Write and Verify Pin Functions

Pin Name	Function
V_{PP}	Normally 2.7 to 6 V; 12.5 V is applied during the write/verify cycles.
X1, X2	After a write/verify write, the X1 and X2 clock pins are pulsed. The inverted signal of the X1 should be input to the X2. Note that these pins are also pulsed during a read.
MD0 - MD3	Operation mode selection pins during the write/verify cycles
P40 - P43 (Four low-order bits) P50 - P53 (Four high-order bits)	8-bit data input/output pins during the write/verify cycles
V_{DD}	Supply voltage Normally 2.7 to 6 V; 6 V is applied during the write/verify cycles.

Cautions 1. The pins not used for write and verify should be processed as follows.

Port 0 - 2, Port 6, XT1
S0 - S9, T0 - T15 ···· **Connect to GND (directly connectable)**
RESET, PPO, V_{LOAD}

XT2 ····· Open

2. An opaque film should be placed over the UV erase window of the μPD75P218KB except when erasing the EPROM contents.

3. The μPD75P218CW/GF does not have a UV erase window, thus the PROM contents cannot be erased with ultraviolet ray.

4.1 PROM WRITE AND VERIFY OPERATION

When +6 V and +12.5 V are applied to the V_{DD} and V_{PP} pins, respectively, the PROM is placed in the write/verify mode. The operation is selected by the MD0 to MD3 pins, as shown in Table 4-2.

Table 4-2 PROM Write and Verify Operation Mode

Operation Mode Specification						Operation Mode
V_{PP}	V_{DD}	MD0	MD1	MD2	MD3	
+12.5 V	+6 V	H	L	H	L	Clear program memory address to 0
		L	H	H	H	Write mode
		L	L	H	H	Verify mode
		H	×	H	H	Program inhibit

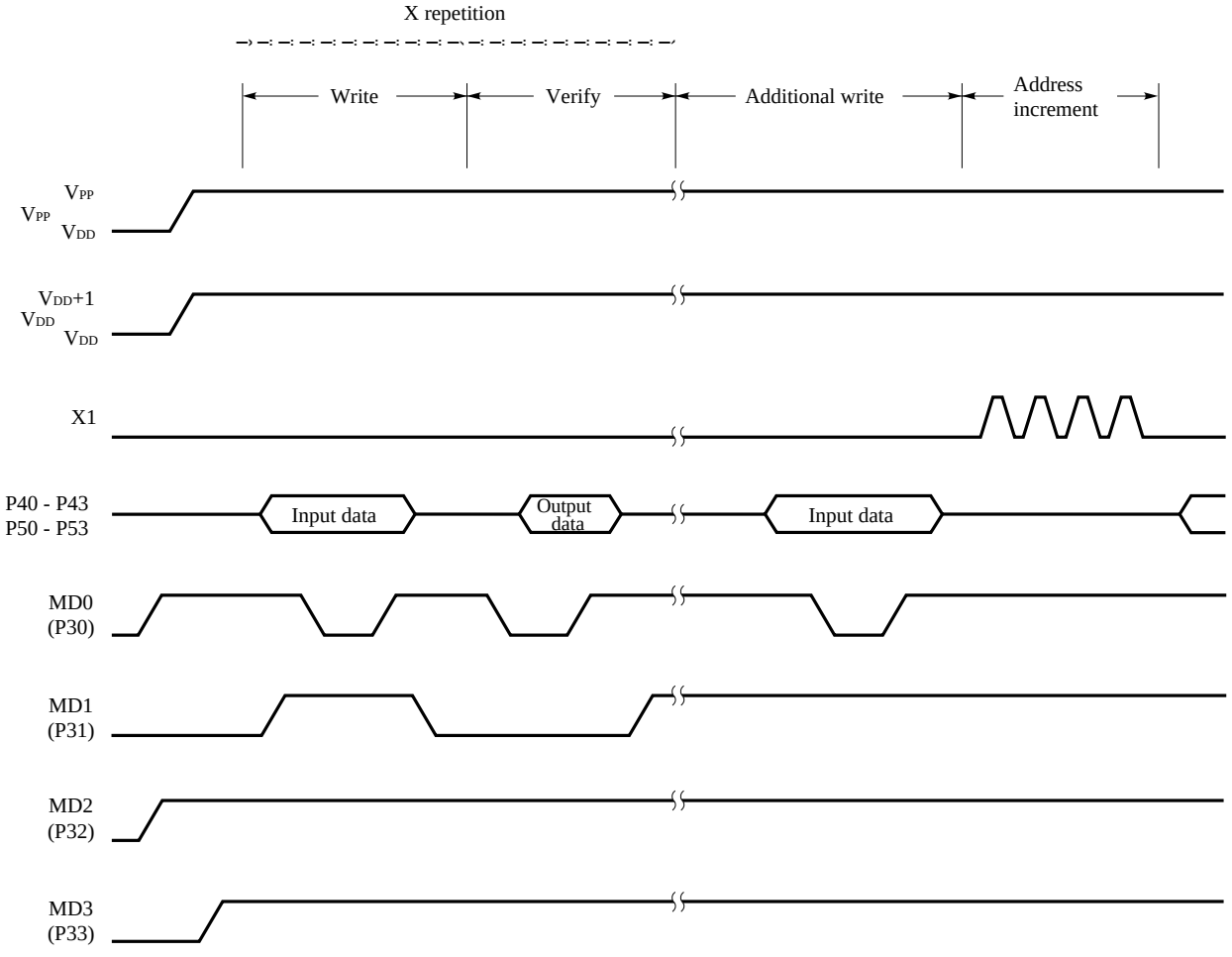
×: Don't care.

4.2 PROM WRITE/VERIFY PROCEDURE

PROMs can be written at high speed using the following procedure: (see the following figure)

(1) Connect unused pins to V_{SS}. Set the X1 pin low.
(2) Supply 5 volts to the V_{DD} and V_{PP} pins.
(3) Wait for 10 μs.
(4) Select the zero clear program memory address mode.
(5) Supply 6 volts to the V_{DD} and 12.5 volts to the V_{PP} pins.
(6) Select the program inhibit mode.
(7) Write data in the 1 ms write mode.
(8) Select the program inhibit mode.
(9) Select the verify mode. If the data is correct, proceed to step (10). If not, repeat steps (7), (8) and (9).
(10) Perform one additional write (duration of 1 ms × number of writes at (7) to (9)).
(11) Select the program inhibit mode.
(12) Apply four pulses to the X1 pin to increment the program memory address by one.
(13) Repeat steps (7) to (12) until the end address is reached.
(14) Select the zero clear program memory address mode.
(15) Return the V_{DD} and V_{PP} pins back to + 5 volts.
(16) Turn off the power.

Fig. 4-1 PROM Write Timing



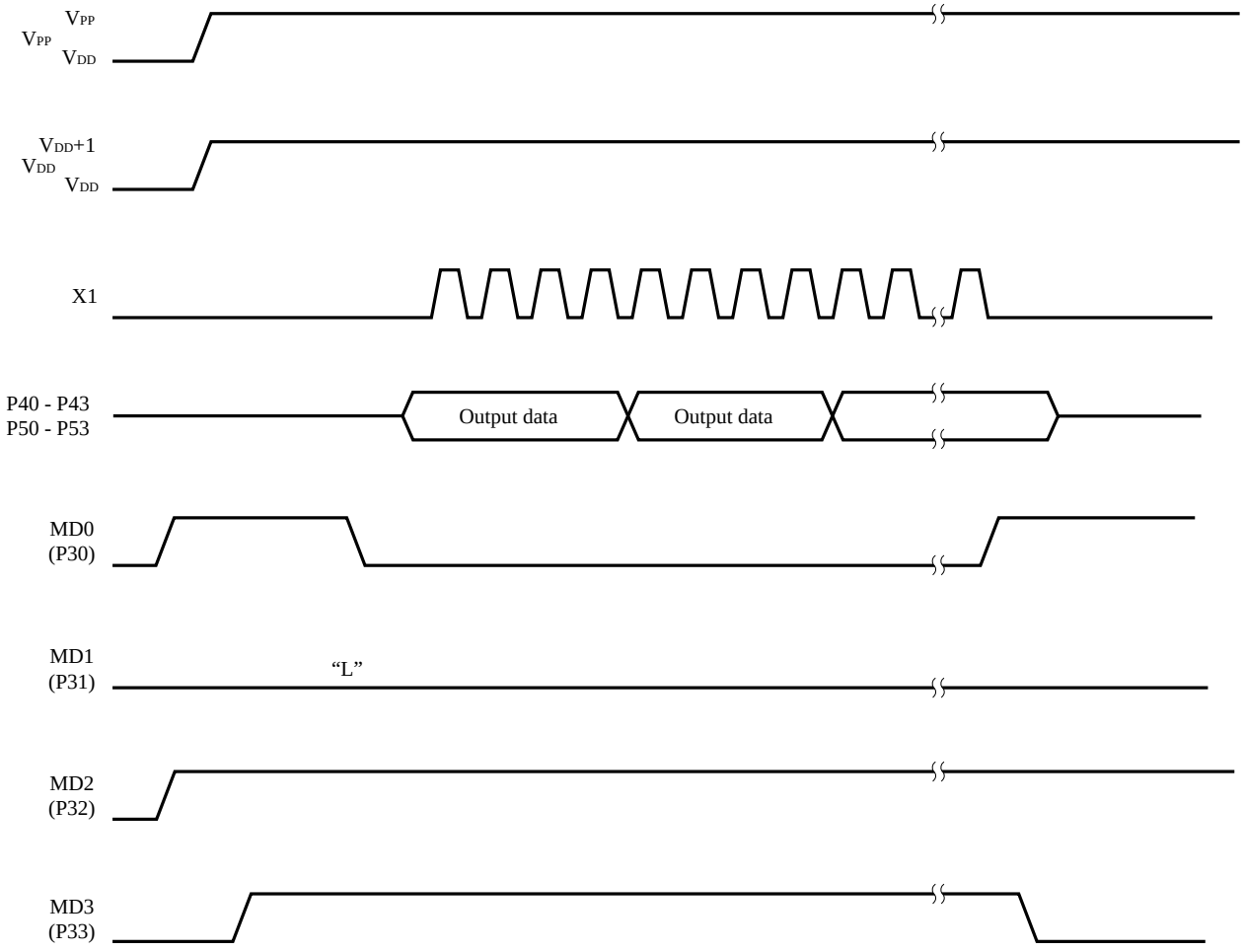
X: number of writes performed at (7) to (9)

4.3 PROM READ PROCEDURE

The PROM contents can be read in the verify mode by using the following procedure: (see the following figure)

(1) Connect unused pins to V_{SS}. Set the X1 pin low.
(2) Supply 5 volts to the V_{DD} and V_{PP} pins.
(3) Wait for 10 μs.
(4) Select the clear program memory address mode.
(5) Supply 6 volts to the V_{DD} and 12.5 volts to the V_{PP} pins.
(6) Select the program inhibit mode.
(7) Select the verify mode. Apply four pulses to the X1 pin. Every four clock pulses will output the data stored in one address.
(8) Select the program inhibit mode.
(9) Select the clear program memory address mode.
(10) Return the V_{DD} and V_{PP} pins back to + 5 volts.
(11) Turn off the power.

Fig. 4-2 PROM Read Timing



4.4 ERASING METHOD

The program data contents of the μPD75P218KB are erased by lighting ultraviolet ray whose wavelength is about 250 nm on the window. The minimum amount of radiation exposure required to erase the contents completely is 15 W·s/cm^2 (ultraviolet ray strength times erase time).

This corresponds to about 15 to 20 minutes when using a UV lamp on the market (wavelength 254 nm, strength 12 mW/cm^2).

Cautions 1. The programmed data contents may also be erased if the uncovered window is exposed to direct sunlight or a fluorescent light even for several hours. Thus, to protect the data contents, cover the window with an opaque film.
NEC attaches quality-tested shading film to the UV EPROM products for shipping.

2. For normal EPROM erase, the distance between the light source and the window should be 2.5 cm or less.

Remark The erase time may be prolonged if the UV lamp is old or if the device window is dirty.

5. ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings (T_a = 25 ˚C)

Parameter	Symbol	Conditions	Ratings	Unit
Power supply voltage	V_{DD}		–0.3 to +7.0	V
	V_{LOAD}		V_{DD} – 40 to V_{DD} + 0.3	V
	V_{PP}		–0.3 to +13.5	V
Input voltage	V_I		–0.3 to V_{DD} + 0.3	V
Output voltage	V_O	Other than display pins	–0.3 to V_{DD} + 0.3	V
	V_{OD}	Display pins	V_{DD} – 40 to V_{DD} + 0.3	V
High-level output current	I_{OH}	Single pin; other than display pins	–15	mA
		Single pin; S0 - S9	–15	mA
		Single pin; T0 - T15	–30	mA
		Total of all pins other than display	–20	mA
		Total of all display pins	–120	mA
Low-level output current	I_{OL}	Single pin	17	mA
		Total of all pins	60	mA
Operating temperature	T_{opt}		–40 to +70	˚C
Storage temperature	T_{stg}		–65 to +150	˚C

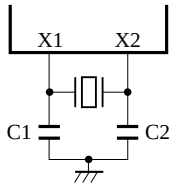
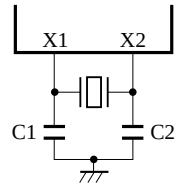
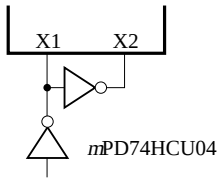
Operating Power Supply Voltage (T_a = –40 to +70 ˚C)

Parameter	Conditions	MIN.	MAX.	Unit
CPU **Note 1**		**Note 2**	6.0	V
Display controller		4.5	6.0	V
Timer/pulse generator		4.5	6.0	V
Other hardwares **Note 1**		2.7	6.0	V

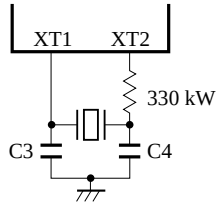
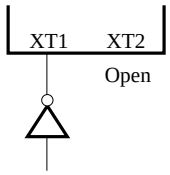
Notes 1. The CPU does not include the system clock oscillator, the display controller, or the timer/pulse generator.

2. Varies according to the cycle time. See AC Characteristics.

Main System Clock Configurations (T_a = –40 to +70 °C, V_{DD} = 2.7 to 6.0 V)

Resonator	Recommended constants	Parameter	Conditions	MIN.	TYP.	MAX.	Unit
Ceramic resonator		Note 1 Oscillation (f_{XX}) frequency	V_{DD} = Oscillator operating voltage range	2.0		6.2	MHz
		Note 2 Oscillation stabilization time	After V_{DD} reaches the minimum oscillator operating voltage range			4	ms
Crystal resonator		Note 1 Oscillation frequency (f_{XX})		2.0	4.19	6.2	MHz
		Note 2 Oscillation stabilization time	V_{DD} = 4.5 to 6.0 V			10	ms
						30	ms
External clock		Note 1 X1 input frequency (f_X)		2.0		6.2	MHz
		X1 input high- and low-level width (t_{XH}, t_{XL})		81		250	ns

Subsystem Clock Configurations (T_a = –40 to +70 °C, V_{DD} = 2.7 to 6.0 V)

Resonator	Recommended constants	Parameter	Conditions	MIN.	TYP.	MAX.	Unit
Crystal resonator		Note 1 Oscillation frequency (f_{XT})		32	32.768	35	kHz
		Note 2 Oscillation stabilization time	V_{DD} = 4.5 to 6.0 V		1.0	2	s
						10	s
External clock		XT1 input frequency (f_{XT})		32		100	kHz
		XT1 input high- and low-level width (t_{XTH}, t_{XTL})		5		15	μs

Notes 1. The oscillator frequency and input frequency indicate only the oscillator characteristics. Refer to the AC Characteristics for the instruction execution time.

2. The oscillation stabilization time is the time required for the oscillation to stabilize after V_{DD} is applied and reaches the V_{DD} spec or after STOP mode is released.

Capacitance (T_a = 25 °C, V_{DD} = 0 V)

Parameter		Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input capacitance		C_{IN}	f = 1 MHz			15	pF
Output capacitance	Other than display output	C_{OUT}	Unmeasured pins returned to 0 V			15	pF
	Display output					35	pF
Input/Output capacitance		C_{IO}				15	pF

Recommended Oscillation Circuit Constants

Main System Clock: Ceramic Resonator (T_a = –40 to +70 °C)

Manufacturer	Part number	Frequency (MHz)	Capacitance (pF)		Oscillation voltage (V)	
			MIN.	MAX.	MIN.	MAX.
Murata	CSA×××MG	2.00 - 2.44	30	30	2.7	6.0
	CST×××MT		On-chip	On-chip		
	CSA×××MG093	2.45 - 3.50	30	30		
	CST×××MGW093		On-chip	On-chip		
	CSA×××MGU	2.51 - 6.00	30	30		
	CST×××MGWU		On-chip	On-chip		
	CSA×××MG	2.45 - 3.50	30	30	3.0	
	CST×××MGW		On-chip	On-chip		
	CSA×××MG	2.51 - 6.00	30	30	3.3	
	CST×××MGW		On-chip	On-chip		
Kyocera	KBR – 2.0MS	2.0	47	47	2.7	6.0
	KBR – 4.0MWS	4.0	33	33		
	KBR – 4.19MWS	4.19				
	KBR – 6.0MWS	6.0				

DC Characteristics (T_a = –40 to +70 °C, V_{DD} = 2.7 to 6.0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
High-level input voltage	V_{IH1}	All except ports 0, 1, 6; X1, X2, XT1, $\overline{RESET}$		0.7V_{DD}		V_{DD}	V
	V_{IH2}	Port 0, 1, $\overline{RESET}$		0.75V_{DD}		V_{DD}	V
	V_{IH3}	X1, X2, XT1		V_{DD} – 0.4		V_{DD}	V
	V_{IH4}	Port 6	V_{DD} = 4.5 to 6.0 V	0.65V_{DD}		V_{DD}	V
				0.7V_{DD}		V_{DD}	V
Low-level input voltage	V_{IL1}	All except ports 0, 1, 6; X1, X2, XT1, $\overline{RESET}$		0		0.3V_{DD}	V
	V_{IL2}	Port 0, 1, 6, $\overline{RESET}$		0		0.2V_{DD}	V
	V_{IL3}	X1, X2, XT1		0		0.4	V
High-level output voltage	V_{OH}	All outputs	V_{DD} = 4.5 to 6.0 V, I_{OH} = –1 mA	V_{DD} – 1.0			V
			I_{OH} = –100 μA	V_{DD} – 0.5			V
Low-level output voltage	V_{OL}	Port 4, 5	V_{DD} = 4.5 to 6.0 V, I_{OL} = 15 mA		0.4	2.0	V
		All outputs	V_{DD} = 4.5 to 6.0 V, I_{OL} = 1.6 mA			0.4	V
			I_{OL} = 400 μA			0.5	V
High-level input leakage current	I_{LIH1}	All except X1, X2, XT1	V_{IN} = V_{DD}			3	μA
	I_{LIH2}	X1, X2, XT1				20	μA
Low-level input leakage current	I_{LIL1}	All except X1, X2, XT1	V_{IN} = 0 V			–3	μA
	I_{LIL2}	X1, X2, XT1				–20	μA
High-level output leakage current	I_{LOH}	All outputs	V_{OUT} = V_{DD}			3	μA
Low-level output leakage current	I_{LOL1}	All except display outputs	V_{OUT} = 0 V			–3	μA
	I_{LOL2}	Display outputs	V_{OUT} = V_{LOAD} = V_{DD} – 35 V			–10	μA
Display output current	I_{OD}	S0-S9	V_{DD} = 4.5 to 6.0 V	–3	–5.5		mA
		T0-T15	V_{OD} = V_{DD} – 2 V	–15	–22		mA
On-chip pull-down resistor	R_L	Display outputs	V_{OD} – V_{LOAD} = 35 V	25	70	135	kΩ
Note 1 Power supply current	I_{DD1}	6.0 MHz crystal oscillator	V_{DD} = 5 V ± 10 % Note 2		6.5	18.0	mA
			V_{DD} = 3 V ± 10 % Note 3		0.85	2.5	mA
	I_{DD2}		HALT mode V_{DD} = 5 V ± 10 %		1350	4000	μA
			HALT mode V_{DD} = 3 V ± 10 %		450	1350	μA
	I_{DD1}	4.19 MHz crystal oscillator C1 = C2 = 15 pF	V_{DD} = 5 V ± 10 % Note 2		4.0	12.0	mA
			V_{DD} = 3 V ± 10 % Note 3		0.55	1.5	mA
	I_{DD2}		HALT mode V_{DD} = 5 V ± 10 %		900	2700	μA
			HALT mode V_{DD} = 3 V ± 10 %		300	900	μA
	I_{DD3}	Note 4	V_{DD} = 3 V ± 10 %		100	300	μA
	I_{DD4}	32kHz crystal oscillator	HALT mode V_{DD} = 3 V ± 10 %		20	60	μA
			STOP mode V_{DD} = 3 V ± 10 %		5	15	μA
	I_{DD5}	XT1 = 0 V STOP mode	V_{DD} = 5 V ± 10 %		0.5	20	μA
			V_{DD} = 3 V ± 10 %		0.1	10	μA

Notes 1. Does not include pull-down resistor current.

2. Value during high-speed operation and when the processor clock control (PCC) register is set to 0011.

3. Value during low-speed operation and when the PCC register is set to 0000.

4. Value when the system clock control register (SCC) is set to 1001, generation of the main system clock pulse is stopped, and the CPU is operated by the subsystem clock pulse.

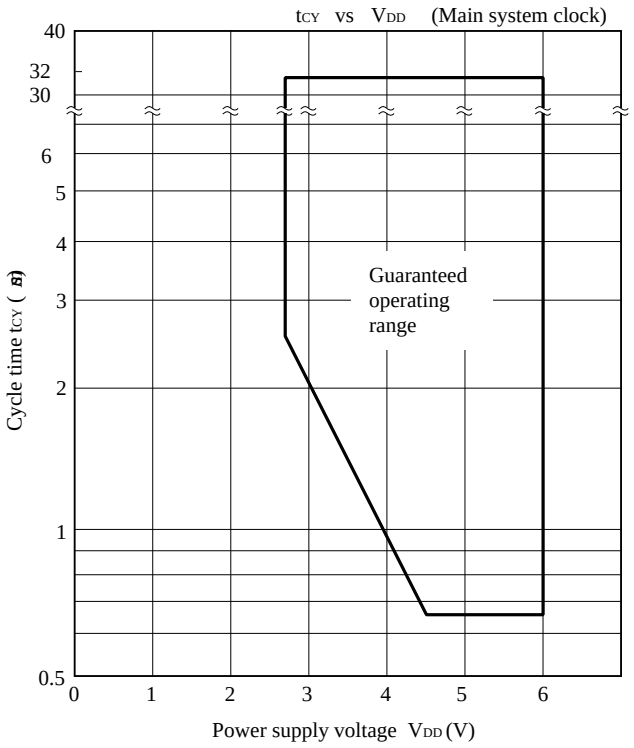
AC Characteristics (T_a = –40 to +70 °C, V_{DD} = 2.7 to 6.0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Note 1 CPU clock cycle time (minimum instruction execution time = 1 machine cycle)	t_{CY}	Main system clock	V_{DD} = 4.5 to 6.0 V	0.67		32	μs
				2.6		32	μs
		Subsystem clock		114	122	125	μs
TI0 input frequency	f_{TI}	V_{DD} = 4.5 to 6.0 V		0		0.6	MHz
				0		165	kHz
TI0 input low- and high-level width	t_{TIH}, t_{TIL}	V_{DD} = 4.5 to 6.0 V		0.83			μs
				3			μs
$\overline{SCK}$ cycle time	t_{KCY}	V_{DD} = 4.5 to 6.0 V	Input	0.8			μs
			Output	0.95			μs
			Input	3.2			μs
			Output	3.8			μs
$\overline{SCK}$ low- and high-level width	t_{KH}, t_{KL}	V_{DD} = 4.5 to 6.0 V	Input	0.4			μs
			Output	t_{KCY}/2–50			ns
			Input	1.6			μs
			Output	t_{KCY}/2–150			ns
SI setup time (to $\overline{SCK}$ ↑)	t_{SIK}			100			ns
SI hold time (from $\overline{SCK}$ ↑)	t_{KSI}			400			ns
$\overline{SCK}$ ↓ → SO output delay time	t_{KSO}	V_{DD} = 4.5 to 6.0 V				300	ns
						1000	ns
Interrupt inputs low- and high-level width	t_{INTH}, t_{INTL}		INT0	**Note 2**			μs
			INT1	$2t_{CY}$			μs
			INT2,4	10			μs
$\overline{RESET}$ low-level width	t_{RSL}			10			μs

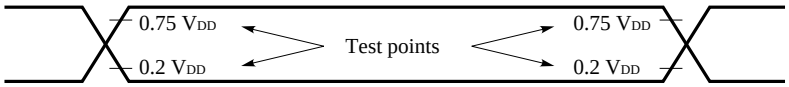
Notes 1. The CPU clock (Φ) cycle time is determined by the oscillator frequency of the connected resonator, the system clock control register (SCC), and the processor clock control register (PCC).

The right chart shows the cycle time t_{CY} characteristics for power supply voltage V_{DD} during the main system clock operation.

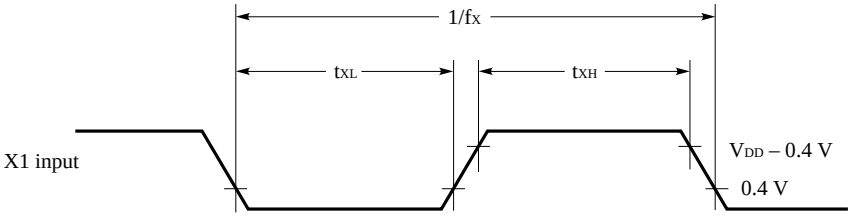
2. $2t_{CY}$ or $128/f_{XX}$, depending on the setting of the interrupt mode register (IM0).

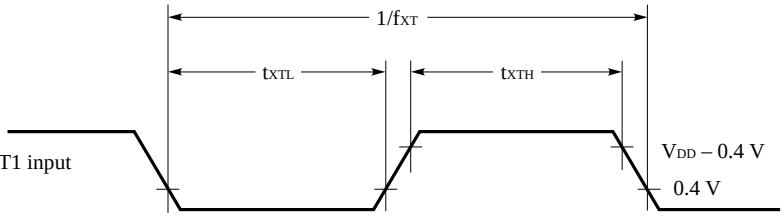


AC Timing Test Points (Except X1, XT1)

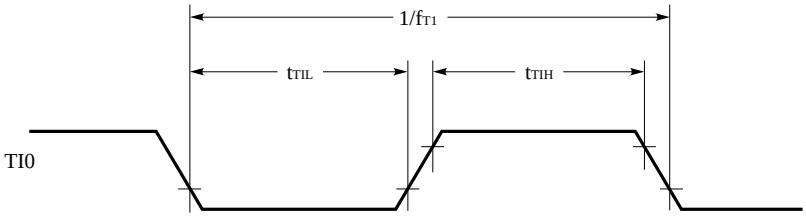


Clock Timing

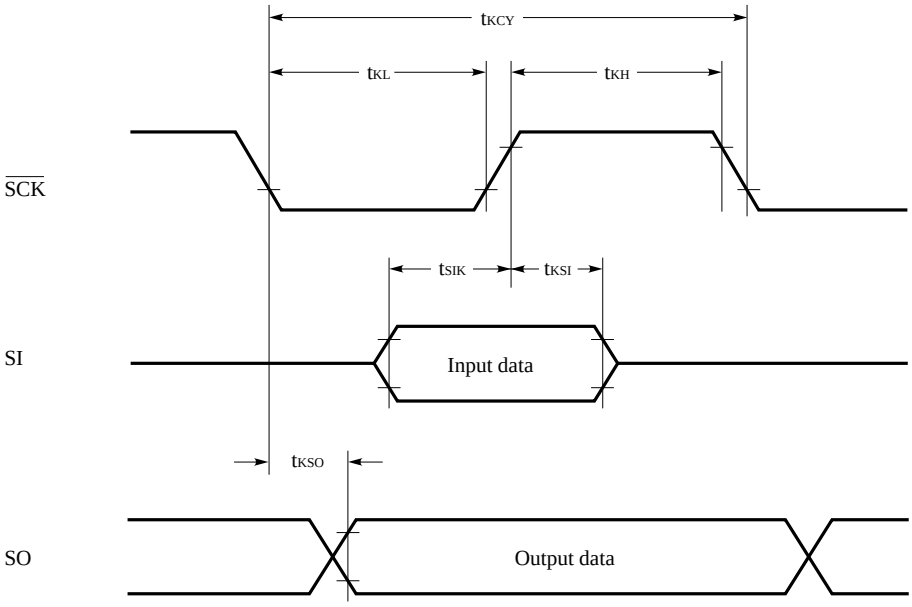




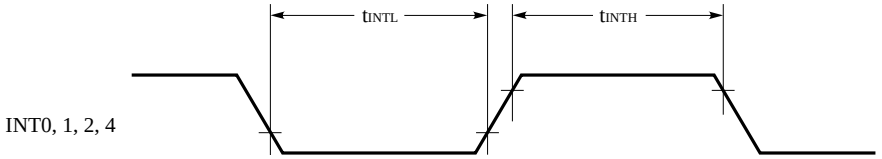
TI0 Timing



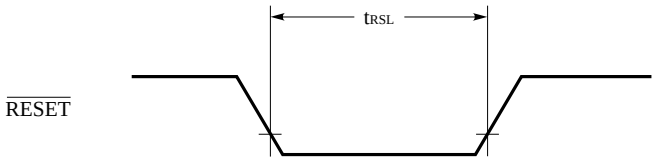
Serial Transfer Timing



Interrupt Input Timing



RESET Input Timing



Data Memory STOP Mode Low Voltage Data Retention Characteristics (T_a = –40 to +70 °C)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data retention voltage	V_{DDDR}		2.0		6.0	V
Data retention current **Note 1**	I_{DDDR}	V_{DDDR} = 2.0 V		0.1	10	μA
Release signal SET time	t_{SREL}		0			μs
Oscillation stabilization time **Note 2**	t_{WAIT}	Release by $\overline{RESET}$ input		$2^{17}/f_x$		ms
		Release by interrupt request		**Note 3**		ms

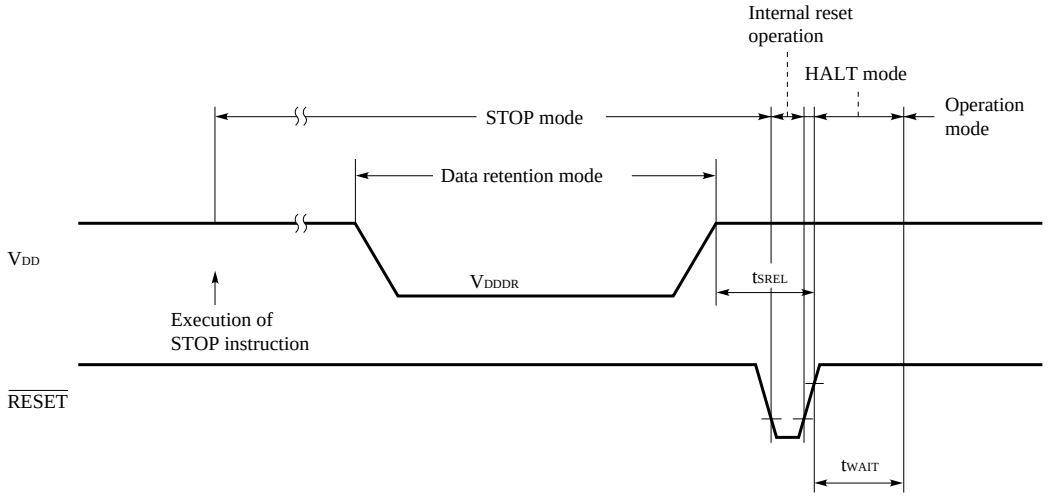
Notes 1. Does not include pull-down resistor current.

2. The oscillation stabilization WAIT time is the time during which the CPU operation is stopped to prevent unstable operation while the oscillation is started.

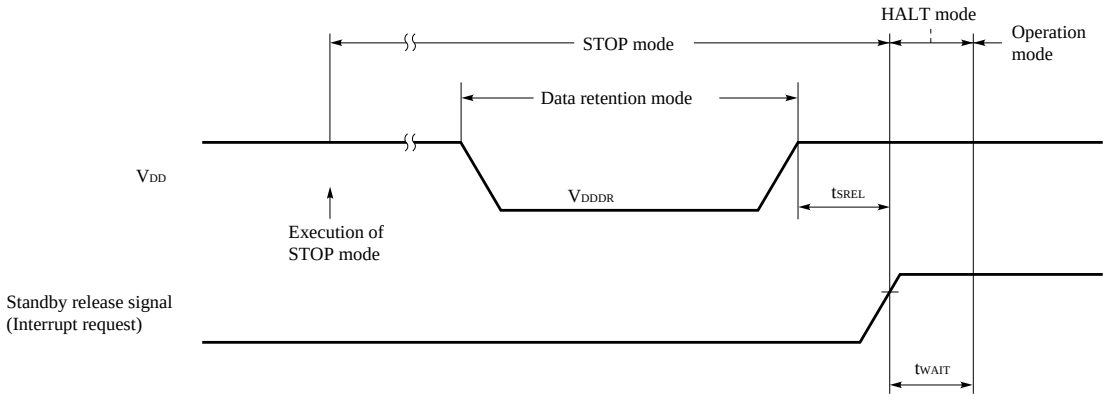
3. The WAIT time depends on the setting of the basic interval timer mode register (BTM) according to the following table.

BTM3	BTM2	BTM1	BTM0	WAIT time	
				(f_{XX} = 6.0 MHz)	(f_{XX} = 4.19 MHz)
–	0	0	0	$2^{20}/f_{XX}$ (approx. 175 ms)	$2^{20}/f_{XX}$ (approx. 250 ms)
–	0	1	1	$2^{17}/f_{XX}$ (approx. 21.8 ms)	$2^{17}/f_{XX}$ (approx. 31.3 ms)
–	1	0	1	$2^{15}/f_{XX}$ (approx. 5.46 ms)	$2^{15}/f_{XX}$ (approx. 7.82 ms)
–	1	1	1	$2^{13}/f_{XX}$ (approx. 1.37 ms)	$2^{13}/f_{XX}$ (approx. 1.95 ms)

Data Retention Timing (STOP mode is released by $\overline{RESET}$ input)



Data Retention Timing (STOP mode is released by interrupt signal)



DC Programming Characteristics (T_a = 25 ± 5 °C, V_{DD} = 6.0 ± 0.25 V, V_{PP} = 12.5 ± 0.3 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
High-level input voltage	V_{IH1}	All except X1, X2	0.7V_{DD}		V_{DD}	V
	V_{IH2}	X1, X2	V_{DD} – 0.5		V_{DD}	V
Low-level input voltage	V_{IL1}	All except X1, X2	0		0.3V_{DD}	V
	V_{IL2}	X1, X2	0		0.4	V
Input leakage current	I_{LI}	V_{IN} = V_{IL} or V_{IH}			10	μA
High-level output voltage	V_{OH}	I_{OH} = –1 mA	V_{DD} – 1.0			V
Low-level output voltage	V_{OL}	I_{OL} = 1.6 mA			0.4	V
V_{DD} power supply current	I_{DD}				30	mA
V_{PP} power supply current	I_{PP}	MD0 = V_{IL}, MD1 = V_{IH}			30	mA

Cautions 1. V_{PP} must not exceed +13.5 V, including overshoot.

2. V_{DD} is to be applied prior to V_{PP} and to be removed after V_{PP} is removed.

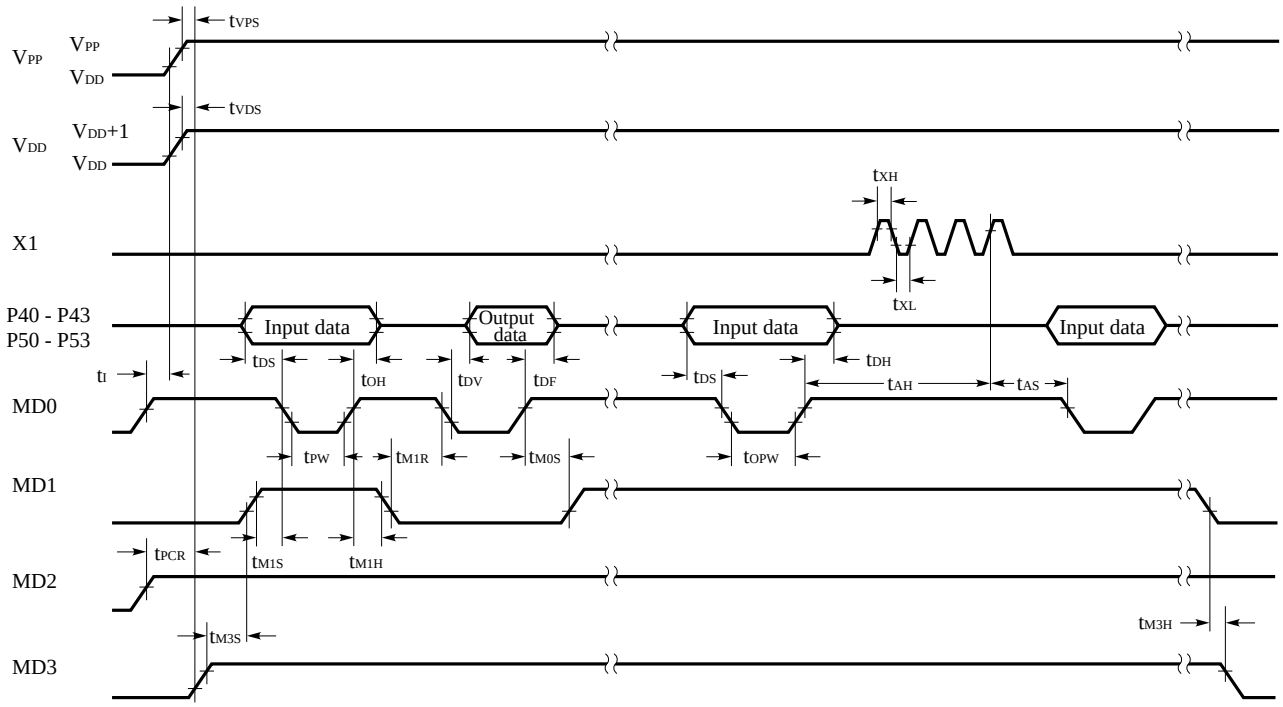
AC Programming Characteristics (T_a = 25 ± 5 °C, V_{DD} = 6.0 ± 0.25 V, V_{PP} = 12.5 ± 0.3 V, V_{SS} = 0 V)

Parameter	Symbol	Note 1	Conditions	MIN.	TYP.	MAX.	Unit
Address setup time Note 2 (to MD0 ↓)	t_{AS}	t_{AS}		2			μs
MD1 setup time (to MD0 ↓)	T_{M1S}	t_{OES}		2			μs
Data setup time (to MD0 ↓)	t_{DS}	t_{DS}		2			μs
Address hold time Note 2 (from MD0 ↑)	T_{AH}	t_{AH}		2			μs
Data hold time (from MD0 ↑)	t_{DH}	t_{DH}		2			μs
MD0 ↑ → data output float delay time	t_{DF}	t_{DF}		0		130	ns
V_{PP} setup time (to MD3 ↑)	t_{VPS}	t_{VPS}		2			μs
V_{DD} setup time (to MD3 ↑)	t_{VDS}	t_{VCS}		2			μs
Initialized program pulse width	t_{PW}	t_{PW}		0.95	1.0	1.05	ms
Additional program pulse width	t_{OPW}	t_{OPW}		0.95		21.0	ms
MD0 setup time (to MD1 ↑)	t_{M0S}	t_{CES}		2			μs
MD0 ↓ → data output delay time	t_{DV}	t_{DV}	MD0 = MD1 = V_{IL}			1	μs
MD1 hold time (to MD0 ↑)	t_{M1H}	t_{OEH}	t_{M1H} + t_{M1R} ≥ 50 μs	2			μs
MD1 recovery time (from MD0 ↓)	t_{M1R}	t_{OR}		2			μs
Program counter reset time	t_{PCR}	–		10			μs
X1 input low- and high-level width	t_{XH}, t_{XL}	–		0.125			μs
X1 input frequency	f_X	–				4.19	MHz
Initial mode set time	t_I	–		2			μs
MD3 setup time (to MD1 ↑)	t_{M3S}	–		2			μs
MD3 hold time (from MD1 ↓)	t_{M3H}	–		2			μs
MD3 setup time (to MD0 ↓)	t_{M3SR}	–	During program read cycle	2			μs
Address Note 2 → Data output delay time	t_{DAD}	t_{ACC}	During program read cycle	2			μs
Address Note 2 → Data output hold time	t_{HAD}	t_{OH}	During program read cycle	0		130	ns
MD3 hold time (from MD0 ↑)	t_{M3HR}	–	During program read cycle	2			μs
MD3 ↓ → Data output float delay time	t_{DFR}	–	During program read cycle	2			μs

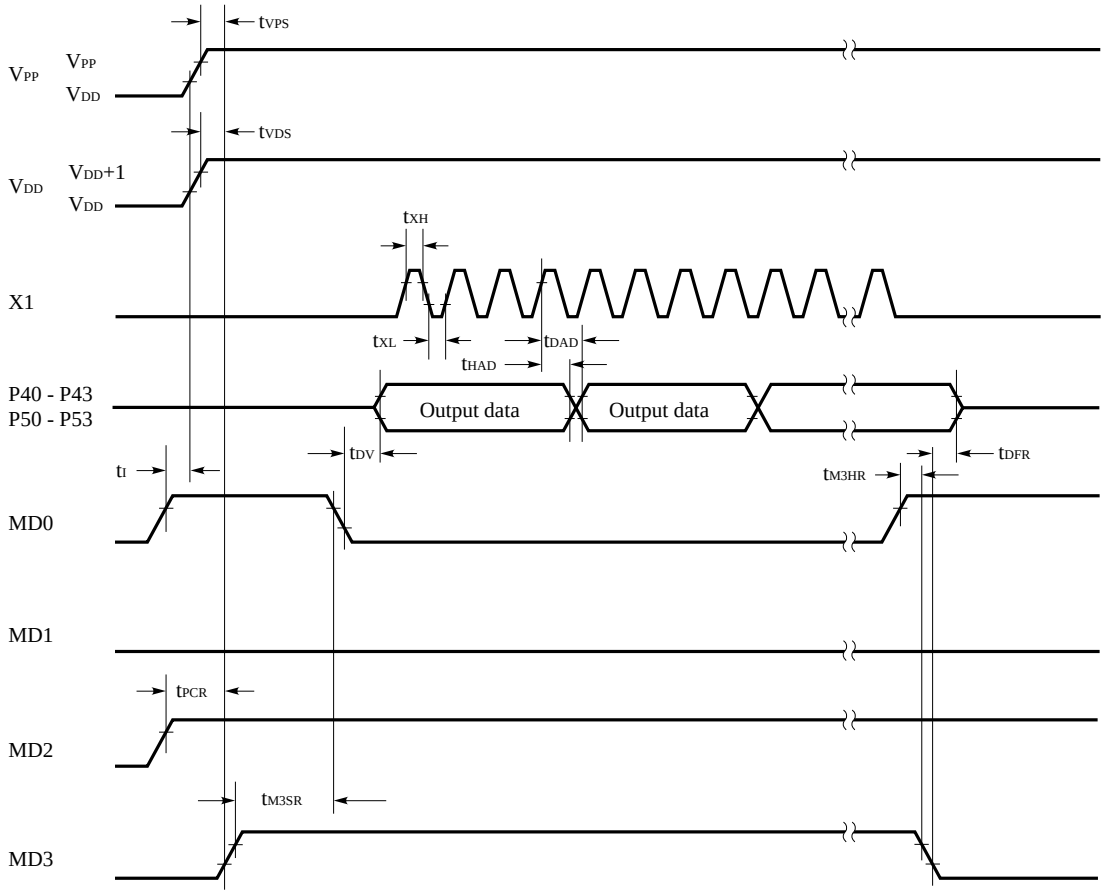
Notes 1. These symbols correspond to those of the μPD27C256A.

2. The internal address signal is incremented by the rising edge of the fourth X1 pulse; it is not connected to an external pin.

Program Memory Write Timing

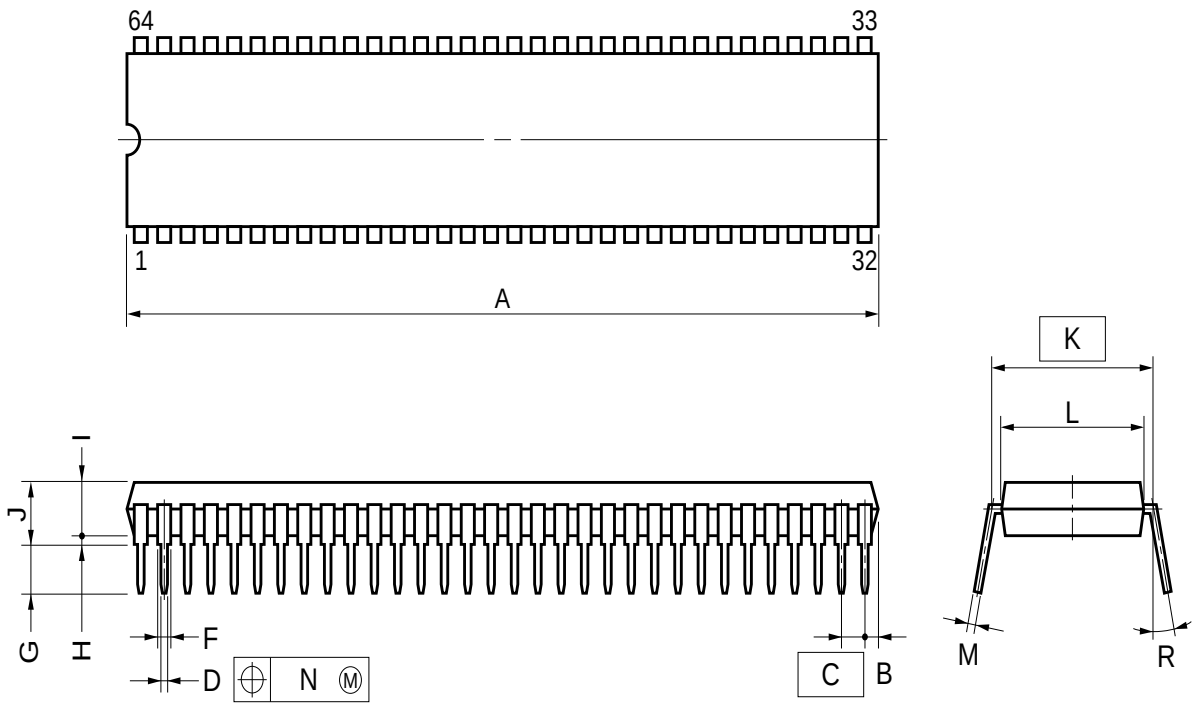


Program Memory Read Timing



6. PACKAGE DRAWINGS

64 PIN PLASTIC SHRINK DIP (750 mil)



NOTE

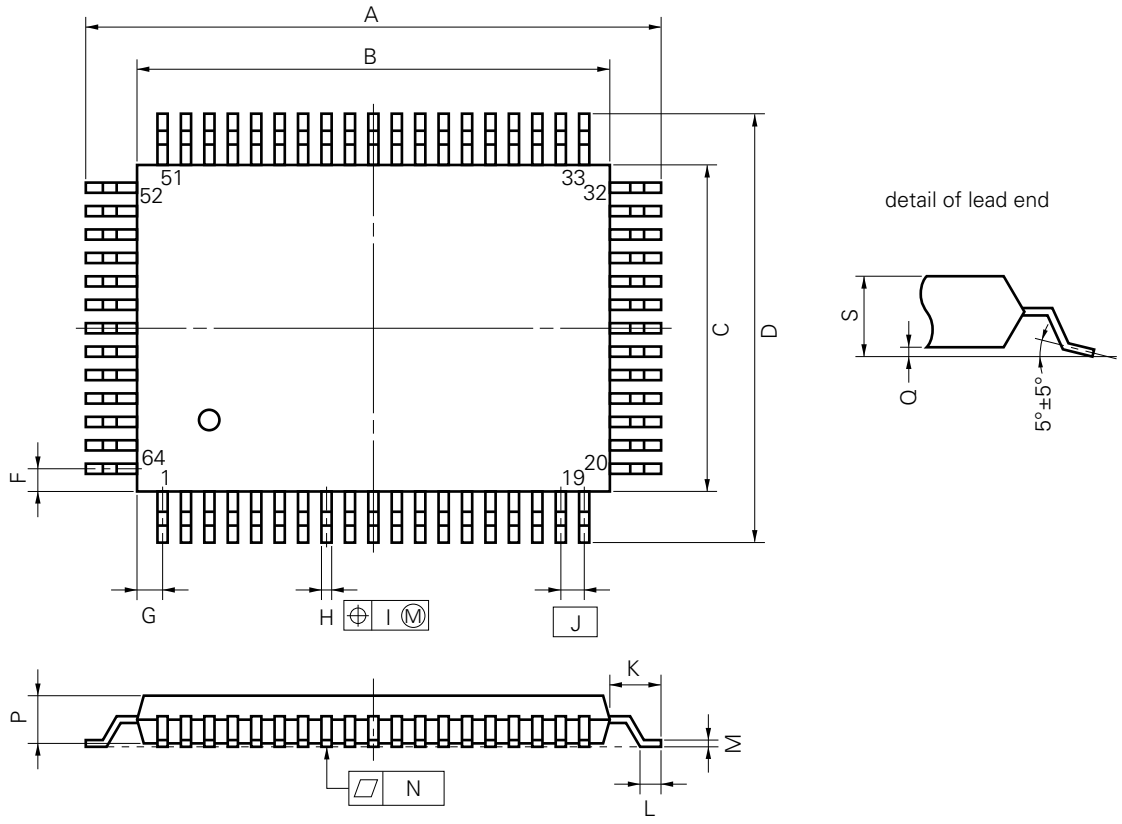
1) Each lead centerline is located within 0.17 mm (0.007 inch) of its true position (T.P.) at maximum material condition.

2) Item "K" to center of leads when formed parallel.

ITEM	MILLIMETERS	INCHES
A	58.68 MAX.	2.311 MAX.
B	1.78 MAX.	0.070 MAX.
C	1.778 (T.P.)	0.070 (T.P.)
D	0.50 ± 0.10	$0.020^{+0.004}_{-0.005}$
F	0.9 MIN.	0.035 MIN.
G	3.2 ± 0.3	0.126 ± 0.012
H	0.51 MIN.	0.020 MIN.
I	4.31 MAX.	0.170 MAX.
J	5.08 MAX.	0.200 MAX.
K	19.05 (T.P.)	0.750 (T.P.)
L	17.0	0.669
M	$0.25^{+0.10}_{-0.05}$	$0.010^{+0.004}_{-0.003}$
N	0.17	0.007
R	0~15°	0~15°

P64C-70-750A,C-1

64 PIN PLASTIC QFP (14×20)



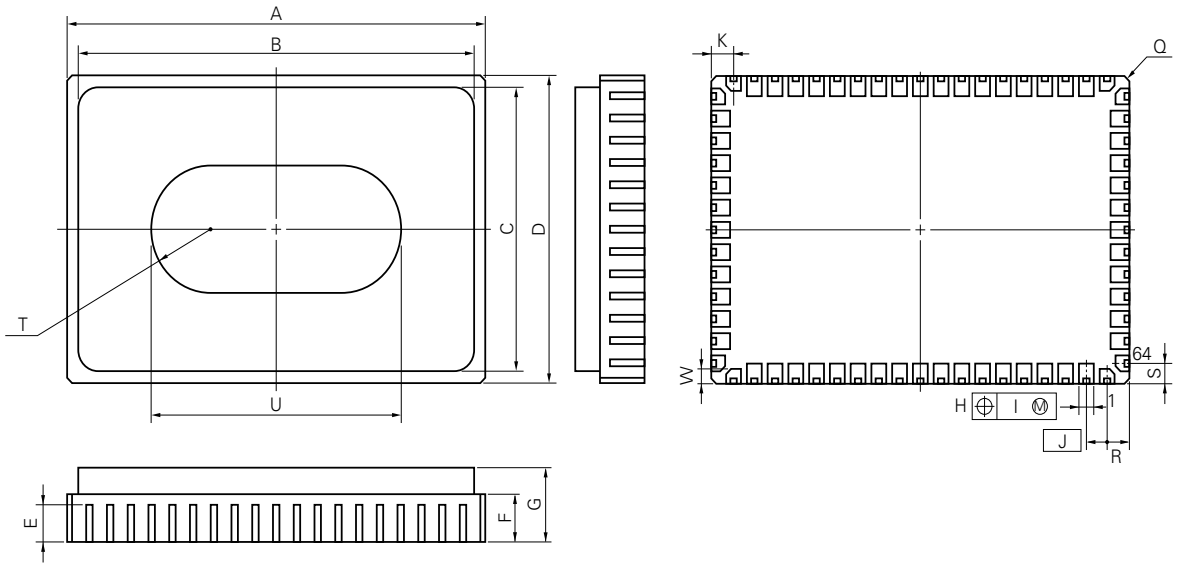
P64GF-100-3B8,3BE,3BR-1

NOTE

Each lead centerline is located within 0.20 mm (0.008 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	23.6±0.4	0.929±0.016
B	20.0±0.2	$0.795^{+0.009}_{-0.008}$
C	14.0±0.2	$0.551^{+0.009}_{-0.008}$
D	17.6±0.4	0.693±0.016
F	1.0	0.039
G	1.0	0.039
H	0.40±0.10	$0.016^{+0.004}_{-0.005}$
I	0.20	0.008
J	1.0 (T.P.)	0.039 (T.P.)
K	1.8±0.2	$0.071^{+0.008}_{-0.009}$
L	0.8±0.2	$0.031^{+0.009}_{-0.008}$
M	$0.15^{+0.10}_{-0.05}$	$0.006^{+0.004}_{-0.003}$
N	0.12	0.005
P	2.7	0.106
Q	0.1±0.1	0.004±0.004
S	3.0 MAX.	0.119 MAX.

64 PIN CERAMIC WQFN



X64KW-100A-2

NOTE

Each lead centerline is located within 0.10 mm (0.004 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	20.0±0.4	$0.787^{+0.017}_{-0.016}$
B	19.0	0.748
C	13.2	0.520
D	14.0±0.4	0.551±0.016
E	1.64	0.065
F	2.14	0.084
G	3.556 MAX.	0.140 MAX.
H	0.7±0.10	$0.028^{+0.004}_{-0.005}$
I	0.10	0.004
J	1.0 (T.P.)	0.039 (T.P.)
K	1.0±0.2	$0.039^{+0.009}_{-0.008}$
Q	C 0.25	C 0.010
R	1.0	0.039
S	1.0	0.039
T	R 3.0	R 0.118
U	12.0	0.472
W	0.8±0.2	$0.031^{+0.009}_{-0.008}$

7. RECOMMENDED SOLDERING CONDITIONS

The following conditions (See table below) must be met when soldering this product.

Please consult with our sales offices in case other soldering process is used, or in case soldering is done under different conditions.

For more details, refer to our document **"SEMICONDUCTOR DEVICE MOUNTING TECHNOLOGY MANUAL"** (IEI-1207).

TYPE OF SURFACE MOUNT DEVICE

μPD75P218GF-3BR

Soldering Process	Soldering Conditions	Symbol
Wave Soldering	Solder temperature: 260 ˚C or lower, Flow time: 10 seconds or less, Exposure limit Note: 7 days (10 hour pre-baking is required at 125 ˚C afterwards) Number of flow processes: 1	WS60-107-1
Infrared Ray Reflow	Peak temperature of package surface: 230 ˚C or lower Reflow time: 30 seconds or less (210 ˚C or higher), Number of reflow processes: 1 Exposure limit Note: 7 days (10 hour pre-baking is required at 125 ˚C afterwards)	IR30-107-1
VPS	Peak temperature of package surface: 215 ˚C or lower Reflow time: 40 seconds or less (200 ˚C or higher), Number of reflow processes: 1 Exposure limit Note: 7 days (10 hour pre-baking is required at 125 ˚C afterwards)	VP15-107-1
Partial Heating Method	Pin temperature: 300 ˚C or lower, Time: 3 seconds or less (Per side of the package)	–

Note Exposure limit before soldering after dry-pack package is opened. Storage conditions: 25 ˚C and relative humidity at 65 % or less.

Caution Do not apply more than one soldering method at any one time, except for "Partial heating method".

TYPE OF THROUGH HOLE DEVICE

μPD75P218CW

Soldering Process	Soldering Conditions
Wave Soldering (only lead part)	Solder temperature: 260 ˚C or lower, Flow time: 10 seconds or less
Partial Heating Method	Pin temperature: 260 ˚C or lower, Time: 10 seconds or less

Caution This wave soldering should be applied only to lead part, and do not jet molten solder on the surface of package.

APPENDIX DEVELOPMENT TOOLS

The following development tools are provided for the development of a system which employs the μPD75P218.

Language processor

<table>
<tr><td rowspan="4">RA75X relocatable assembler</td><td colspan="4">This program converts symbolic source code for the μPD75000 series of microcomputers into executable absolute address object code.
There are also functions such as generating a symbol table and optimizing branch instructions automatically.</td></tr>
<tr><td rowspan="2">Host machine</td><td colspan="2" rowspan="2">OS</td><td rowspan="2">Distribution media</td><td rowspan="2">Part number</td></tr>
<tr></tr>
<tr><td>PC-9800 series</td><td colspan="2">MS-DOS™
(Ver. 3.10 to Ver. 3.30C)</td><td>3.5-inch 2HD</td><td>μS5A13RA75X</td></tr>
<tr><td>5-inch 2HD</td><td>μS5A10RA75X</td></tr>
<tr><td></td><td>IBM PC series</td><td colspan="2">PC DOS™
(Ver. 3.1)</td><td>5-inch 2HC</td><td>μS7B10RA75X</td></tr>
</table>

PROM programming tools

<table>
<tr><td rowspan="4">Hardware</td><td>PG-1500</td><td colspan="4">The PG-1500 PROM programmer is used together with an accessory board and optional program adapter. It allows the user to program a single chip microcomputer containing PROM and typical 256K-bit to 1M-bit PROMs from a keyboard or a remote control.</td></tr>
<tr><td>PA-75P216ACW</td><td colspan="4">PROM programmer adapter dedicated to μPD75P218CW.
Connect the programmer adapter to PG-1500 for use.</td></tr>
<tr><td>PA-75P218GF</td><td colspan="4">PROM programmer adapter dedicated to μPD75P218GF.
Connect the programmer adapter to PG-1500 for use.</td></tr>
<tr><td>PA-75P218KB</td><td colspan="4">PROM programmer adapter dedicated to μPD75P218KB.
Connect the programmer adapter to PG-1500 for use.</td></tr>
<tr><td rowspan="5">Software</td><td rowspan="5">PG-1500 controller</td><td colspan="4">This program enables the host machine to control the PG-1500 through the serial and parallel interfaces.</td></tr>
<tr><td rowspan="2">Host machine</td><td colspan="2" rowspan="2">OS</td><td rowspan="2">Distribution media</td><td rowspan="2">Part number</td></tr>
<tr></tr>
<tr><td>PC-9800 series</td><td colspan="2">MS-DOS
(Ver. 3.10 to Ver. 3.30C)</td><td>3.5-inch 2HD</td><td>μS5A13PG1500</td></tr>
<tr><td>5-inch 2HD</td><td>μS5A10PG1500</td></tr>
<tr><td>IBM PC series</td><td colspan="2">PC DOS
(Ver. 3.1)</td><td>5-inch 2HC</td><td>μS7B10PG1500</td></tr>
</table>

Debugging tools

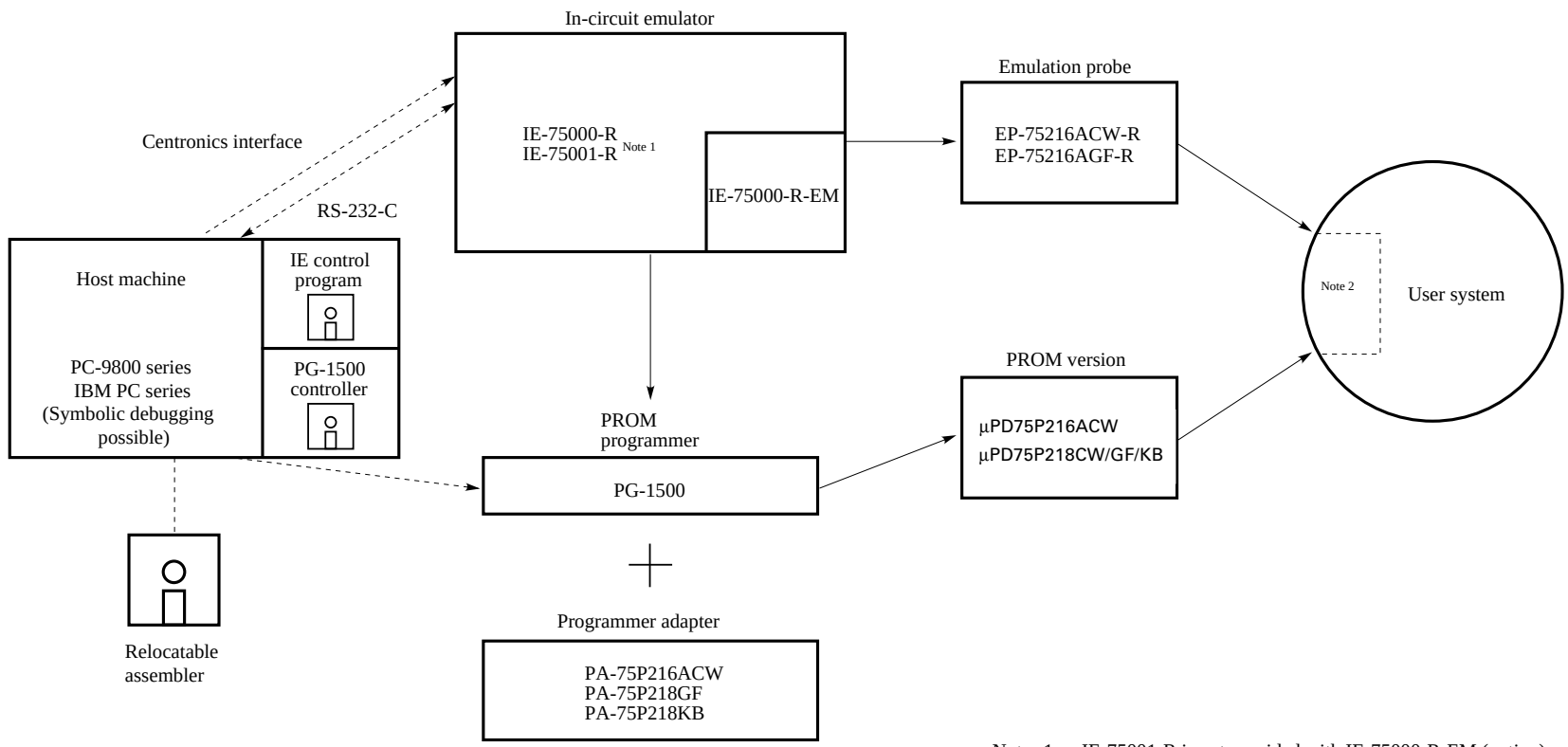
<table>
<tr><td rowspan="7">Hardware</td><td>IE-75000-R Note 1</td><td colspan="3">The IE-75000-R is an in-circuit emulator available for the 75X series. This emulator is used together with the emulation probe to develop application systems of the μPD75P218. For efficient debugging, the emulator is connected to the host machine and PROM programmer.</td></tr>
<tr><td>IE-75000-R-EM Note 2</td><td colspan="3">The IE-75000-R-EM is an emulation board for the IE-75000-R and IE-75001-R. The IE-75000-R contains the emulation board. The emulation board is used together with the IE-75000-R or IE75001-R to evaluate the μPD75P218.</td></tr>
<tr><td>IE-75001-R</td><td colspan="3">The IE-75001-R is an in-circuit emulator available for the 75X series. This emulator is used together with the IE-75000-R-EM Note 2 emulation board and emulation probe to develop application systems of the μPD75P218. For efficient debugging, the emulator is connected to the host machine and PROM programmer.</td></tr>
<tr><td>EP-75216ACW-R</td><td colspan="3">Emulation probe for the μPD75P218CW. Connect this probe to the IE-75000-R or IE-75001-R for use.</td></tr>
<tr><td>EP-75216AGF-R
EV-9200G-64</td><td colspan="3">Emulation probe for the μPD75P218GF. Connect this probe to the IE-75000-R or IE-75001-R for use. A 64-pin conversion socket, the EV-9200G-64, attached to the probe facilitates the connection of the probe with the user system.</td></tr>
<tr><td rowspan="4">Software</td><td rowspan="4">IE control program</td><td colspan="3">This program enables the host machine to control the IE-75000-R or IE-75001-R on the host machine through the RS-232-C interface.</td></tr>
<tr><td rowspan="2">Host machine</td><td>OS</td><td>Distribution media</td><td rowspan="2">Part number</td></tr>
<tr><td>PC-9800 series</td><td>MS-DOS (Ver. 3.10 to Ver. 3.30C)</td><td>3.5-inch 2HD</td><td>μS5A13IE75X</td></tr>
<tr><td>5-inch 2HD</td><td>μS5A10IE75X</td></tr>
<tr><td>IBM PC series</td><td>PC DOS (Ver. 3.1)</td><td>5-inch 2HC</td><td>μS7B10IE75X</td></tr>
</table>

Notes 1. Provided only for maintenance purposes.

2. The IE-75000-R-EM is an option.

Remark NEC is not responsible for the operation of the IE control program and assembler unless it runs on any host machine with the operation system listed above.

Configuration of Development Tools



Notes 1. IE-75001-R is not provided with IE-75000-R-EM (option).
2. EV-9200G-64

[MEMO]

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note:
Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note:
No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note:
Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

M4 92.6