TOSHIBA CMOS DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

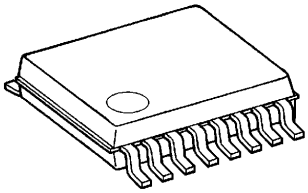
TC7MH238FK

3 - To - 8 Line Decoder

The TC7MH238 is an advanced high speed CMOS 3 - to - 8 DECODER fabricated with silicon gate C²MOS technology.
It achieves the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation.
When the device is enabled, 3 Binary Select inputs (A, B and C) determine which one of the outputs (Y0 - Y7) will go High.
When enable input G1 is held low or either $\overline{G}$2A or $\overline{G}$2B is held high, decoding function is inhibited and all outputs go Low.
G1 $\overline{G}$2A, and $\overline{G}$2B inputs are provided to ease cascade connection and for use as an address decoder for memory systems.
An input protection circuit ensures that 0 to 7V can be applied to the input pins without regard to the supply voltage. This device can be used to interface 5V to 3V systems and two supply systems such as battery back up. This circuit prevents device destruction due to mismatched supply and input voltages.

Features:

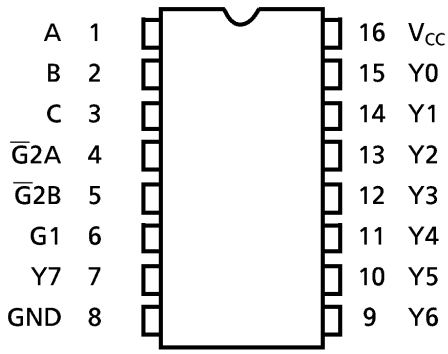
- High Speed····· t_{pd} = 5.5ns(typ.) at V_{CC} = 5V
- Low Power Dissipation····· I_{CC} = 4μA(max) at Ta = 25°C
- High Noise Immunity····· $V_{NIH} = V_{NIL}$ = 28% V_{CC} (min)
- Power Down Protection is provided on all inputs.
- Balanced Propagation Delays····· $t_{pLH} \simeq t_{pHL}$
- Wide Operating Voltage Range···· V_{CC} (opr) = 2V~5.5V
- Pin and Function Compatible with 74ALS238



VSSOP16-P-0030-0.50

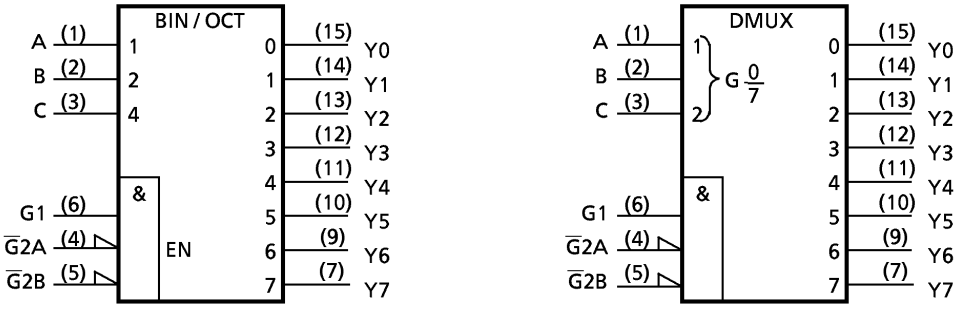
Weight: 0.02g (Typ.)

Pin Assignment



(TOP VIEW)

IEC Logic Symbol



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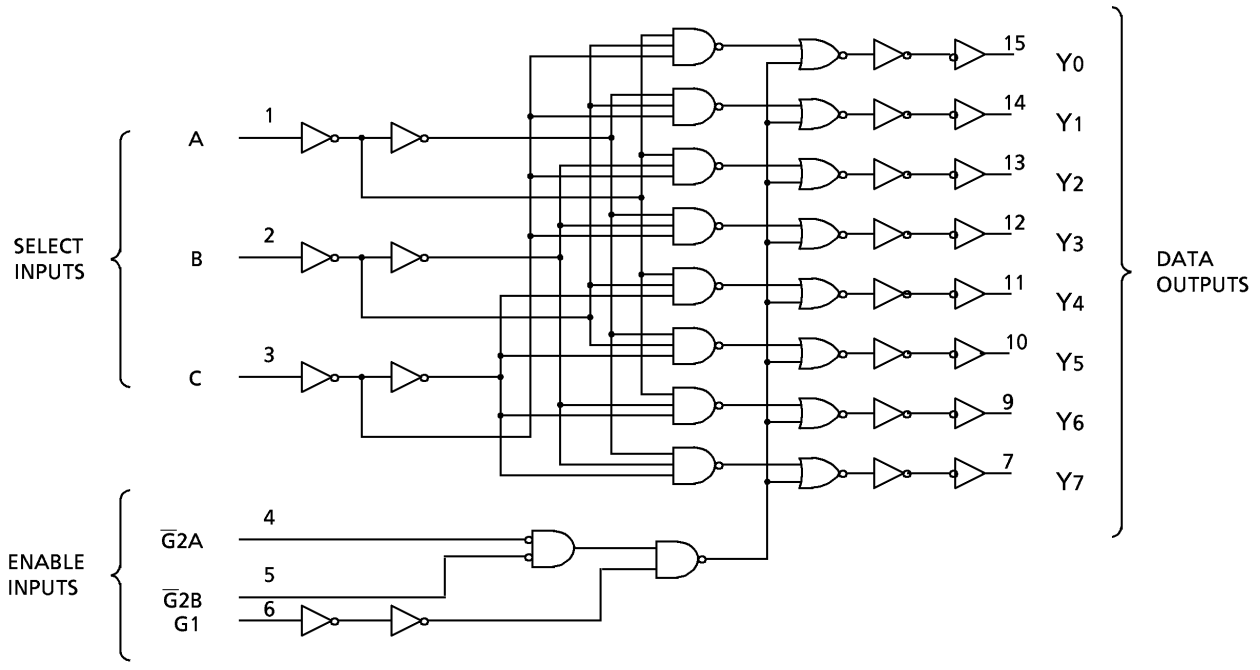
Truth Table

INPUTS						OUTPUTS								SELECTED OUTPUT
ENABLE			SELECT			Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7	
G1	$\overline{G}$2A	$\overline{G}$2B	C	B	A									
L	X	X	X	X	X	L	L	L	L	L	L	L	L	NONE
X	H	X	X	X	X	L	L	L	L	L	L	L	L	NONE
X	X	H	X	X	X	L	L	L	L	L	L	L	L	NONE
H	L	L	L	L	L	H	L	L	L	L	L	L	L	Y0
H	L	L	L	L	H	L	H	L	L	L	L	L	L	Y1
H	L	L	L	H	L	L	L	H	L	L	L	L	L	Y2
H	L	L	L	H	H	L	L	L	H	L	L	L	L	Y3
H	L	L	H	L	L	L	L	L	L	H	L	L	L	Y4
H	L	L	H	L	H	L	L	L	L	L	H	L	L	Y5
H	L	L	H	H	L	L	L	L	L	L	L	H	L	Y6
H	L	L	H	H	H	L	L	L	L	L	L	L	H	Y7

X: Don't Care

Logic Diagram



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Absolute Maximum Ratings

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	−0.5~7.0	V
DC Input Voltage	V_{IN}	−0.5~7.0	V
DC Output Voltage	V_{OUT}	−0.5~V_{CC} + 0.5	V
Input Diode Current	I_{IK}	−20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±75	mA
Power Dissipation	P_D	180	mW
Storage Temperature	T_{stg}	−65~150	°C

Recommended Operating Conditions

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	2.0~5.5	V
Input Voltage	V_{IN}	0~5.5	V
Output Voltage	V_{OUT}	0~V_{CC}	V
Operating Temperature	T_{opr}	−40~85	°C
Input Rise and Fall Time	dt / dv	0~100 (V_{CC} = 3.3 ± 0.3V) 0~20 (V_{CC} = 5 ± 0.5V)	ns / V

DC Electrical Characteristics

PARAMETER	SYMBOL	TEST CONDITION		V_{CC} (V)	Ta = 25°C			Ta = −40~85°C		UNIT
					Min	Typ.	Max	Min	Max	
High - Level Input Voltage	V_{IH}			2.0	1.50	—	—	1.50	—	V
				3.0~5.5	V_{CC}×0.7	—	—	V_{CC}×0.7	—	
Low - Level Input Voltage	V_{IL}			2.0	—	—	0.50	—	0.50	V
				3.0~5.5	—	—	V_{CC}×0.3	—	V_{CC}×0.3	
High - Level Output Voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} = −50μA	2.0	1.9	2.0	—	1.9	—	V
				3.0	2.9	3.0	—	2.9	—	
				4.5	4.4	4.5	—	4.4	—	
			I_{OH} = −4mA	3.0	2.58	—	—	2.48	—	
			I_{OH} = −8mA	4.5	3.94	—	—	3.80	—	
Low - Level Output Voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} = 50μA	2.0	—	0.0	0.1	—	0.1	V
				3.0	—	0.0	0.1	—	0.1	
				4.5	—	0.0	0.1	—	0.1	
			I_{OL} = 4mA	3.0	—	—	0.36	—	0.44	
			I_{OL} = 8mA	4.5	—	—	0.36	—	0.44	
Input Leakage Current	I_{IN}	V_{IN} = 5.5V or GND		0~5.5	—	—	±0.1	—	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN} = V_{CC} or GND		5.5	—	—	4.0	—	40.0	

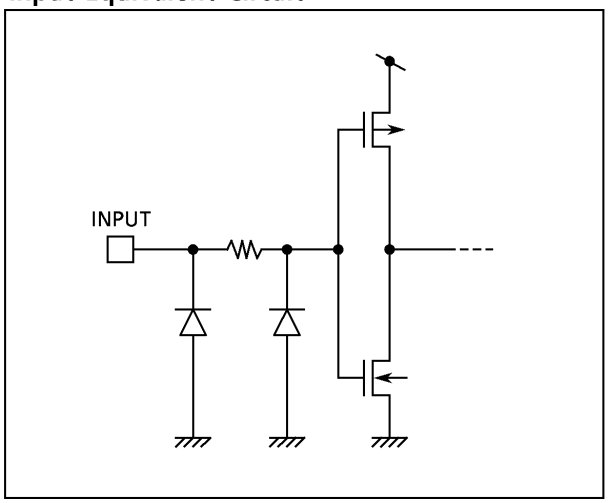
AC Electrical Characteristics (Input $t_r = t_f = 3ns$)

PARAMETER	SYMBOL	TEST CONDITION			Ta = 25°C			Ta = −40~85°C		UNIT
			V_{CC} (V)	CL (pF)	Min	Typ.	Max	Min	Max	
Propagation Delay Time (A, B, C - Y)	t_{pLH} t_{pHL}		3.3 ± 0.3	15	—	8.0	12.3	1.0	14.5	ns
				50	—	10.5	15.8	1.0	18.0	
			5.0 ± 0.5	15	—	5.5	8.1	1.0	9.5	
				50	—	7.0	10.1	1.0	11.5	
Propagation Delay Time (G 1 - Y)	t_{pLH} t_{pHL}		3.3 ± 0.3	15	—	8.1	12.8	1.0	15.0	
				50	—	10.6	16.3	1.0	18.5	
			5.0 ± 0.5	15	—	5.4	8.1	1.0	9.5	
				50	—	6.9	10.1	1.0	11.5	
Propagation Delay Time ($\overline{G}$ 2 - Y)	t_{pLH} t_{pHL}		3.3 ± 0.3	15	—	8.1	12.3	1.0	14.5	
				50	—	10.6	15.8	1.0	18.0	
			5.0 ± 0.5	15	—	5.7	8.1	1.0	9.5	
				50	—	7.2	10.1	1.0	11.5	
Input Capacitance	C_{IN}				—	4	10	—	10	pF
Power Dissipation Capacitance	C_{PD}	(Note 1)			—	37	—	—	—	

(Note 1): C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation:

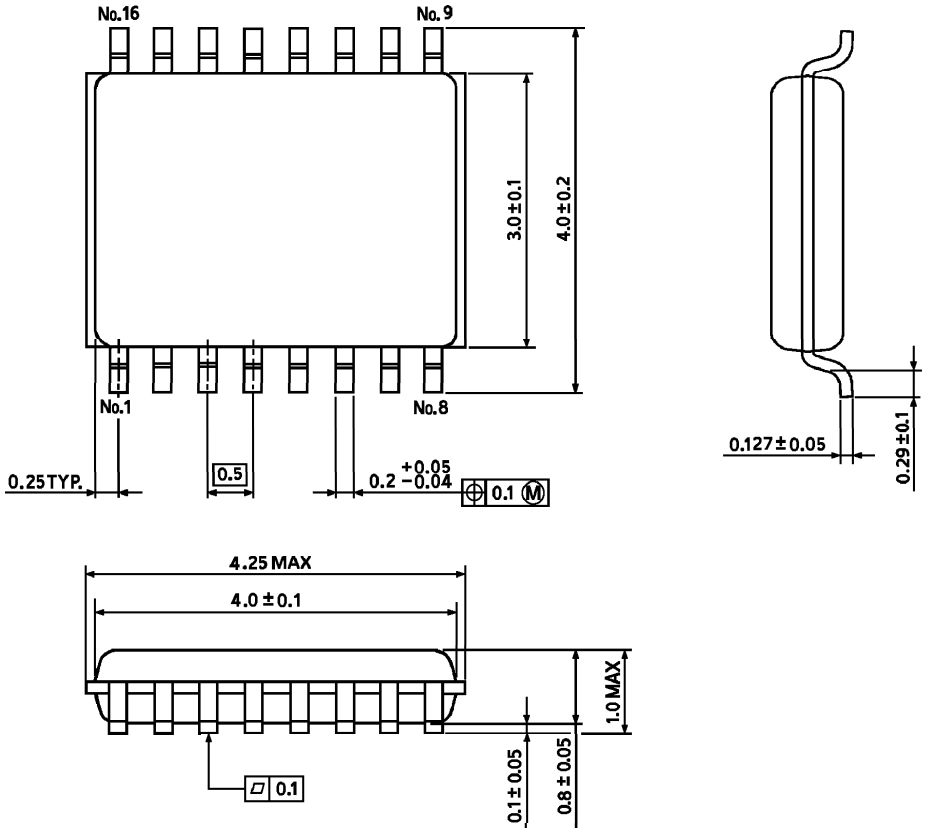
$$I_{CC\,(opr.)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

Input Equivalent Circuit



Outline Drawing

VSSOP16-P-0030-0.50 Unit: mm



Weight: 0.02g (Typ.)