

Power Amplifier/Antenna Switch for PHS

Description

The CXG1015N is a power amplifier/antenna switch MMIC for PHS. This is designed using the Sony's GaAs J-FET process and operates at a single positive power supply.

Features

- Single positive power supply 3.0 V
- Output power 20.2 dBm
(Antenna switch transfer output pin power)
- Low current consumption 160 mA
(Output power of 20.2 dBm)
- High power gain 39 dB Typ.
(Output power of 20.2 dBm)
- Low insertion loss 0.5 dB Typ.
- Small mold package 20-pin SSOP
(Pin interval of 0.5 mm pitch)

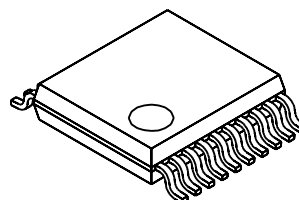
Structure

GaAs J-FET MMIC

Applications

- Power amplifiers for PHS
- Antenna switches for PHS

20 pin SSOP (Plastic)

**Absolute Maximum Ratings** (Ta=25 °C)

- | | | | |
|-----------------------------------|------------------|-------------|----|
| • Supply voltage | V _{DD} | 6 | V |
| • Voltage between gate and source | V _{GS0} | 1.5 | V |
| • Drain current | I _{DD} | 550 | mA |
| • Power dissipation | P _D | 3 | W |
| • Channel temperature | T _{ch} | 150 | °C |
| • Operating temperature | T _{opr} | -35 to +85 | °C |
| • Storage temperature | T _{stg} | -65 to +150 | °C |

Electrical Characteristics

Power Amplifier + Antenna Switch Transfer Block

$V_{DD}=3.0\text{ V}$, $V_{CTL}=2.0\text{ V}$, $f=1.90\text{ GHz}$

($T_a=25\text{ }^\circ\text{C}$)

Item	Symbol	Min.	Typ.	Max.	Unit
* Current consumption	I_{DD}		160		mA
* Gate voltage adjustment value	V_{GG2}	0	0.25	0.7	V
Output power (Power Amplifier + Antenna Switch Transfer Block)	P_{OUT}	20.2			dBm
* Power gain	G_P	35.5	39	42	dB
* Adjacent channel leak power ratio (600 kHz \pm 100 kHz)	ACPR600		-59	-54	dBc

- * Values where V_{GG1} and V_{GG2} are adjusted so that I_{DD} becomes 160 mA when the power amplifier output pin and the antenna switch transfer input pin are connected on the Sony's recommended evaluation board and the output power on the antenna switch transfer output pin is 20.2 dBm.

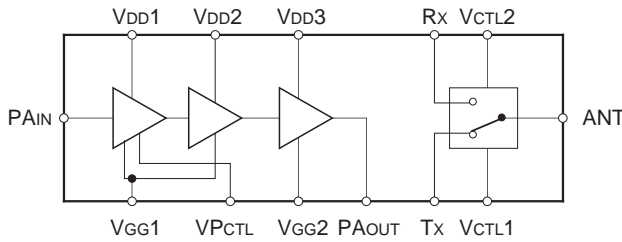
Antenna Switch Receive Block

$V_{CTL(L)}=0\text{ V}$, $V_{CTL(H)}=3.0\text{ V}$

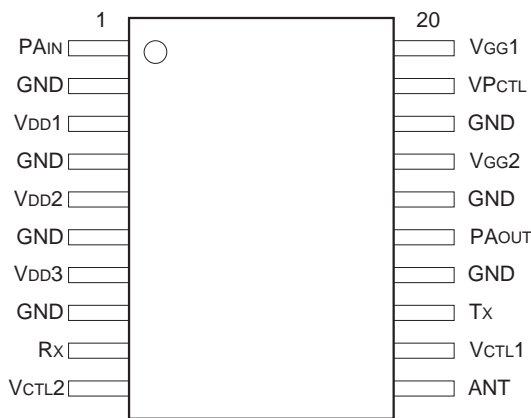
($T_a=25\text{ }^\circ\text{C}$)

Item	Symbol	Min.	Typ.	Max.	Unit
Insertion loss	IL		0.5	0.8	dB
Isolation	ISO	20	24		dB
Control pin current	I_{CTL}		40	100	μA

Block Diagram



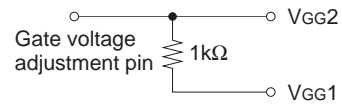
Pin Configuration



Antenna Switch Operation

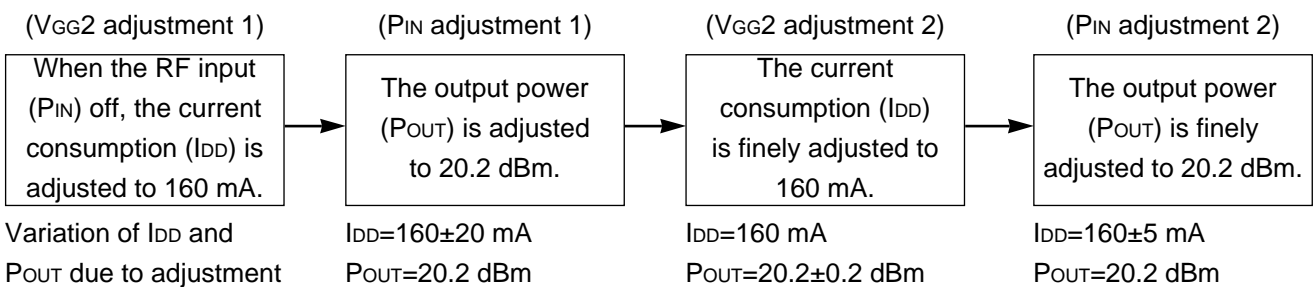
V _{CTL1} =3 V	ANT-Tx	ON
V _{CTL2} =0 V	ANT-Rx	OFF
V _{CTL1} =0 V	ANT-Tx	OFF
V _{CTL2} =3 V	ANT-Rx	ON

Gate Bias Circuit of Power Amplifier Block

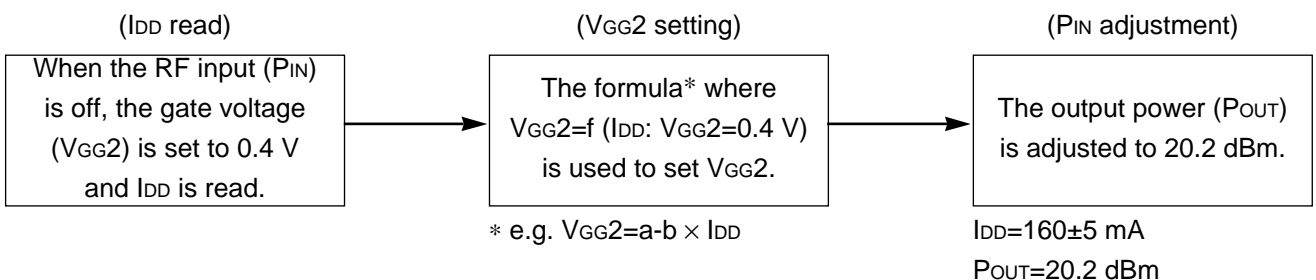


Recommended Current Adjustment Method

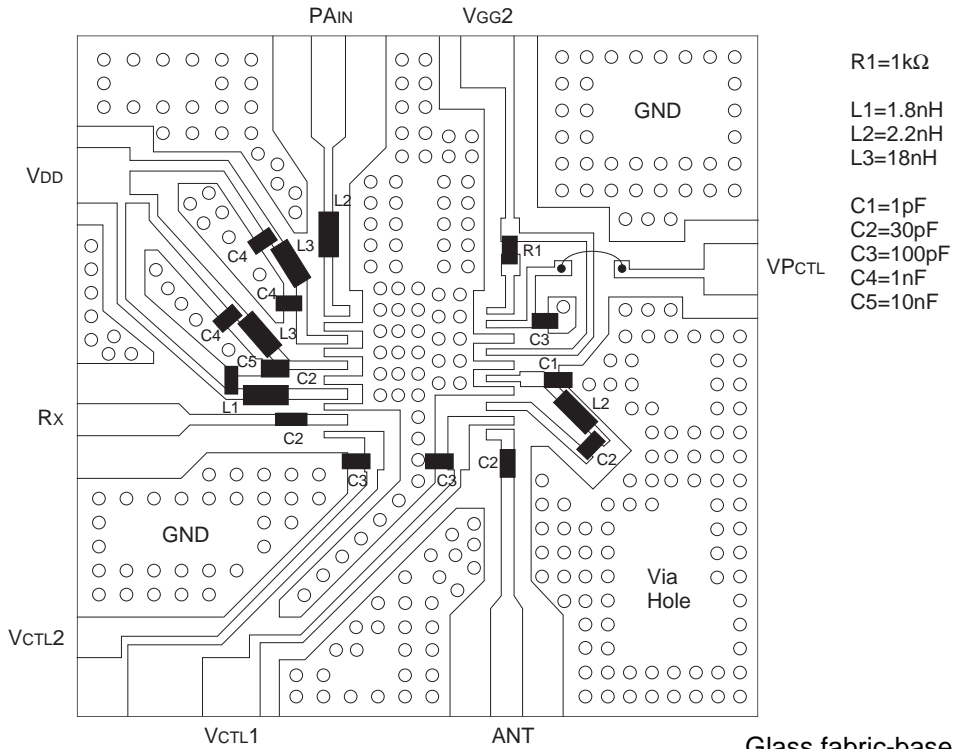
(1) V_{GG2}/P_{IN} separate adjustment



(2) Simple adjustment

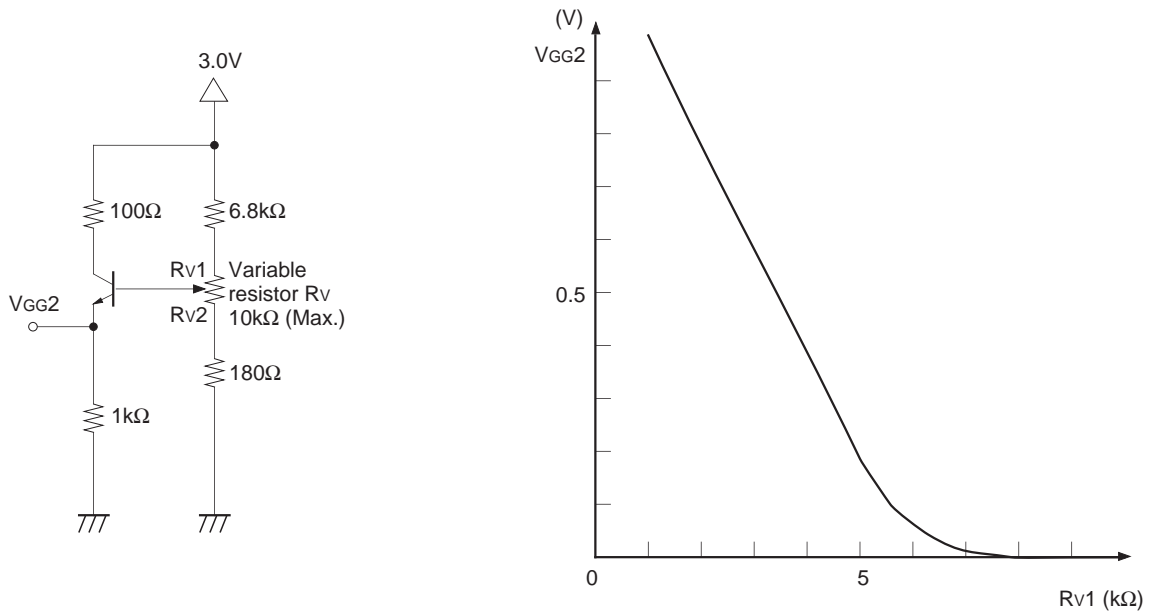


Recommended Evaluation Circuit



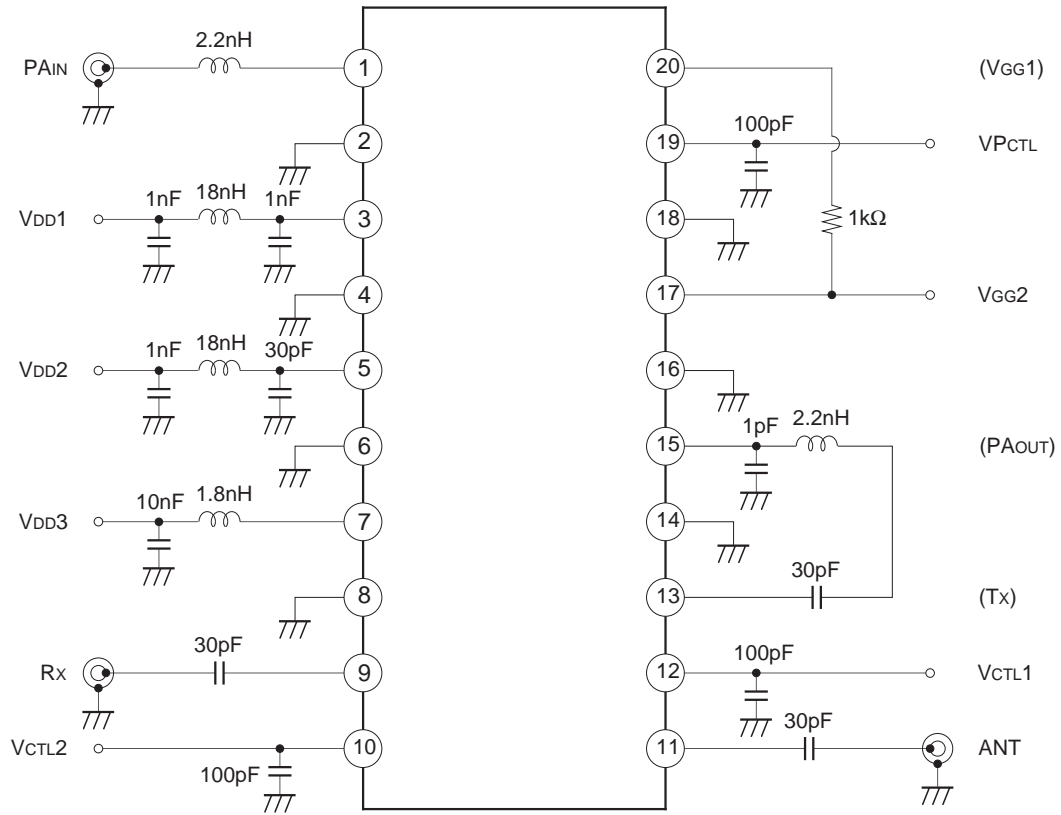
Glass fabric-base epoxy board
 GND for the overall back side
 Dimension : 25 mm × 25 mm
 Thickness : 0.2 mm

Recommended Gate Bias Circuit and Circuit Characteristics



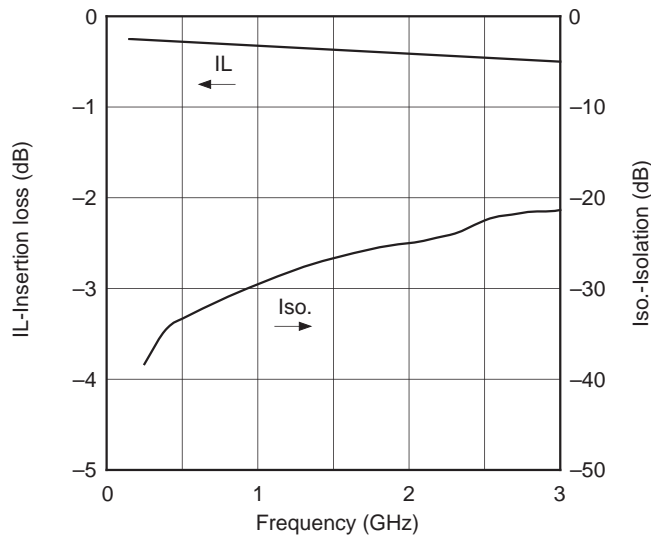
Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

Recommended External Circuit

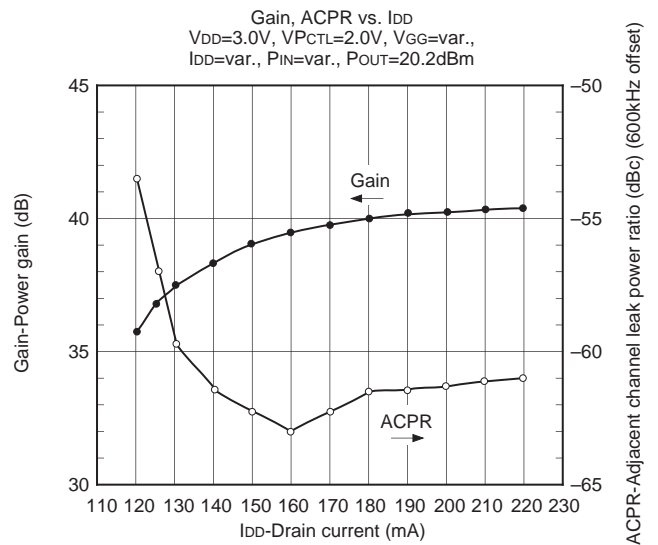
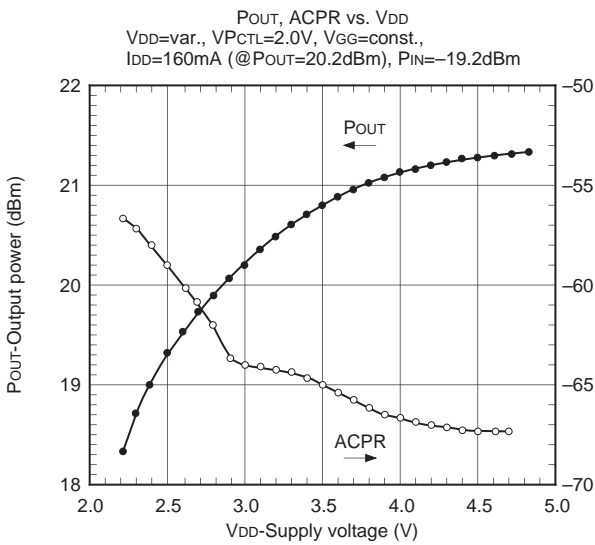
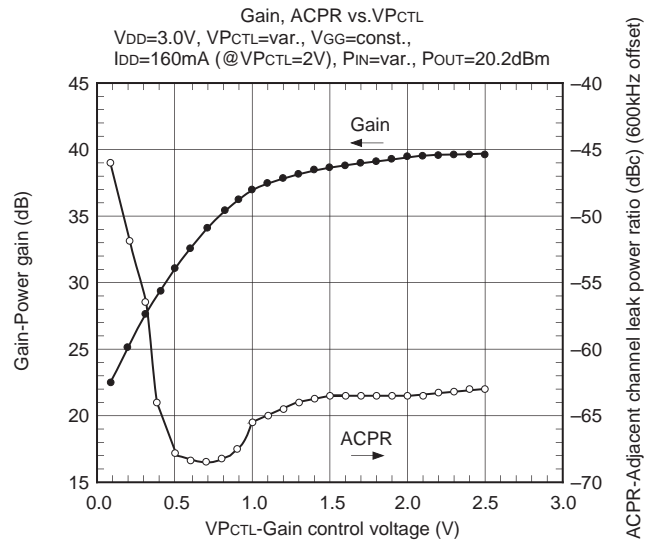
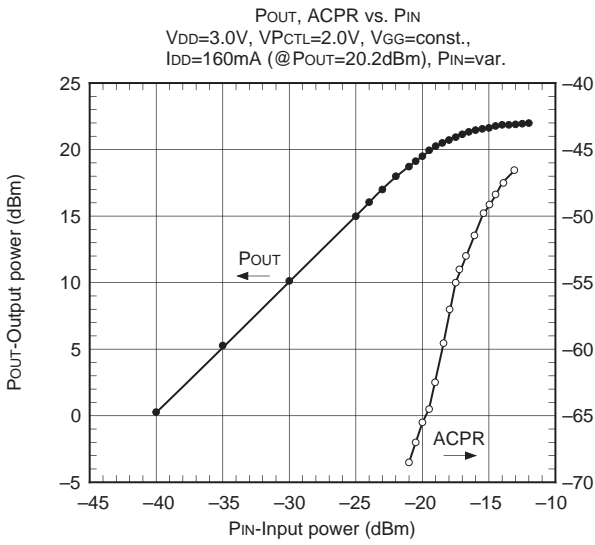


Example of Representative Characteristics (Ta=25 °C)
Antenna Switch Receive Block

IL, Iso. vs. Freq.

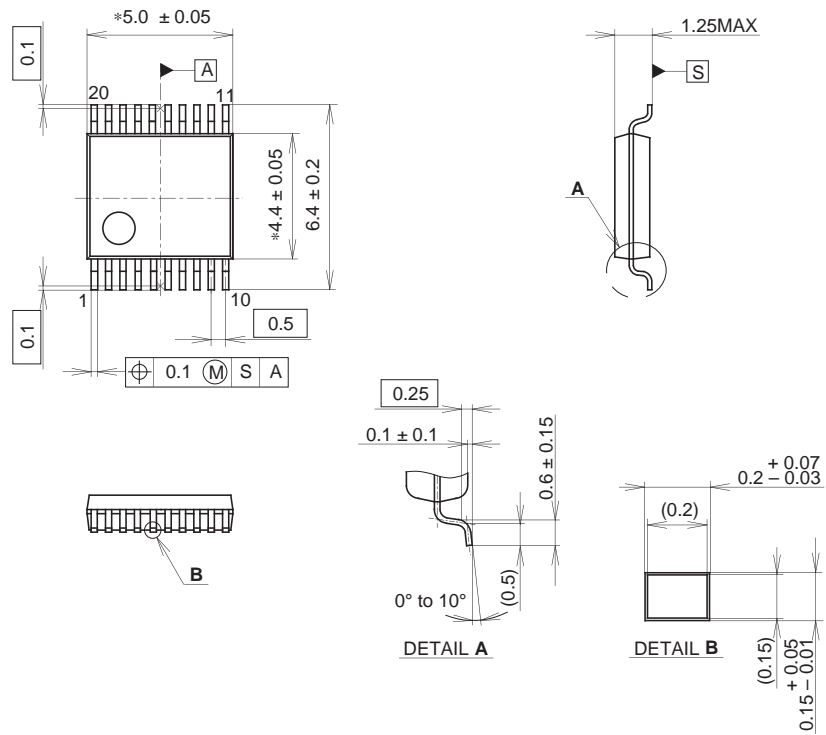


Example of Representative Characteristics
Power Amplifier + Antenna Switch Transfer Block



Package Outline Unit : mm

20PIN SSOP(PLASTIC)



NOTE: Dimension "*" does not include mold protrusion.

PACKAGE STRUCTURE

SONY CODE	SSOP-20P-L03
EIAJ CODE	SSOP020-P-0044
JEDEC CODE	_____

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER/PALLADIUM PLATING
LEAD MATERIAL	COPPER ALLOY
PACKAGE MASS	0.1g