DATA SHEET

NEC

BIPOLAR ANALOG INTEGRATED CIRCUIT

μPC2713T

1.2 GHz LOW NOISE WIDE BAND AMPLIFIER
SILICON BIPOLAR MONOLITHIC INTEGRATED CIRCUIT

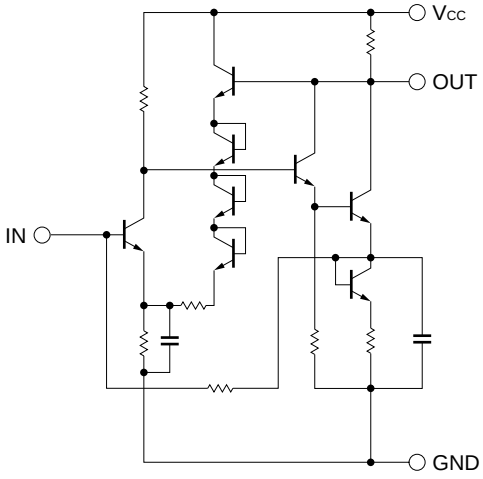
FEATURES

- High power gain : 29 dB TYP. @ f = 0.5 GHz
- Excellent frequency response : 1.2 GHz TYP. @ 3 dB down below the gain at 0.1 GHz
- Low noise figure : 3.2 dB TYP.
- Single supply voltage : 5 V
- Input and output matching : 50 Ω
- Mini package : 6 pin mini mold

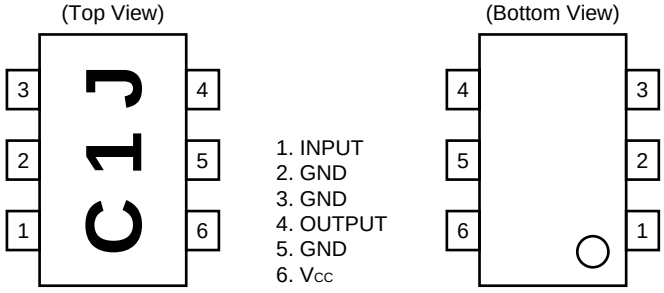
ORDERING INFORMATION

PART NUMBER	PACKAGE	SUPPLYING FORM
μPC2713T-E3	6 pin mini mold	Embossed tape 8 mm wide. QTY 3 kp/Reel. Pin 1, 2, 3 face to perforation side of the tape.

EQUIVALENT CIRCUIT



PIN CONNECTIONS



Document No. P12430EJ2V0DS00 (2nd edition)
(Previous No. IC-2950)
Date Published March 1997 N
Printed in Japan

ABSOLUTE MAXIMUM RATINGS (Unless otherwise specified, T_A = +25 °C)

Supply Voltage	V_{CC}	6	V
Total Circuit Current	I_{CC}	30	mA
Power Dissipation	P_D	280*	mW
Operating Temperature	T_{opt}	–40 to +85	°C
Storage Temperature	T_{stg}	–55 to +150	°C
Input Power	P_{in}	+10	dBm

* Mounted on 50 × 50 × 1.6 mm double copper clad epoxy glass PWB (T_A = +85 °C)

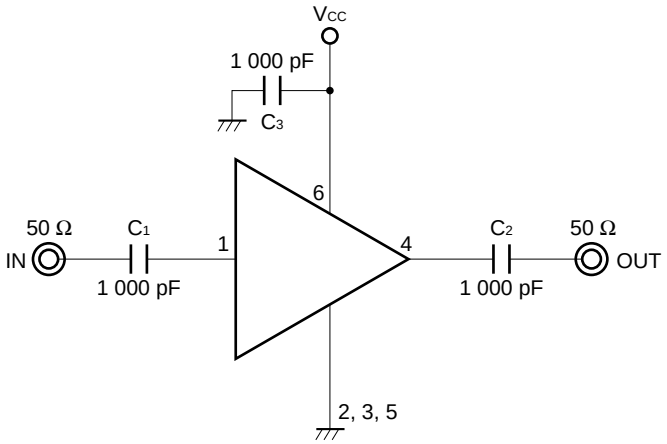
RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply Voltage	V_{CC}	4.5	5.0	5.5	V

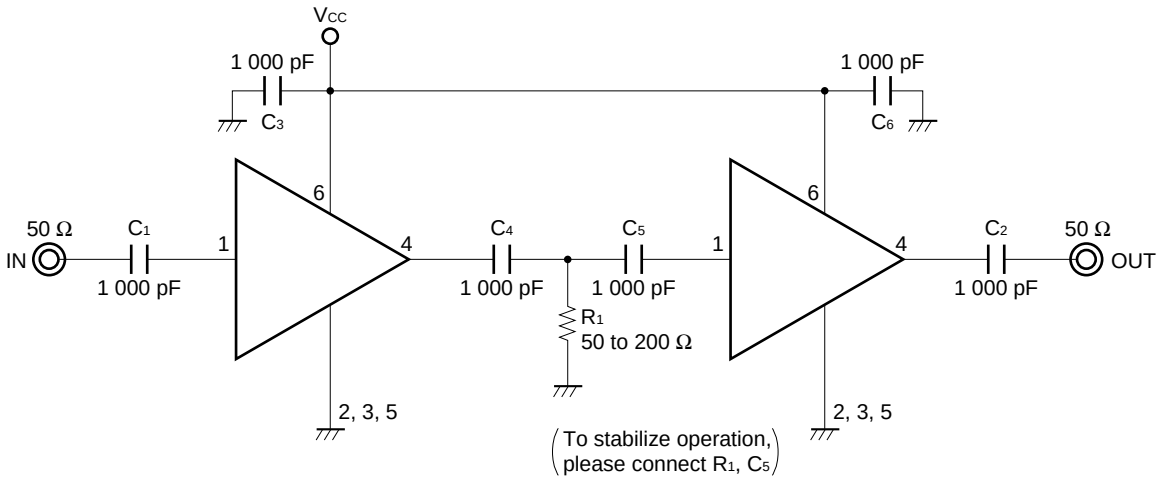
ELECTRICAL CHARACTERISTICS (T_A = +25 °C, V_{CC} = 5.0 V, Z_S = Z_L = 50 Ω)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
Circuit Current	I_{CC}	9	12	15	mA	No Signal
Power Gain	G_P	26	29	33	dB	f = 0.5 GHz
Maximum Output Level	$P_{O(sat)}$	+4	+7		dBm	f = 0.5 GHz, P_{in} = 0 dBm
Noise Figure	NF		3.2	4.5	dB	f = 0.5 GHz
Upper Limit Operating Frequency	f_U	0.9	1.2		GHz	3 dB down below flat gain at f = 0.1 GHz
Isolation	ISL	35	40		dB	f = 0.5 GHz
Input Return Loss	RL_{in}	10	13		dB	f = 0.5 GHz
Output Return Loss	RL_{out}	6	9		dB	f = 0.5 GHz
Gain Flatness	ΔG_P		±0.8		dB	f = 0.1 to 0.8 GHz

TEST CIRCUIT



EXAMPLE OF APPLICATION CIRCUIT



The application circuits and their parameters are for reference only and are not intended for use in actual design-ins.

Capacitors for V_{CC}, input and output pins

1 000 pF capacitors are recommendable as bypass capacitor for V_{CC} pin and coupling capacitors for input/output pins.

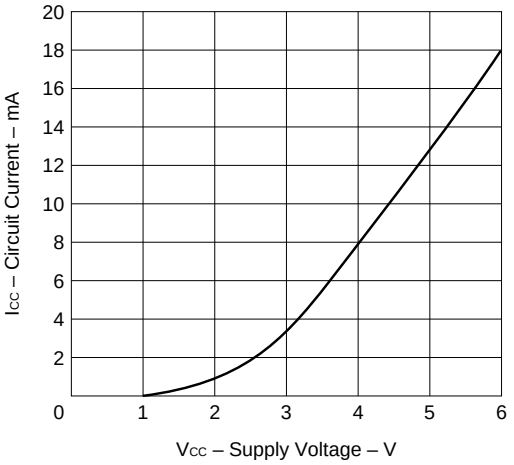
Bypass capacitor for V_{CC} pin is intended to minimize V_{CC} pin's ground impedance. Therefore, stable bias can be supplied against V_{CC} fluctuation.

Coupling capacitors for input/output pins are intended to minimize RF serial impedance and cut DC.

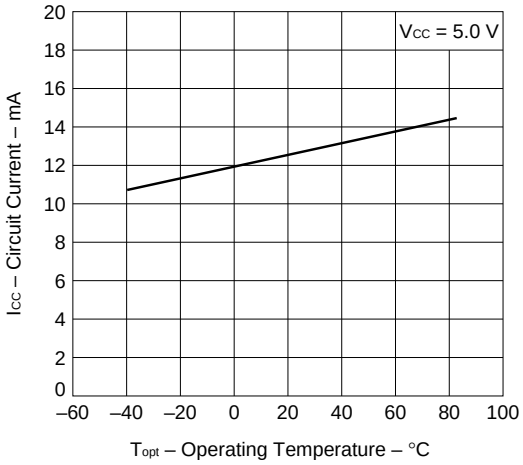
To get flat gain from 100 MHz up, 1 000 pF capacitors are assembled on the test circuit. [Actually, 1 000 pF capacitors give flat gain at least 10 MHz. In the case of under 10 MHz operation, increase the value of coupling capacitor such as 2 200 pF. Because the coupling capacitors are determined by the equation of $C = 1/(2 \pi fZs)$.]

TYPICAL CHARACTERISTICS (T_A = +25 °C)

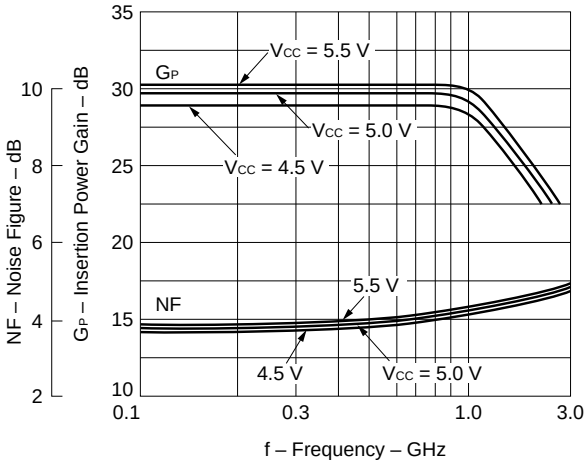
CIRCUIT CURRENT vs. SUPPLY VOLTAGE



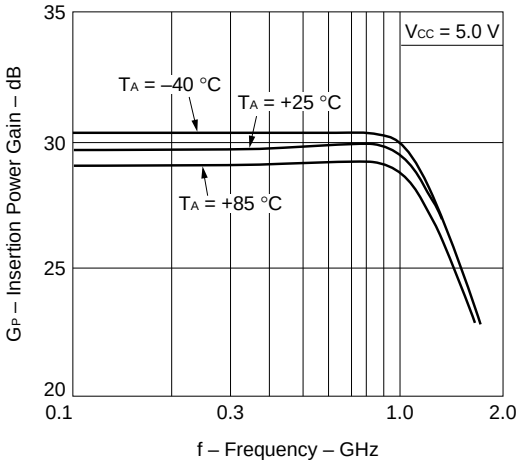
CIRCUIT CURRENT vs. OPERATING TEMPERATURE



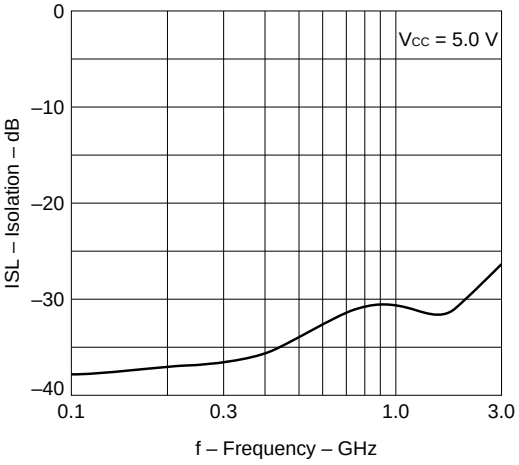
NOISE FIGURE AND INSERTION POWER GAIN vs. FREQUENCY



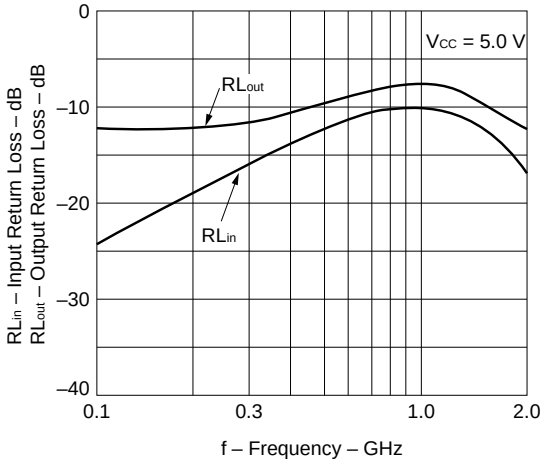
INSERTION POWER GAIN vs. FREQUENCY



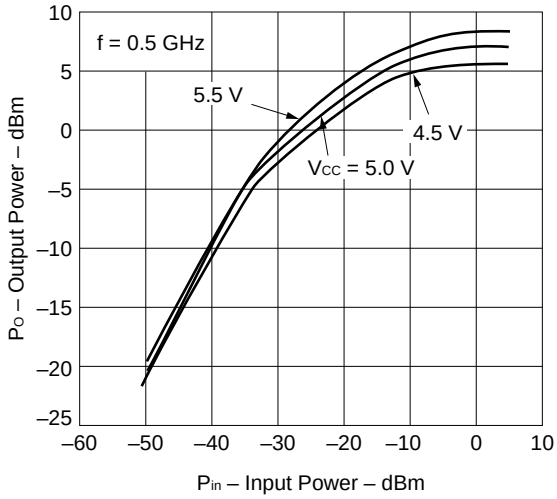
ISOLATION vs. FREQUENCY



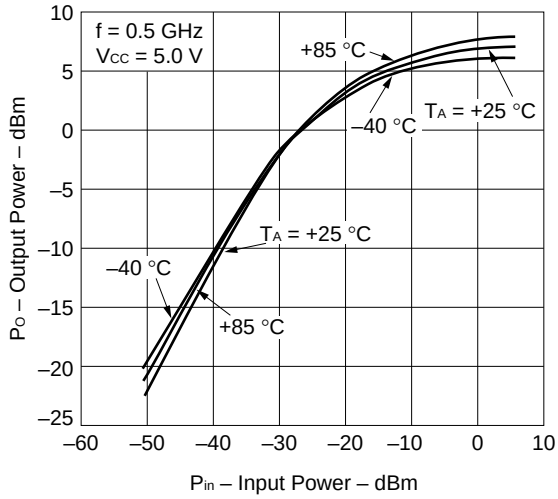
INPUT RETURN LOSS, OUTPUT RETURN LOSS vs. FREQUENCY



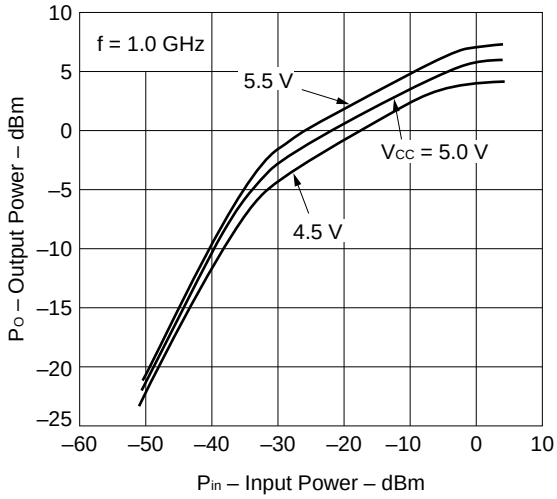
OUTPUT POWER vs. INPUT POWER



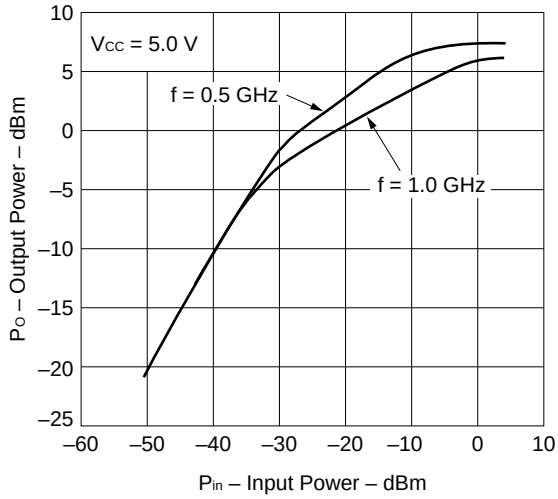
OUTPUT POWER vs. INPUT POWER



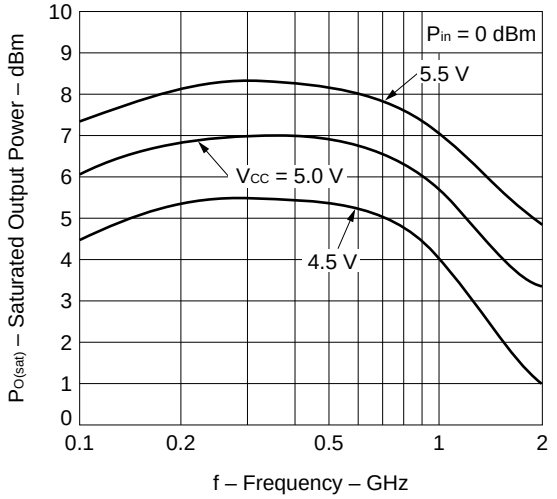
OUTPUT POWER vs. INPUT POWER



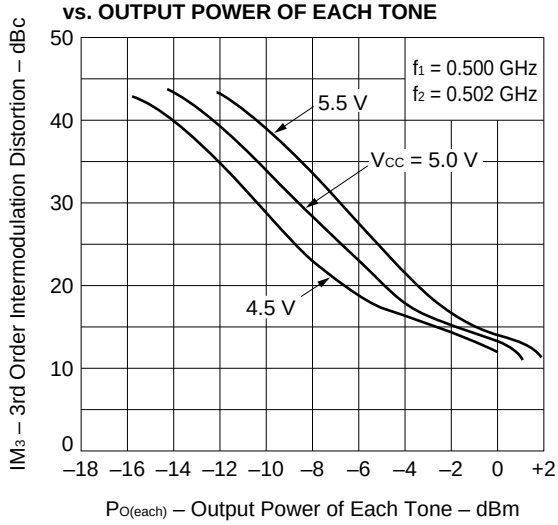
OUTPUT POWER vs. INPUT POWER



SATURATED OUTPUT POWER vs. FREQUENCY

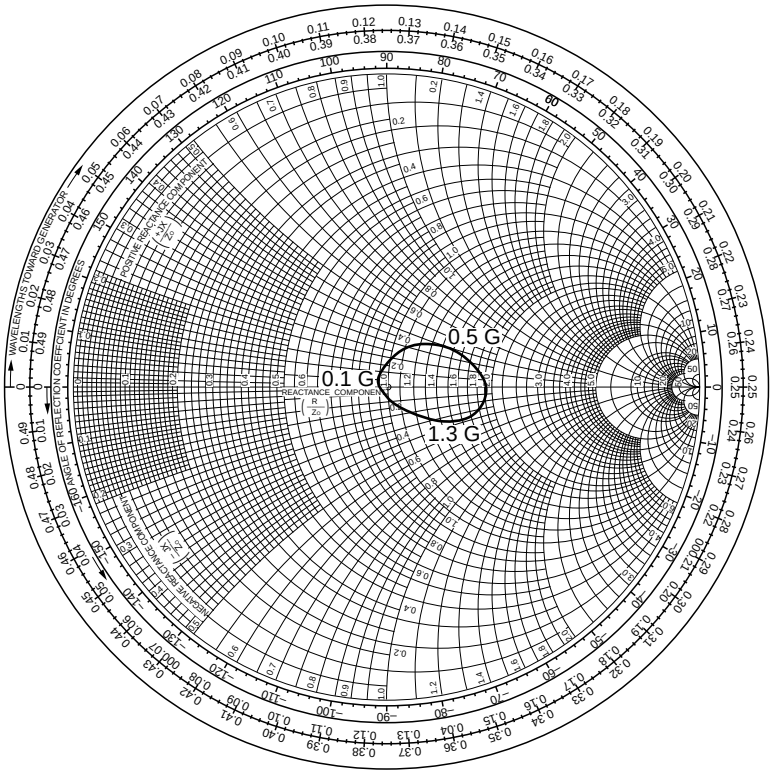


THIRD ORDER INTERMODULATION DISTORTION vs. OUTPUT POWER OF EACH TONE



S PARAMETER

S_{11}-FREQUENCY



S_{22}-FREQUENCY

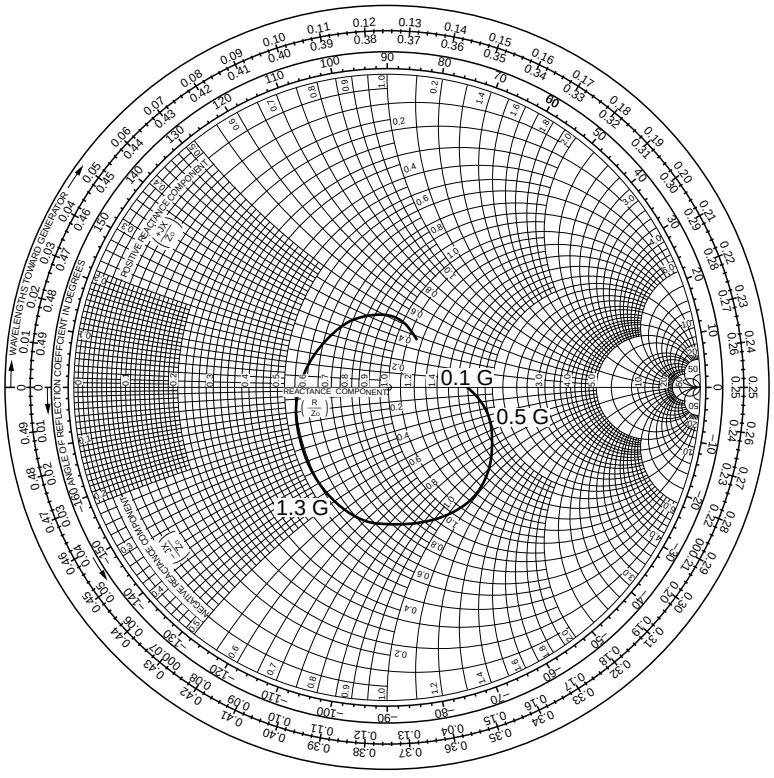
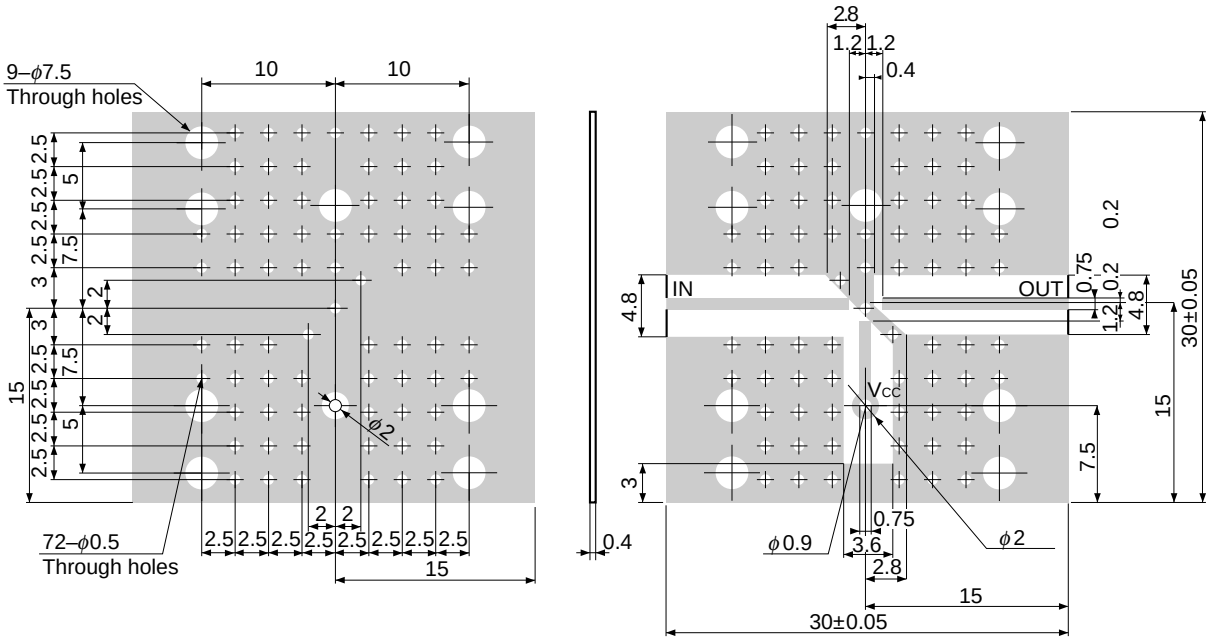


Illustration of evaluation board for the test circuit



Note

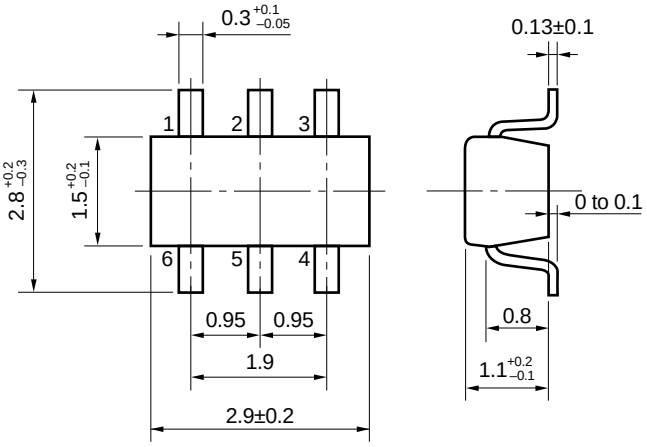
(1) 30 × 30 × 0.4 mm double sided copper clad polyimide board.

(2) Back side: GND pattern

(3) Solder plated on pattern

(4) ⊕⊕⊕: Through holes

6 PINS MINI MOLD PACKAGE DIMENSIONS (Unit: mm)



NOTE ON CORRECT USE

(1) Observe precautions for handling because of electro-static sensitive devices.

(2) Form a ground pattern as wide as possible to keep the minimum ground impedance (to prevent undesired oscillation).

(3) Keep the track length of the ground pins as short as possible.

(4) Connect a bypass capacitor (e.g. 1 000 pF) to the V_{CC} pin.

RECOMMENDED SOLDERING CONDITIONS

This product should be soldered in the following recommended conditions. Other soldering methods and conditions than the recommended conditions are to be consulted with our sales representatives.

μPC2712T

Soldering method	Soldering conditions	Recommended condition symbols
Infrared ray reflow	Package peak temperature: 235 °C, Hour: within 30 s. (more than 210 °C), Time: 3 times, Limited days; no.*	IR35-00-3
VPS	Package peak temperature: 215 °C, Hour: within 40 s. (more than 200 °C), Time: 3 times, Limited days: no.*	VP15-00-3
Wave soldering	Soldering tub temperature: less than 260 °C, Hour: within 10 s. Time: 1 time, Limited days: no.*	WS60-00-1
Pin part heating	Pin area temperature: less than 300 °C, Hour: within 3 s. Limited days: no.*	

*: It is the storage days after opening a dry pack, the storage conditions are 25 °C, less than 65 % RH.

Note 1. The combined use of soldering method is to be avoided (However, except the pin area heating method).

For details of recommended soldering conditions for surface mounting, refer to information document SEMICONDUCTOR DEVICE MOUNTING TECHNOLOGY MANUAL (C10535E).

[MEMO]

[MEMO]

M4 96.5