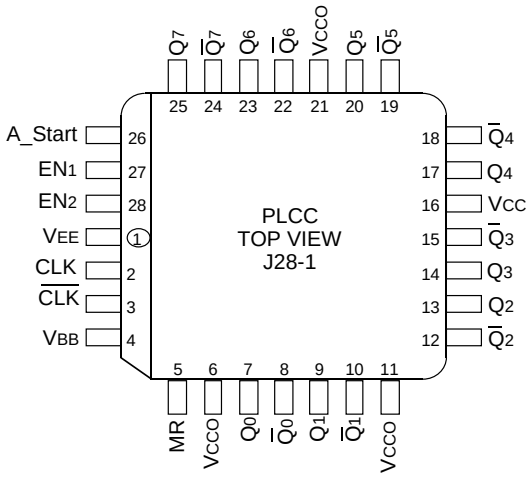
8-BIT RIPPLE COUNTER

FEATURES

- **1.8GHz min. count frequency**
- **Extended 100E V_{EE} range of –4.2V to –5.5V**
- **Synchronous and asynchronous enable pins**
- **Differential clock input and data output pins**
- **V_{BB} output for single-ended use**
- **Asynchronous Master Reset**
- **Internal 75KΩ input pull-down resistors**
- **Available in 28-pin PLCC packge**

PIN CONFIGURATION



PIN NAMES

Pin	Function
CLK, /CLK	Differential Clock Inputs
Q_0–Q_7, $\overline{Q}_0$–$\overline{Q}_7$	Differential Q Outputs
A_Start	Asynchronous Enable Input
EN_1, EN_2	Synchronous Enable Inputs
MR	Asynchronous Master Reset
V_{BB}	Switching Reference Output
V_{CCO}	V_{CC} to Output

DESCRIPTION

The SY10/100E137 are very high speed binary ripple counters. The two least significant bits were designed with very fast edge rates, while the more significant bits maintain standard ECLinPS output edge rates. This allows the counters to operate at very high frequencies, while maintaining a moderate power dissipation level.

The devices are ideally suited for multiple frequency clock generation, as well as for counters in high-performance ATE time measurement boards.

Both asynchronous and synchronous enables are available to maximize the device's flexibility for various applications. The asynchronous enable input, A_Start, when asserted, enables the counter while overriding any synchronous enable signals. The E137 features XOR'ed enable inputs, EN_1 and EN_2, which are synchronous to the CLK input. When only one synchronous enable is asserted, the counter becomes disabled on the next CLK transition. All outputs remain in the previous state poised for the other synchronous enable or A_Start to be asserted in order to re-enable the counter. Asserting both synchronous enables causes the counter to become enabled on the next transition of the CLK. EN_1 (or EN_2) and CLK edges are coincident. Sufficient delay has been inserted in the CLK path (to compensate for the XOR gate delay and the internal D-flip-flop set-up time) to ensure that the synchronous enable signal is clocked correctly; hence, the counter is disabled.

The E137 can also be driven single-endedly utilizing the V_{BB} output supply as the voltage reference for the CLK input signal. If a single-ended signal is to be used, the V_{BB} pin should be connected to the $\overline{CLK}$ input and bypassed to ground via a 0.01µF capacitor. V_{BB} can only source/sink 0.5mA; therefore, it should be used as a switching reference for the E137 only.

All input pins left open will be pulled LOW via an input pull-down resistor. Therefore, do not leave the differential CLK inputs open. Doing so causes the current source transistor of the input clock gate to become saturated, thus upsetting the internal bias regulators and jeopardizing the stability of the device.

The asynchronous Master Reset resets the counter to an all zero state upon assertion.

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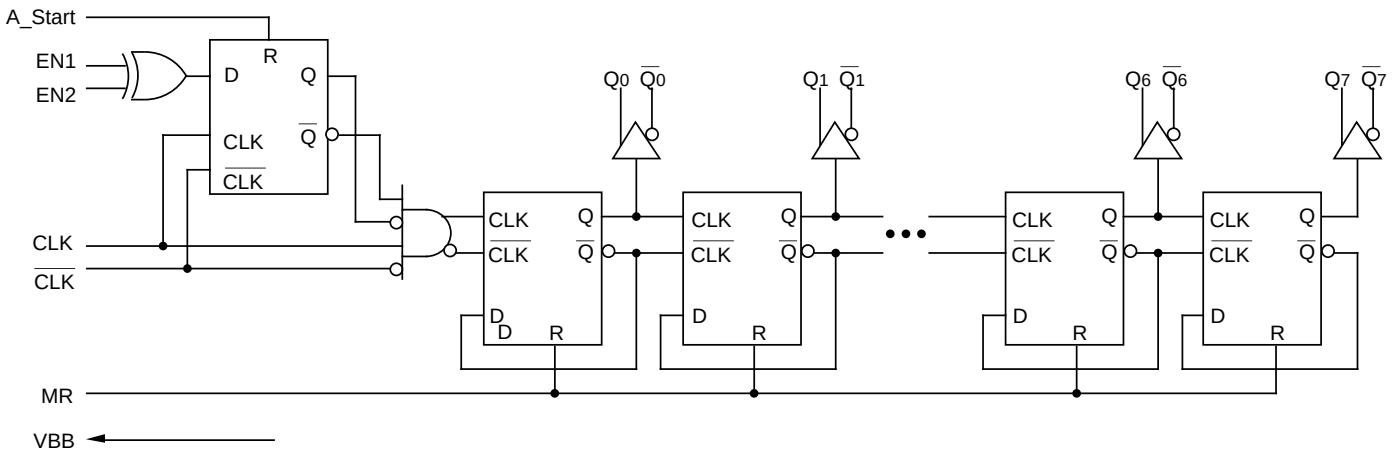
BLOCK DIAGRAM



SEQUENTIAL TRUTH TABLE(1)

Function	EN_1	EN_2	A_Start	MR	CLK	Q_7	Q_6	Q_5	Q_4	Q_3	Q_2	Q_1	Q_0
Reset	X	X	X	H	X	L	L	L	L	L	L	L	L
Count	L	L	L	L	Z	L	L	L	L	L	L	L	H
	L	L	L	L	Z	L	L	L	L	L	L	H	L
	L	L	L	L	Z	L	L	L	L	L	L	H	H
Stop	H	L	L	L	Z	L	L	L	L	L	L	H	H
	H	L	L	L	Z	L	L	L	L	L	L	H	H
Async. Start	H	L	H	L	Z	L	L	L	L	L	H	L	L
	H	L	H	L	Z	L	L	L	L	L	H	L	H
	L	L	H	L	Z	L	L	L	L	L	H	H	L
Count	L	L	L	L	Z	L	L	L	L	L	H	H	H
	L	L	L	L	Z	L	L	L	L	H	L	L	L
	L	L	L	L	Z	L	L	L	L	H	L	L	H
Stop	L	H	L	L	Z	L	L	L	L	H	L	L	H
	L	H	L	L	Z	L	L	L	L	H	L	L	H
Sync. Start	H	H	L	L	Z	L	L	L	L	H	L	H	L
	H	H	L	L	Z	L	L	L	L	H	L	H	H
	H	H	L	L	Z	L	L	L	L	H	H	L	L
Stop	H	L	L	L	Z	L	L	L	L	H	H	L	L
	H	L	L	L	Z	L	L	L	L	H	H	L	L
Count	L	L	L	L	Z	L	L	L	L	H	H	L	H
	L	L	L	L	Z	L	L	L	L	H	H	H	L
	L	L	L	L	Z	L	L	L	L	H	H	H	H
Reset	X	X	X	H	X	L	L	L	L	L	L	L	L

NOTE:

1. Z = LOW-to-HIGH transition

DC ELECTRICAL CHARACTERISTICS

V_{EE} = V_{EE} (Min.) to V_{EE} (Max.); V_{CC} = V_{CCO} = GND

Symbol	Parameter	T_A = 0°C			T_A = +25°C			T_A = +85°C			Unit	Condition
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
V_{BB}	Output Reference Voltage 10E	–1.38	—	–1.27	–1.35	—	–1.25	–1.31	—	–1.19	V	—
	100E	–1.38	—	–1.26	–1.38	—	–1.26	–1.38	—	–1.26		
I_{IH}	Input HIGH Current	—	—	150	—	—	150	—	—	150	µA	—
I_{EE}	Power Supply Current 10E	—	121	145	—	121	145	—	121	145	mA	—
	100E	—	121	145	—	121	145	—	139	167		

AC ELECTRICAL CHARACTERISTICS

V_{EE} = V_{EE} (Min.) to V_{EE} (Max.); V_{CC} = V_{CCO} = GND

Symbol	Parameter	T_A = 0°C			T_A = +25°C			T_A = +85°C			Unit	Condition
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
f_{COUNT}	Max. Count Frequency	1800	2200	—	1800	2200	—	1800	2200	—	MHz	—
t_{PLH} t_{PHL}	Propagation Delay to Output										ps	—
	CLK to Q_0	1300	1700	2150	1300	1700	2150	1350	1750	2200		
	CLK to Q_1	1600	2025	2500	1600	2050	2500	1650	2100	2550		
	CLK to Q_2	1950	2425	2925	1950	2450	2925	2025	2500	3000		
	CLK to Q_3	2275	2750	3350	2275	2775	3350	2350	2850	3425		
	CLK to Q_4	2625	3125	3750	2625	3150	3750	2700	3225	3625		
	CLK to Q_5	2950	3450	4150	2950	3475	4150	3050	3550	4250		
	CLK to Q_6	3250	3775	4450	3250	3800	4450	3375	3925	4600		
	CLK to Q_7	3575	4075	4800	3575	4125	4800	3700	4250	4950		
	A_Start to Q_0	950	1325	1700	950	1325	1700	950	1325	1700		
	MR to Q_0	700	1000	1300	700	1000	1300	700	1000	1300		
t_S	Set-up Time (EN_1, EN_2)	0	–150	—	0	–150	—	0	–150	—	ps	—
t_H	Hold Time (EN_1, EN_2)	300	150	—	300	150	—	300	150	—	ps	—
t_{RR}	Reset Recovery Time MR, A_Start	400	200	—	400	200	—	400	200	—	ps	—
t_{PW}	Minimum Pulse Width CLK, MR, A_Start	400	—	—	400	—	—	400	—	—	ps	—
V_{PP}	Minimum Input Swing (CLK)	0.25	—	1.0	0.25	—	1.0	0.25	—	1.0	V	1
V_{CMR}	Com. Mode Range (CLK)	–0.4	—	–2.0	–0.4	—	–2.0	–0.4	—	–2.0	V	—
t_r t_f	Rise/Fall Time, 20% to 80%										ps	—
	Q_0, Q_1	150	—	400	150	—	400	150	—	400		
	Q_2–Q_7	275	—	600	275	—	600	275	—	600		

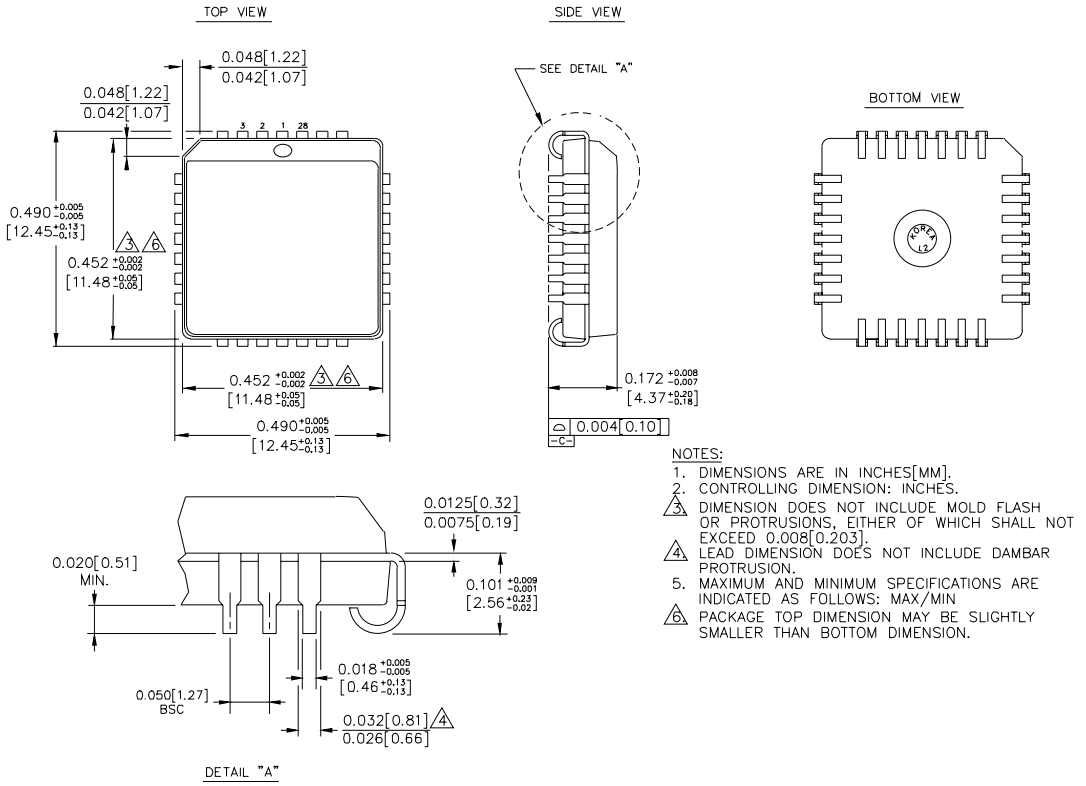
NOTE:

1. Minimum input swing for which AC parameters are guaranteed. Full DC ECL output swings will be generated with only 50mV input swings.

PRODUCT ORDERING CODE

Ordering Code	Package Type	Operating Range
SY10E137JC	J28-1	Commercial
SY10E137JCTR	J28-1	Commercial
SY100E137JC	J28-1	Commercial
SY100E137JCTR	J28-1	Commercial

28 LEAD PLCC (J28-1)



Rev. 03

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