

April 1988 Revised July 1999

74F74

Dual D-Type Positive Edge-Triggered Flip-Flop

General Description

The F74 is a dual D-type flip-flop with Direct Clear and Set inputs and complementary $(Q,\ \overline{Q})$ outputs. Information at the input is transferred to the outputs on the positive edge of the clock pulse. Clock triggering occurs at a voltage level of the clock pulse and is not directly related to the transition time of the positive-going pulse. After the Clock Pulse input threshold voltage has been passed, the Data input is locked out and information present will not be transferred to

the outputs until the next rising edge of the Clock Pulse input

Asynchronous Inputs:

 $\label{eq:lower} \mbox{LOW input to } \overline{S}_D \mbox{ sets Q to HIGH level} \\ \mbox{LOW input to } \overline{C}_D \mbox{ sets Q to LOW level} \\ \mbox{Clear and Set are independent of clock}$

Simultaneous LOW on \overline{C}_D and \overline{S}_D

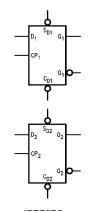
makes both Q and Q HIGH

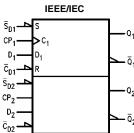
Ordering Code:

Order Number	Package Number	Package Description
74F74SC	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-120, 0.150 Narrow
74F74SJ	M14D	14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74F74PC	N14A	14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide

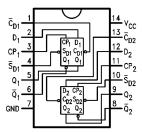
Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Logic Symbols





Connection Diagram



Unit Loading/Fan Out

D' M	Post data	U.L.	Input I _{IH} /I _{IL}	
Pin Names	Description	HIGH/LOW	Output I _{OH} /I _{OL}	
D ₁ , D ₂	Data Inputs	1.0/1.0	20 μA/–0.6 mA	
CP ₁ , CP ₂	Clock Pulse Inputs (Active Rising Edge)	1.0/1.0	20 μA/–0.6 mA	
\overline{C}_{D1} , \overline{C}_{D2}	Direct Clear Inputs (Active LOW)	1.0/3.0	20 μA/–1.8 mA	
\overline{S}_{D1} , \overline{S}_{D2}	Direct Set Inputs (Active LOW)	1.0/3.0	20 μA/–1.8 mA	
$Q_1, \overline{Q}_1, Q_2, \overline{Q}_2$	Outputs	50/33.3	−1 mA/20 mA	

Truth Table

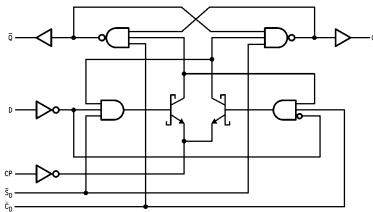
	Inp	Outputs			
S _D	¯C _D CP			Q	Q
L	Н	Х	Х	Н	L
Н	L	X	Χ	L	Н
L	L	X	Χ	Н	Н
Н	Н	~	h	Н	L
Н	Н	~	- 1	L	Н
Н	Н	L	X	Q_0	\overline{Q}_0

H (h) = HIGH Voltage Level L (I) = LOW Voltage Level X = Immaterial

 $Q_0 = Previous Q(\overline{Q})$ before LOW-to-HIGH Clock Transition

Lower case letters indicate the state of the referenced input or output one setup time prior to the LOW-to-HIGH clock transition.

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings(Note 1)

Recommended Operating Conditions

 $\begin{array}{ll} \mbox{Storage Temperature} & -65^{\circ}\mbox{C to } +150^{\circ}\mbox{C} \\ \mbox{Ambient Temperature under Bias} & -55^{\circ}\mbox{C to } +125^{\circ}\mbox{C} \\ \end{array}$

Junction Temperature under Bias -55° C to $+150^{\circ}$ C V_{CC} Pin Potential to Ground Pin -0.5V to +7.0V

Voltage Applied to Output

in HIGH State (with V_{CC} = 0V) Standard Output -0.5V to V_{CC}

3-STATE Output -0.5V to +5.5V

Current Applied to Output

in LOW State (Max) twice the rated I_{OL} (mA) ESD Last Passing Voltage (Min) 4000V

Free Air Ambient Temperature $0^{\circ}\text{C} \text{ to } +70^{\circ}\text{C}$ Supply Voltage +4.5V to +5.5V

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

DC Electrical Characteristics

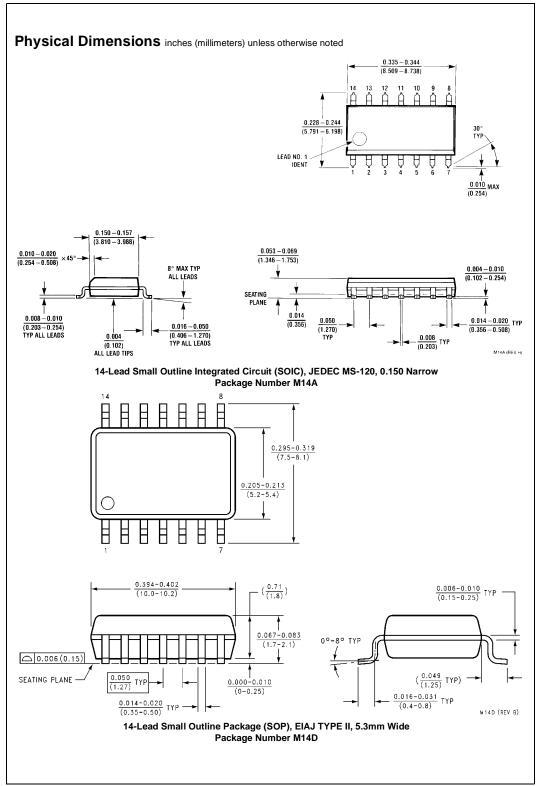
Symbol	Parameter		Min	Тур	Max	Units	v _{cc}	Conditions
V _{IH}	Input HIGH Voltage		2.0			V		Recognized as a HIGH Signal
V _{IL}	Input LOW Voltage				0.8	V		Recognized as a LOW Signal
V _{CD}	Input Clamp Diode Voltage				-1.2	V	Min	I _{IN} = -18 mA
V _{OH}	Output HIGH	10% V _{CC}	2.5			V	Min	I _{OH} = -1 mA
	Voltage	$5\% V_{CC}$	2.7			V	IVIIII	$I_{OH} = -1 \text{ mA}$
V _{OL}	Output LOW	10% V _{CC}			0.5	V	Min	I _{OL} = 20 mA
	Voltage							
I _{IH}	Input HIGH Current				5.0	μА	Max	V _{IN} = 2.7V
I _{BVI}	Input HIGH Current Breakdown Test				7.0	μА	Max	V _{IN} = 7.0V
I _{CEX}	Output HIGH Leakage Current				50	μА	Max	V _{OUT} = V _{CC}
V _{ID}	Input Leakage Test		4.75			V	0.0	I _{ID} = 1.9 μA All Other Pins Grounded
I _{OD}	Output Leakage Circuit Current				3.75	μА	0.0	V _{IOD} = 150 mV All Other Pins Grounded
I _{IL}	Input LOW Current				-0.6			V _{IN} = 0.5V (D, CP)
					-1.8	mA	Max	$V_{IN} = 0.5V (\overline{C}_D, \overline{S}_D)$
Ios	Output Short-Circuit Current		-60		-150	mA	Max	V _{OUT} = 0V
Icc	Power Supply Current			10.5	16.0	mA	Max	

AC Electrical Characteristics

Symbol	Parameter	$T_A = +25^{\circ}C$ $V_{CC} = +5.0V$ $C_L = 50 \text{ pF}$			$T_A = 0$ °C to +70°C $V_{CC} = +5.0V$ $C_L = 50 \text{ pF}$		Units	
		Min	Тур	Max	Min	Max		
f _{MAX}	Maximum Clock Frequency	100	125		100		MHz	
t _{PLH}	Propagation Delay	3.8	5.3	6.8	3.8	7.8		
t_{PHL}	CP_n to Q_n or \overline{Q}_n	4.4	6.2	8.0	4.4	9.2	ns	
t _{PLH}	Propagation Delay	3.2	4.6	6.1	3.2	7.1		
t _{PHL}	\overline{C}_{Dn} or \overline{S}_{Dn} to Q_n or \overline{Q}_n	3.5	7.0	9.0	3.5	10.5	ns	

AC Operating Requirements

Symbol	Parameter	$T_A = +25$ °C $V_{CC} = +5.0V$		$T_A = 0^{\circ}C \text{ to } +70^{\circ}C$ $V_{CC} = +5.0V$		Units
		Min	Max	Min	Max	1
t _S (H)	Setup Time, HIGH or LOW	2.0		2.0		
t _S (L)	D _n to CP _n	3.0		3.0		
t _H (H)	Hold Time, HIGH or LOW	1.0		1.0		ns
t _H (L)	D _n to CP _n	1.0		1.0		
t _W (H)	CP _n Pulse Width	4.0		4.0		
$t_W(L)$	HIGH or LOW	5.0		5.0		ns
t _W (L)	C _{Dn} or S _{Dn} Pulse Width	4.0		4.0		ns
	LOW					
t _{REC}	Recovery Time	2.0		2.0		ns
	\overline{C}_{Dn} or \overline{S}_{Dn} to CP					



Physical Dimensions inches (millimeters) unless otherwise noted (Continued) 0.740 - 0.770 (18.80 - 19.56)0.090 (2.286) 14 13 12 11 10 9 8 14 13 12 INDEX AREA 0.250 ± 0.010 (6.350 ± 0.254) PIN NO. 1 PIN NO. 1 IDENT 1 2 3 4 5 6 7 1 2 3 $\frac{0.092}{(2.337)}$ DIA 0.030 MAX (0.762) DEPTH OPTION 1 OPTION 02 $\frac{0.135 \pm 0.005}{(3.429 \pm 0.127)}$ 0.300 - 0.320 $\frac{0.630 - 8.128}{(7.620 - 8.128)}$ 0.060 0.145 - 0.2004° TYP Optional (1.651) (3.683 - 5.080) $\frac{0.008 - 0.016}{(0.203 - 0.406)}$ TYP 0.020 (0.508) 0.125 - 0.150 0.075 ± 0.015 $\overline{(3.175 - 3.810)}$ (1.905 ± 0.381) (7.112) MIN 0.014 - 0.0230.100 ± 0.010 (2.540 ± 0.254) (0.356 - 0.584) $\frac{0.050 \pm 0.010}{(1.270 - 0.254)}$ TYP 0.325 ^{+0.040} -0.015

14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide Package Number N14A

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8.255 + 1.016

N14A (REV F)

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