3.3V, 2GHz ANY-DIFFERENTIAL INPUT-TO-LVDS 1:4 FANOUT BUFFER/ TRANSLATOR W/ INTERNAL TERMINATION

Precision Edge™
SY89833L

Precision Edge™

FEATURES

- **Accepts any differential input signal and provides four LVDS output copies**
- **Guaranteed AC performance over temperature and voltage:**
  - **> 2.0GHz f_{MAX}**
  - **< 20ps within-device skew**
  - **< 190ps rise/fall times**
- **Low jitter design**
  - **< 1ps(rms) cycle-to-cycle jitter**
  - **< 10ps(pk-pk) total jitter**
- **3.3V power supply operation**
- **TTL/CMOS input for enable**
- **Unique input termination and V_T pin accepts DC-coupled and AC-coupled inputs (CML, PECL, LVDS, and HSTL)**
- **High-speed LVDS outputs**
- **Wide operating temperature range: –40°C to +85°C**
- **Available in 16-pin (3mm × 3mm) MLF™ package**

APPLICATIONS

- **Processor clock distribution**
- **SONET clock distribution**
- **Fibre Channel clock distribution**
- **Gigabit Ethernet clock distribution**

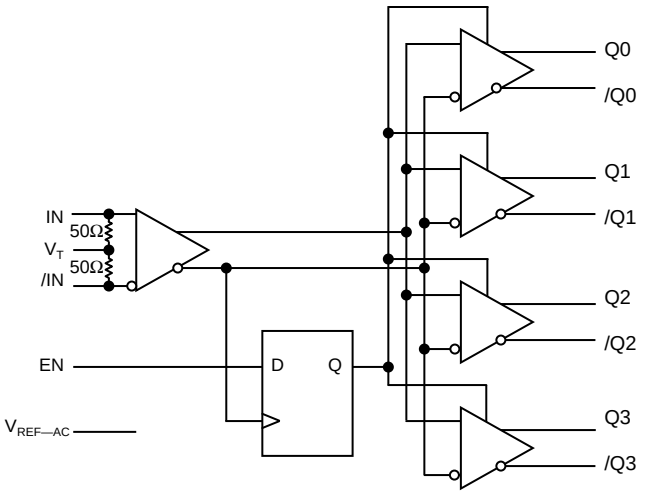
DESCRIPTION

The SY89833L is a 3.3V, high-speed 2GHz differential Low Voltage Differential Swing (LVDS) 1:4 fanout buffer optimized for ultra-low skew applications. Within device skew is guaranteed to be less than 20ps over supply voltage and temperature.

The differential input buffer has a unique internal termination design that allows access to the termination network through a V_T pin. This feature allows the device to easily interface to different logic standards. A V_{REF_AC} reference is included for AC-coupled applications.

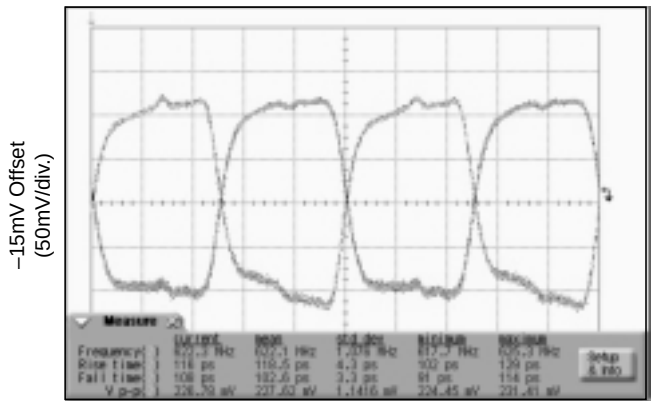
The SY89833L is part of Micrel's high-speed clock synchronization family. For 2.5V applications, the SY89832U provides similar functionality while operating from a 2.5V ±5% supply. For applications that require a different I/O combination, consult the Micrel website at *www.micrel.com*, and choose from a comprehensive product line of high-speed, low-skew fanout buffers, translators and clock generators.

FUNCTIONAL BLOCK DIAGRAM



TYPICAL PERFORMANCE

622MHz Output



TIME (321.9ps/div.)

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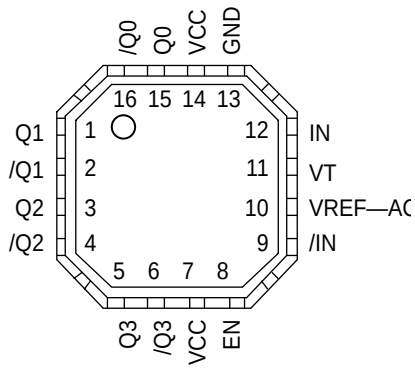
*Micro*LeadFrame and MLF are trademarks of Amkor Technology, Inc.

Rev.: D Amendment: /0
Issue Date: February 2003

PACKAGE/ORDERING INFORMATION



16-Pin MLF™

Ordering Information

Part Number	Package Type	Operating Range	Package Marking
SY89833LMI	MLF-16	Industrial	833L
SY89833LMITR*	MLF-16	Industrial	833L

*Tape and Reel

PIN DESCRIPTION

Pin Number	Pin Name	Pin Function
15, 16, 1, 2, 3, 4, 5, 6	(Q0, /Q0) to (Q3, /Q3)	LVDS Differential (Outputs): Normally terminated with 100Ω across the pair (Q, /Q). See *"LVDS Outputs"* section, Figure 2a. Unused outputs should be terminated with a 100Ω resistor across each pair.
8	EN	TTL/CMOS Compatible Synchronous Enable: When EN goes LOW, Q outputs will go LOW and /Q outputs will go HIGH on the next LOW transition at IN inputs. Input threshold is V_{CC}/2V. A 25kΩ pull-up resistor is included. The default state is HIGH when left floating. The internal latch is clocked on the falling edge of the input signal (IN, /IN).
9, 12	/IN, IN	Differential Clock (Inputs): Internal 50Ω termination resistors to the V_T pin. See *"Input Interface Applications"* section.
10	VREF–AC	Reference Voltages: Equals to V_{CC}–1.4V, and is used for AC-coupled applications. The maximum sink/source current is 0.5mA. See *"Input Interface Applications."* When using $V_{REF–AC}$, bypass with a 0.01µF capacitor to V_{CC}.
11	VT	Termination Center-Tap. For CML or LVDS inputs, leave this pin floating. See Figures 3a to 3f. See *"LVDS Outputs"* Figures 2a and 2b for LVDS differential and common mode measurements.
13, Exposed Pad	GND	Ground. Exposed pad internally connected to GND and must be connected to a ground plane for proper thermal operation.
7, 14	VCC	Positive Power Supply: Bypass with 0.1µF//0.01µF low ESR capacitors.

TRUTH TABLE

IN	/IN	EN	Q	/Q
0	1	1	0	1
1	0	1	1	0
X	X	0	0(1)	1(1)

Note 1. On next negative transition of the input signal (IN).

Absolute Maximum Ratings(Note 1)

Supply Voltage (V_{CC}) ..... –0.5V to +4.0V
Input Voltage (V_{IN}) ..... –0.5V to V_{CC} +0.3V
Output Current (I_{OUT}) ..... ±10mA
Input Current (IN, /IN) ..... ±50mA
V_T Current (I_{VT}) ..... ±100mA
Input Sink/Source Current ($V_{REF–AC}$), **Note 3** ..... ±2mA
Lead Temperature (Soldering, 10 sec.) ..... 220°C
Storage Temperature (T_S) ..... –65°C to +150°C

Operating Ratings(Note 2)

Supply Voltage Range ..... +2.97V to +3.63V
Ambient Temperature (T_A) ..... –40°C to +85°C
Package Thermal Resistance
MLF™ (θ_{JA})
Still-Air ..... 60°C/W
500lfpm ..... 54°C/W
MLF™ (ψ_{JB}), **Note 4** ..... 32°C/W

Note 1. Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to ABSOLUTE MAXIMUM RATING conditions for extended periods may affect device reliability.

Note 2. The data sheet limits are not guaranteed if the device is operated beyond the operating ratings.

Note 3. Due to the limited drive capability use for input of the same package only.

Note 4. Junction-to-board resistance assumes exposed pad is soldered (or equivalent) to the device's most negative potential on the PCB.

DC ELECTRICAL CHARACTERISTICS(Note 1, 2)

T_A = –40°C to +85°C

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{CC}	Power Supply Voltage Range		2.97	3.3	3.63	V
I_{CC}	Power Supply Current	No Load		75	100	mA
R_{IN}	Differential Input Resistance (IN, /IN)		80	100	120	Ω
V_{IH}	Input HIGH Voltage (IN, /IN)	**Note 3**	0.1		V_{CC}+0.3	V
V_{IL}	Input LOW Voltage (IN, /IN)	**Note 3**	–0.3		V_{CC}+0.2	V
V_{IN}	Input Voltage Swing	**Note 3,** see Figure 2c V_{IN} (max), V_T = floating.	0.1		3.6	V
V_{DIFF_IN}	Differential Input Voltage	**Note 3,** see Figure 2d	0.2			V
$\|I_{IN}\|$	Input Current (IN, /IN)	**Note 3**			45	mA
$V_{REF–AC}$	Reference Voltage	**Note 3**	V_{CC}–1.525	V_{CC}–1.425	V_{CC}–1.325	V

Note 1. The circuit is designed to meet the DC specifications shown in the above table after thermal equilibrium has been established.

Note 2. Specification for packaged product only.

Note 3. Due to the internal termination (see *"Differential Input"*) the input current depends on the applied voltages at IN, /IN and V_T inputs. Do not apply a combination of voltages that causes the input current to exceed the maximum limit.

LVDS OUTPUTS DC ELECTRICAL CHARACTERISTICS(Note 1, 2)

V_{CC} = 3.3V ±10%, T_A = –40°C to +85°C

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{OH}	Output HIGH Voltage	**Note 3**			1.475	V
V_{OL}	Output LOW Voltage	**Note 3**	0.925			V
V_{OCM}	Output Common Mode Voltage		1.125		1.275	V
ΔV_{OCM}	Change in Common Mode Voltage		–50		50	mV
V_{OUT}	Single-Ended Output	see Figures 2c-2d	250	350	450	mV
V_{DIFF_OUT}	Differential Output	see Figures 2c-2d	500	700	900	mV

Note 1. The circuit is designed to meet the DC specifications shown in the above table after thermal equilibrium has been established.

Note 2. Specification for packaged product only.

Note 3. Measured as per Figure 2a, 100Ω across Q and /Q outputs.

LVTTL/CMOS INPUTS DC ELECTRICAL CHARACTERISTICS(Note 1, 2)

V_{CC} = 3.3V ±10%, T_A = –40°C to +85°C

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{IH}	Input HIGH Voltage		2.0		V_{CC}	V
V_{IL}	Input LOW Voltage		0		0.8	V
I_{IH}	Input HIGH Current		–125		20	µA
I_{IL}	Input LOW Current				–300	µA

Note 1. The circuit is designed to meet the DC specifications shown in the above table after thermal equilibrium has been established.

Note 2. Specification for packaged product only.

AC ELECTRICAL CHARACTERISTICS[Note 1, 2]

V_{CC} = 3.3V ±10%, T_A = –40°C to +85°C

Symbol	Parameter	Condition	Min	Typ	Max	Units
f_{MAX}	Maximum Frequency	≥200mVpp Output Swing	2.0			GHz
t_{PLH} t_{PHL}	Differential Propagation (Delay) (IN-to-Q)	Input Swing: <400mV	400	500	600	ps
		Input Swing: ≥400V	330	440	530	ps
t_{SKEW}	Within-Device Skew (Differential)	**Note 3**		5	20	ps
	Part-to-Part Skew (Differential)				200	ps
t_S	Set-Up Time (EN to IN, /IN)	**Note 4 and Note 5**	300			ps
t_H	Hold Time (EN to IN, /IN)	**Note 4 and Note 5**	500			ps
t_{JITTER}	Cycle-to-Cycle Jitter (rms)	**Note 6**			1	ps(rms)
	Total Jitter	**Note 7**			10	ps(pk-pk)
t_r, t_f	Output Rise/Fall Times (20% to 80%)		60	110	190	ps

Note 1. Measured with 400mV input signal, 50% duty cycle, all outputs are loaded with 100Ω between Q and /Q. Output swing is ≥ 200mV.

Note 2. Specification for packaged product only.

Note 3. Skew is measured between outputs under identical transitions.

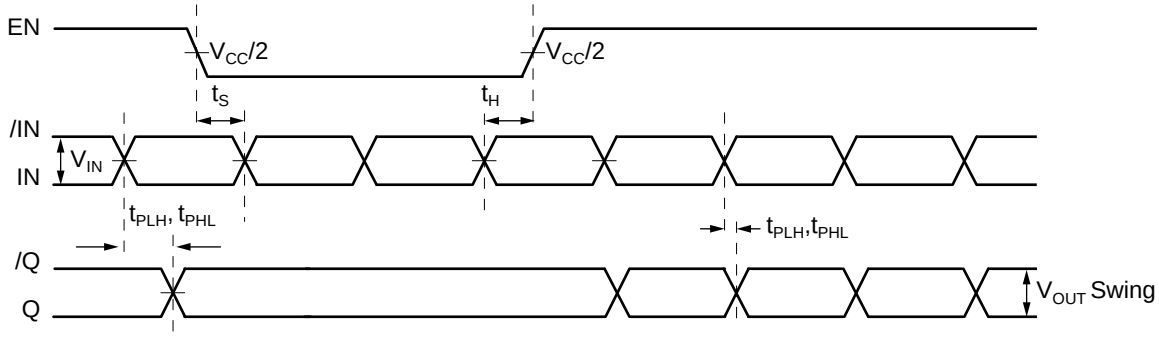
Note 4. Set-up and hold times apply to synchronous applications that intend to enable/disable before the next clock cycle. For asynchronous applications set-up and hold times do not apply.

Note 5. See *"Timing Diagram."*

Note 6. Cycle-to-cycle jitter definition: The variation period between adjacent cycles over a random sample of adjacent cycle pairs. $T_{JITTER\_CC} = T_n - T_{n+1}$ where T is the time between rising edges of the output signal.

Note 7. Total jitter definition: with an ideal clock input frequency of ≤ f_{MAX} (device), no more than one output edge in 10^{12} output edges will deviate by more than the specified peak-to-peak jitter value.

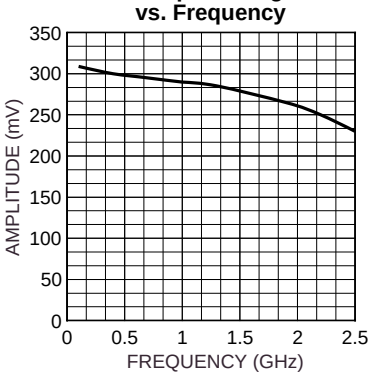
TIMING DIAGRAM



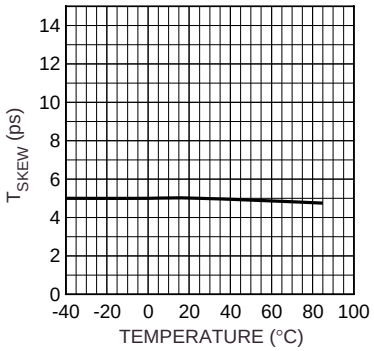
TYPICAL OPERATING CHARACTERISTICS

V_{CC} = 3.3V, V_{IN} = 400mV, T_A = 25°C, unless otherwise stated.

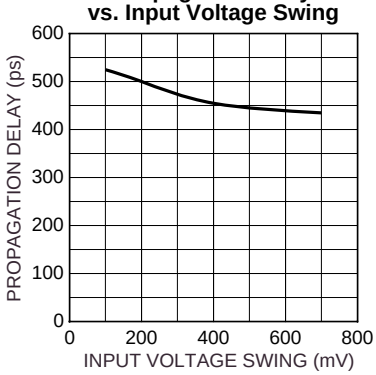
Output Swing vs. Frequency



T_{SKEW} vs. Temperature



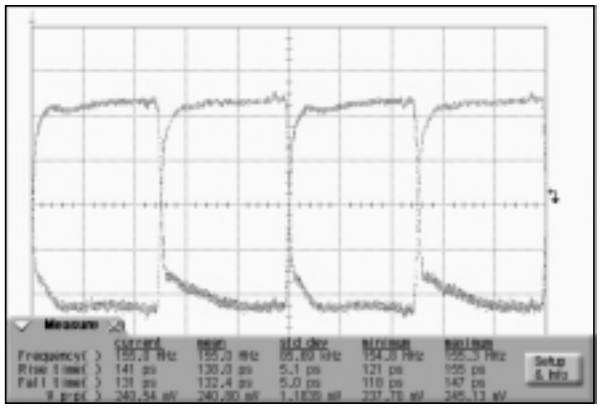
Propagation Delay vs. Input Voltage Swing



FUNCTIONAL CHARACTERISTICS

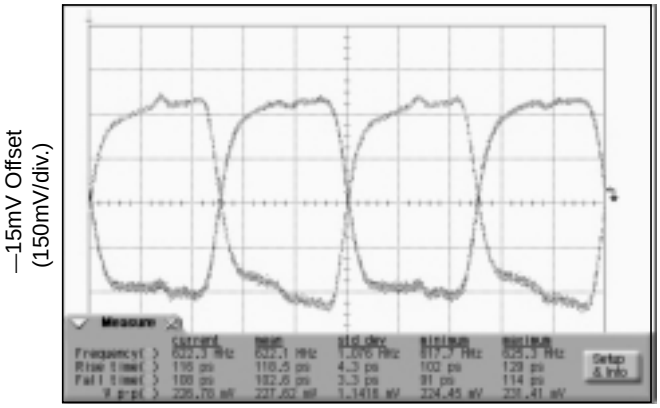
V_{CC} = 3.3V, V_{IN} = 400mV, T_A = 25°C, unless otherwise stated.

155MHz Output



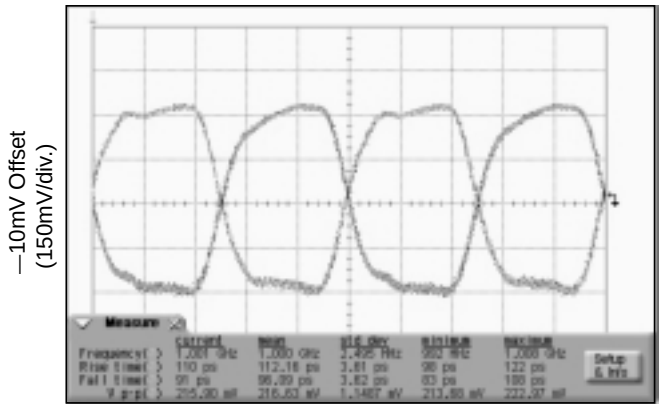
TIME (1.29ns/div.)

622MHz Output



TIME (321.9ps/div.)

1GHz Output



TIME (200ps/div.)

INPUT STAGE

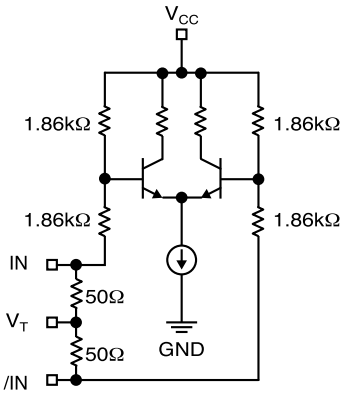


Figure 1a. Simplified Differential Input Buffer

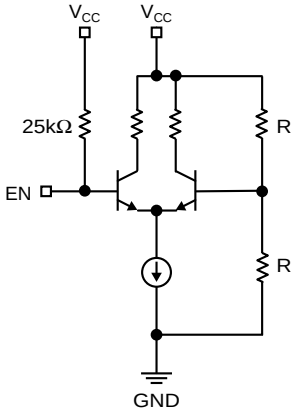


Figure 1b. Simplified TTL/CMOS Input Buffer

LVDS OUTPUTS

LVDS specifies a small swing of 350mV typical, on a nominal 1.25V common mode above ground. The common mode voltage has tight limits to permit large variations in ground noise between an LVDS driver and receiver.

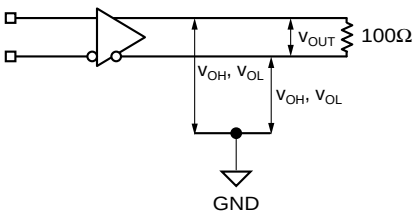


Figure 2a. LVDS Differential Measurement

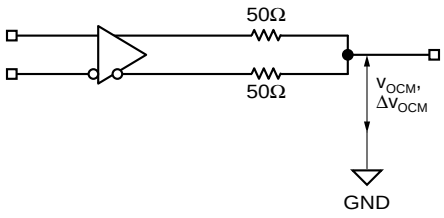


Figure 2b. LVDS Common Mode Measurement

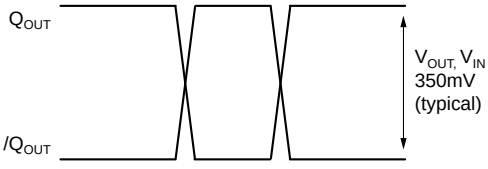


Figure 2c. Single-Ended Swing

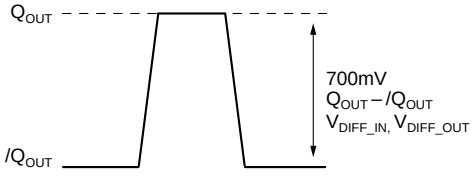


Figure 2d. Differential Swing

INPUT INTERFACE APPLICATIONS

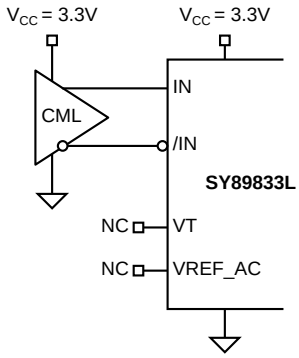


Figure 3a. DC-Coupled CML Input Interface

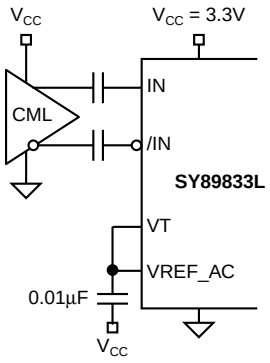


Figure 3b. AC-Coupled CML Input Interface

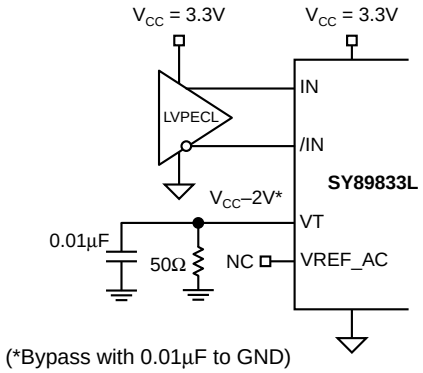


Figure 3c. DC-Coupled PECL Input Interface

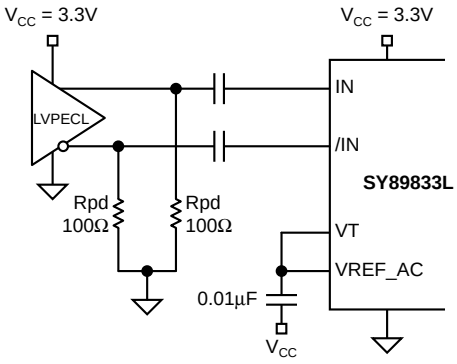


Figure 3d. AC-Coupled PECL Input Interface

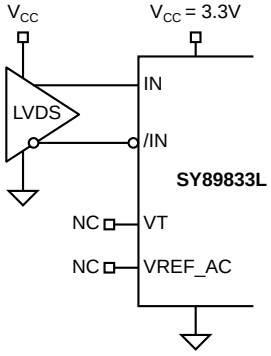


Figure 3e. LVDS Input Interface

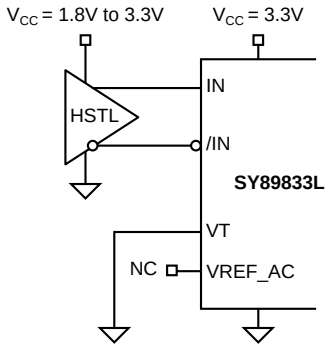
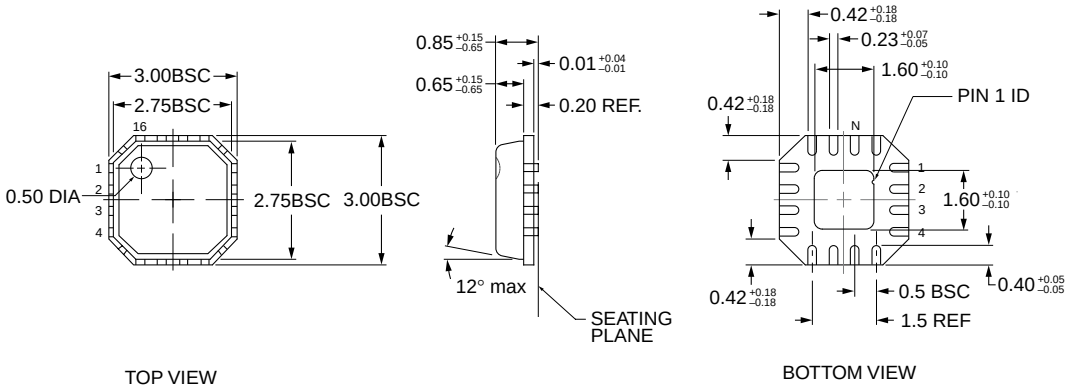


Figure 3f. HSTL Input Interface

RELATED PRODUCT AND SUPPORT DOCUMENTS

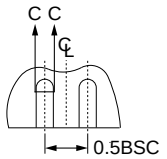
Part Number	Function	Data Sheet Link
SY89830U	2.5V/3.3V/5V 2.5GHz 1:4 PECL/ECL Clock Driver with 2:1 Differential Input Mux	http://www.micrel.com/product-info/products/sy89830u.shtml
SY89831U	2GHz Ultra Low-Jitter and Skew 1:4 LVPECL Fanout Buffer/Translator w/ Internal Termination	http://www.micrel.com/product-info/products/sy89831u.shtml
SY89832U	2GHz Ultra Low-Jitter and Skew 1:4 LVPECL Fanout Buffer/Translator w/ Internal Termination	http://www.micrel.com/product-info/products/sy89832u.shtml
SY89833U	2GHz ANY DIFFERENTIAL INPUT-to-LVDS Out 1:4 Fanout Buffer Translator w/ Internal Termination	http://www.micrel.com/product-info/products/sy89833u.shtml
	16-MLF™ Manufacturing Guidelines Exposed Pad Application Note	http://www.amkor.com/products/notes_papers/MLF_appnote_0301.pdf
HBW Solutions	New Products and Termination App. Note	http://www.micrel.com/product-info/as/solutions.shtml

16 LEAD EPAD *Micro*LeadFrame™ (MLF-16)

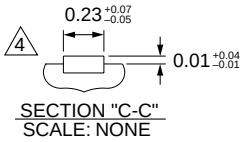


TOP VIEW

BOTTOM VIEW



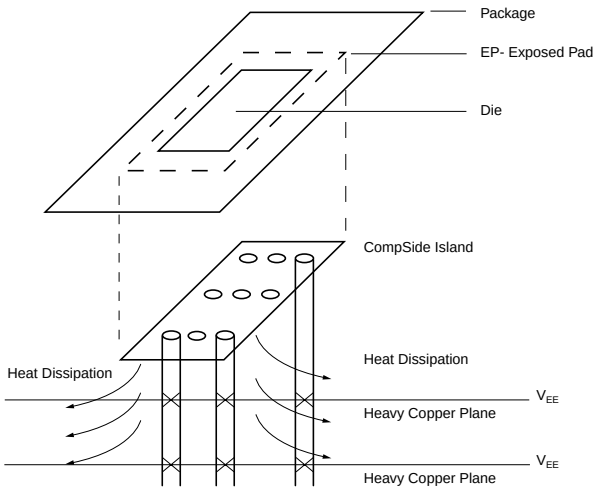
FOR EVEN TERMINAL/SIDE



SECTION "C-C"
SCALE: NONE

1. DIMENSIONS ARE IN mm.
2. DIE THICKNESS ALLOWABLE IS 0.305mm MAX.
3. PACKAGE WARPAGE MAX 0.05mm.
4. THIS DIMENSION APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.20mm AND 0.25mm FROM TIP.
5. APPLIES ONLY FOR TERMINALS

Rev. 02



PCB Thermal Consideration for 16-Pin MLF™ Package
(Always solder, or equivalent, the exposed pad to the PCB)

Package Notes:

Note 1. Package meets Level 2 moisture sensitivity classification, and are shipped in dry-pack form.
Note 2. Exposed pads must be soldered to a ground for proper thermal management.

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