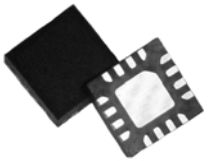
Preliminary

STA-6033

4.9 – 5.9 GHz 3.3V Power Amplifier



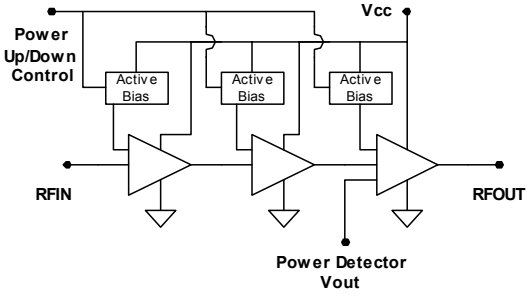
16 pin 3mm x 3mm QFN

Product Description

Sirenza Microdevices' STA-6033 is a high efficiency class AB Heterojunction Bipolar Transistor (HBT) amplifier housed in a low-cost surface-mountable plastic package. This HBT amplifier is made with InGaP on GaAs device technology and fabricated with MOCVD for an ideal combination of low cost and high reliability.

This product is specifically designed as a final stage for 802.11a equipment in the 4.9 - 5.9 GHz band. It can run from a 3.0V to 3.6V supply. Optimized on-chip impedance matching circuitry provides a 50Ω nominal RF input impedance. A single external output matching circuit covers the entire 4.9-5.9GHz band. The external output match allows for load line optimization for other applications or optimized performance over narrower bands. It is designed as a drop in replacement for similar parts in its class.

Functional Block Diagram



Product Features

- **802.11a 54Mb/s Class AB Performance**
  Pout = 18dBm @ 3% EVM, 3.3V, 210mA
- **High Gain = 27dB**
- **Output Return Loss < -12dB for Linear Tune**
- **On-chip Output Power Detector**
- **Simultaneous 4.9- 5.9GHz Broadband**
- **Pin Compatible with Microsemi LX5506**
- **Robust - Survives RF Input Power = +20dBm**
- **Power up/down control < 1μs**

Applications

- **802.11a WLAN, OFDM**
- **General purpose 5.8GHz ISM Band**
- **802.16 WiMax, Fixed Wireless, UNII**

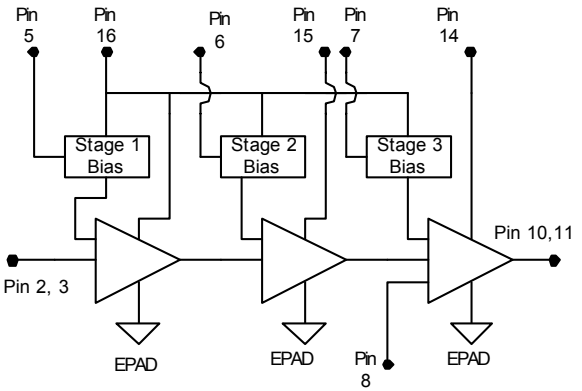
Key Specifications

Symbol	Parameters: Test Conditions, App circuit page 4 Z_0 = 50Ω, V_{CC} = Vpc = 3.3V, Icq = 165mA, T_{BP} = 30ºC	Unit	Min.	Typ.	Max.
f_O	Frequency of Operation	MHz	4900		5900
P_{1dB}	Output Power at 1dB Compression – 4.9 GHz	dBm		26.5	
	Output Power at 1dB Compression – 5.875 GHz		24.0	25.5	
S_{21}	Gain at 4.9 GHz	dB	28.0	30.0	32.0
	Gain at 5.875 GHz		23.6	25.6	27.6
Pout	Output power at 3% EVM 802.11a 54Mb/s - 5.15GHz	dBm		18	
	Output Power at 3% EVM 802.11a 54Mb/s - 5.875GHz			18	
IM3	Third Order Intermod at Pout=15dBm per tone - 5.875GHz	dBc		-38	-34
NF	Noise Figure at 5.875 GHz	dB		5.7	
IRL	Worst Case Input Return Loss 4.9-5.875GHz	dB	11	15	
ORL	Worst Case Output Return Loss 4.9-5.875GHz		8	12	
Vdet Range	Output Voltage Range for Pout=7dBm to 23dBm	V		0.8 to 1.5	
Icq	Vcc Quiescent Current	mA	140	165	190
I_{VPC}	Power Up Control Current,Vpc=3.3V (I_{VPC1} + I_{VPC2} + I_{VPC3})	mA		1.5	
$R_{th, j-l}$	Thermal Resistance (junction - lead)	ºC/W		28	

Pin Out Description

Pin #	Function	Description
1,4,9,12,13	N/C	Pins are not used. May be grounded, left open, or connected to adjacent pin.
5	VPC1	VPC1 is the bias control pin for the stage 1 active bias circuit. An external series resistor is required for proper setting of bias levels. Refer to the evaluation board schematic for resistor value. To prevent potential damage, do not apply voltage to this pin that is +1V greater than voltage applied to pin 16 (Vbias) unless Vpc supply current capability is less than 10 mA.
6	VPC2	VPC2 is the bias control pin for the stage 2 active bias circuit. An external series resistor is required for proper setting of bias levels. Refer to the evaluation board schematic for resistor value. To prevent potential damage, do not apply voltage to this pin that is +1V greater than voltage applied to pin 16 (Vbias) unless Vpc supply current capability is less than 10 mA.
7	VPC3	VPC3 is the control pin for the stage 3 active bias circuits. An external series resistor is required for proper setting of bias levels. Refer to the evaluation board schematic for resistor value. To prevent potential damage, do not apply voltage to this pin that is +1V greater than voltage applied to pin 16 (Vbias) unless Vpc supply current capability is less than 10 mA.
8	Vdet	Ouput power detector voltage. Load with 10K-100K ohms to ground for best performance.
2,3	RFIN	RF input pins. This is DC grounded internal to the IC. Do not apply voltage to this pin. All three pins must be used for proper operation.
10,11	RFOUT	RF output pin. This is also another connection to the 3rd stage collector
14	VC3	3rd stage collector bias pin. Apply 3.0V to 3.6V to this pin.
15	VC2	2nd stage collector bias pin. Apply 3.0V to 3.6V to this pin.
16	VC1,Vbias	1st stage collector bias pin and active bias network VCC. Apply 3.0V to 3.6V to this pin.
EPAD	Gnd	Exposed area on the bottom side of the package needs to be soldered to the ground plane of the board for optimum thermal and RF performance. Several vias should be located under the EPAD as shown in the recommended land pattern (page 5).

Simplified Device Schematic



Absolute Maximum Ratings

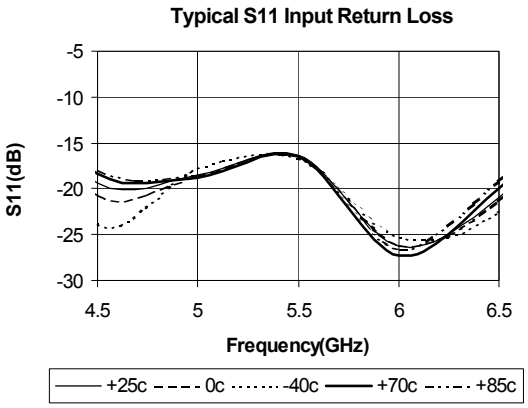
Parameters	Value	Unit
VC3 Collector Bias Current (pin16)	400	mA
VC2 Collector Bias Current (pin18)	140	mA
VC1 Collector Bias Current (pin19)	50	mA
Device Voltage (V_D)	4.5	V
Power Dissipation	1.4	W
Operating Lead Temperature (T_L)	-40 to +85	ºC
RF Input Power for 50 ohm load	20	dBm
Storage Temperature Range	-40 to +150	ºC
Operating Junction Temperature (T_J)	+150	ºC
ESD Human Body Model	>1000	V

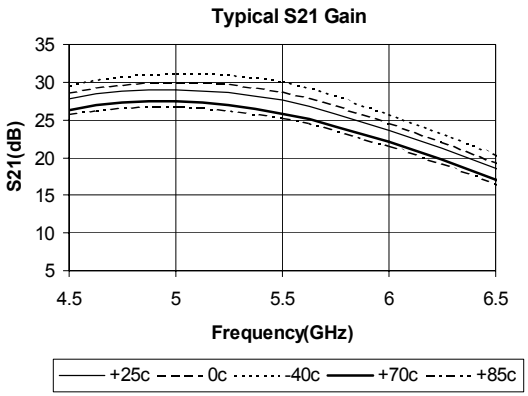
Operation of this device beyond any one of these limits may cause permanent damage. For reliable continuous operation the device voltage and current must not exceed the maximum operating values specified in the table on page one.

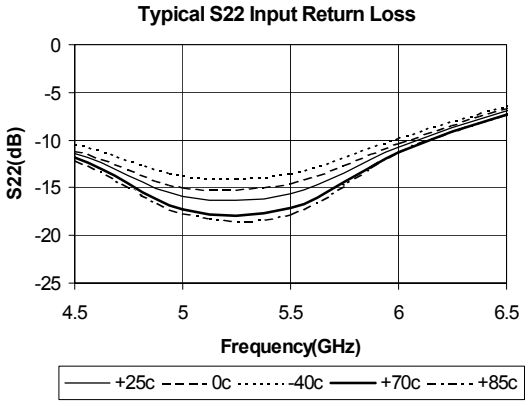
Bias conditions should also satisfy the following expression:
$I_D V_D < (T_J - T_L) / R_{TH, j-l}$

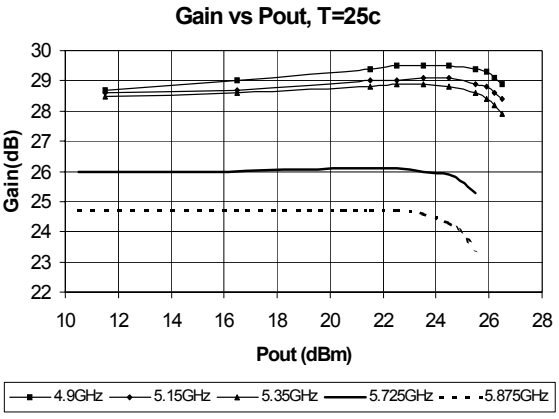
Caution: ESD Sensitive
Appropriate precaution in handling, packaging and testing devices must be observed.

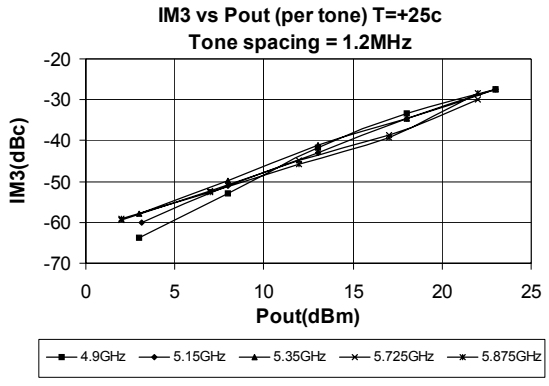
4.9 - 5.9 GHz Evaluation Board Data (Vcc = Vpc = 3.3V, I_q = 165mA)











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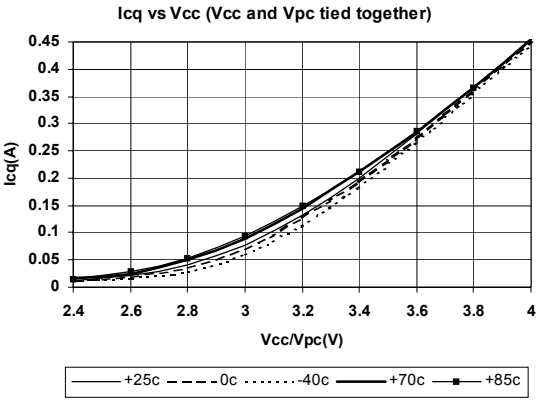
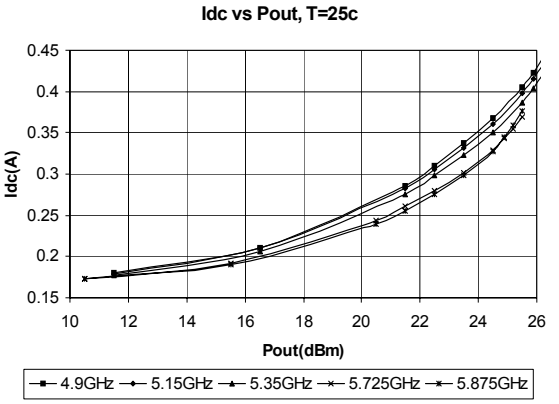
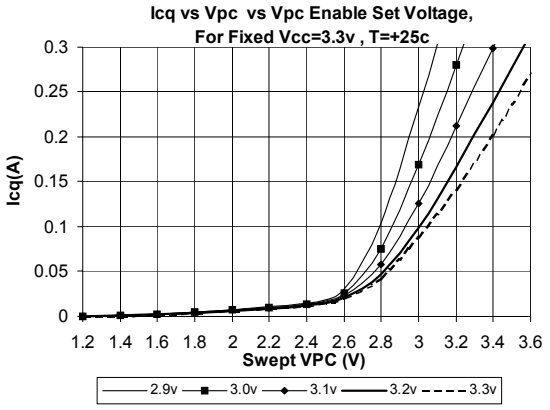
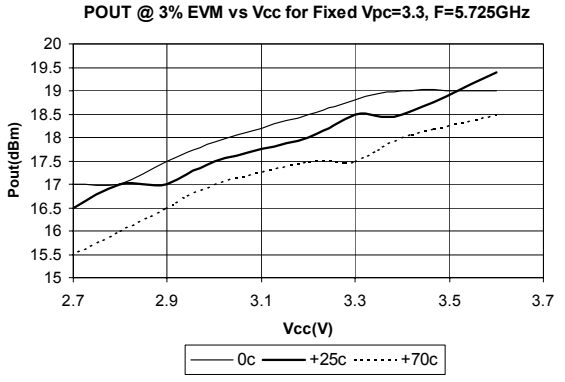
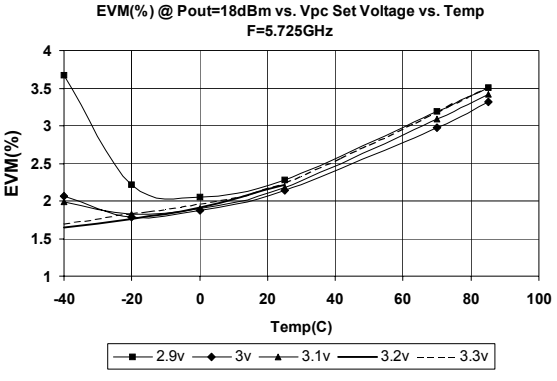
4.9 - 5.9 GHz Evaluation Board Data (Vcc = 3.3V, I_q = 165mA)











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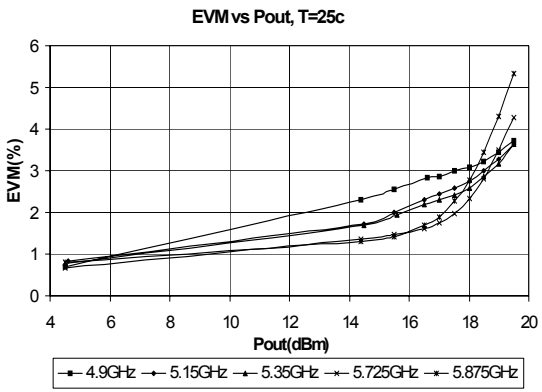
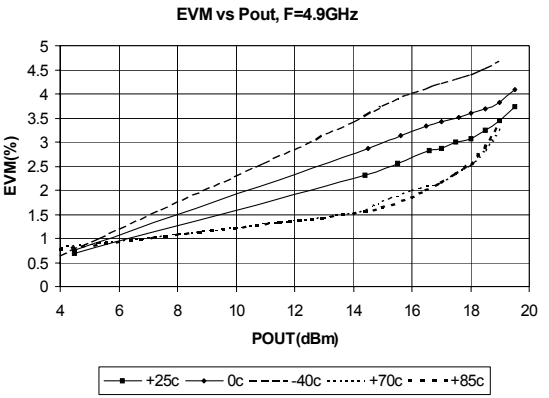
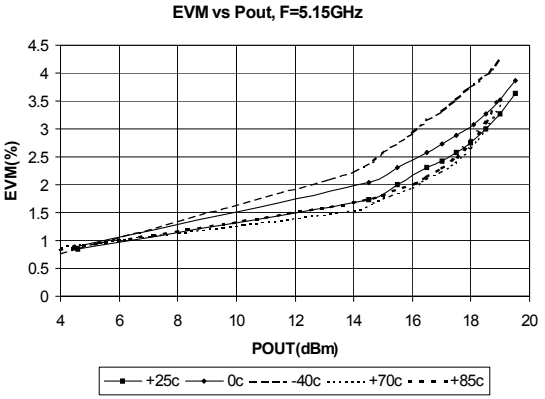
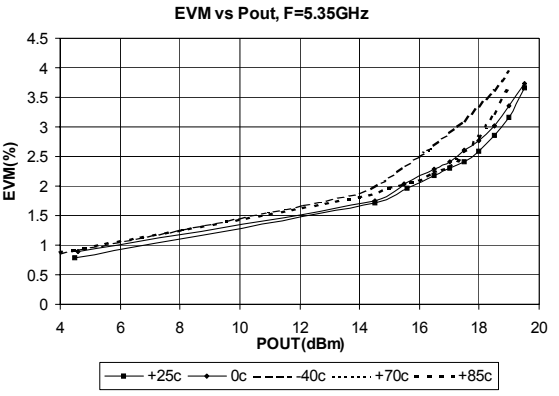
4.9 - 5.9 GHz Evaluation Board Data (Vcc = Vpc = 3.3V, I_q = 165mA)

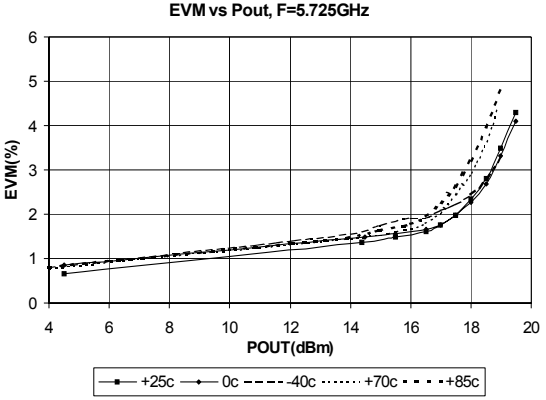
802.11a EVM, OFDM, 54Mb/s, 64QAM

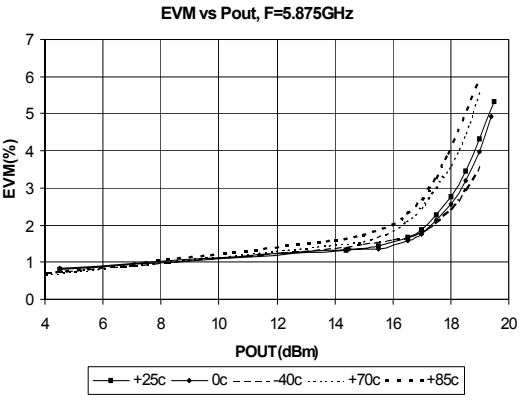












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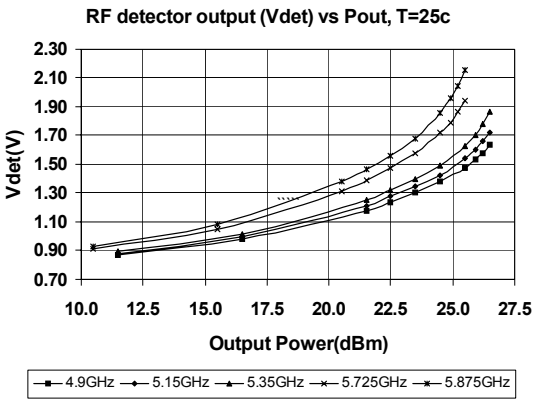
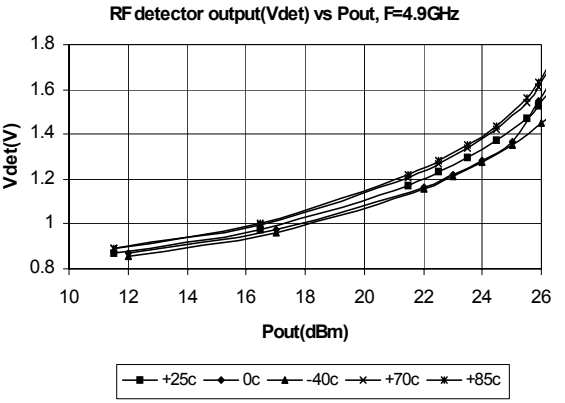
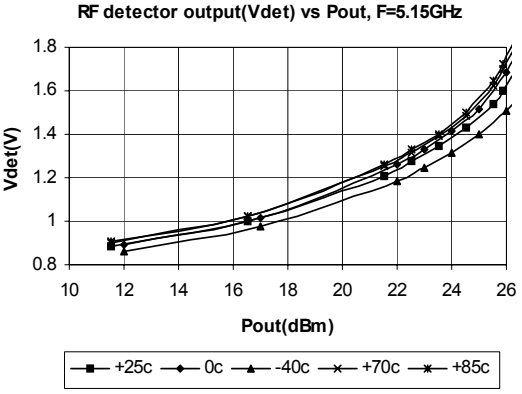
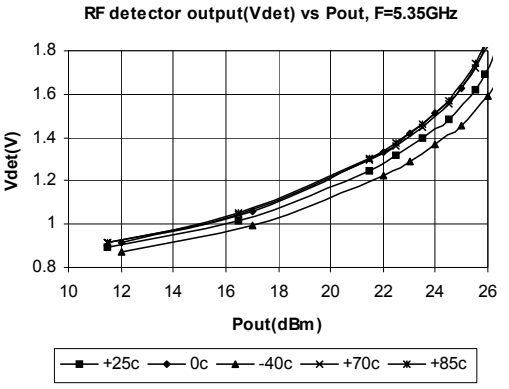
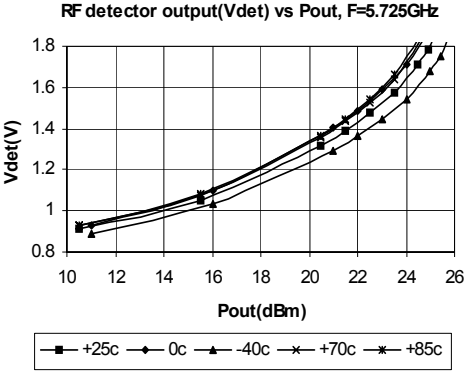
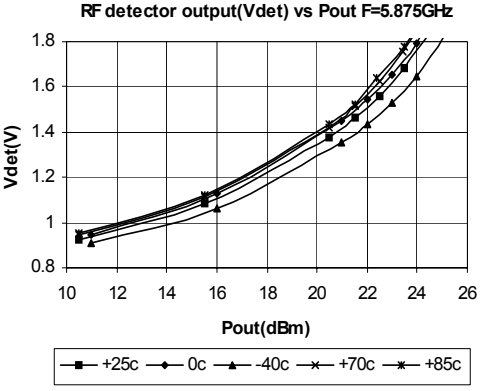




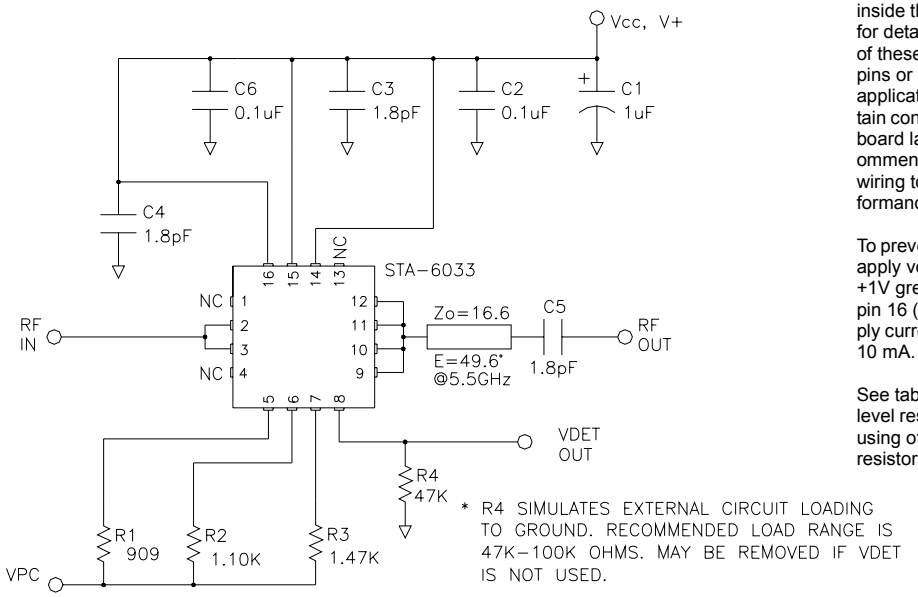








4.9 - 5.9 GHz Evaluation Board Schematic For Vcc = Vpc = V+ = 3.3V Supply



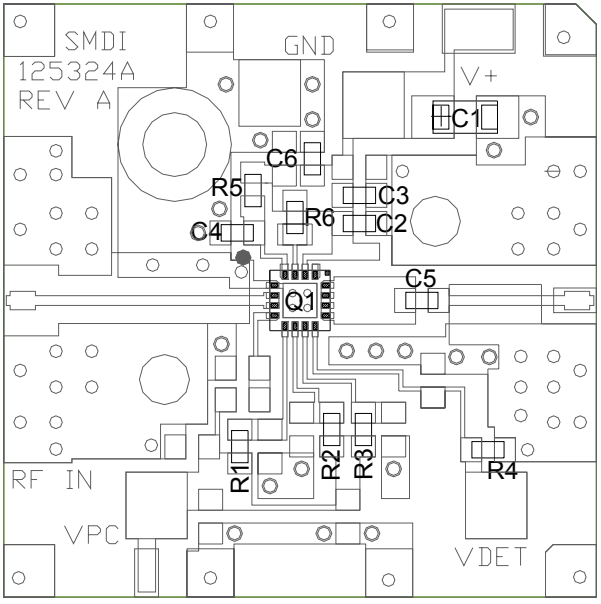
Notes:
Pins 1,4,9,12,13 are unwired (N/C) inside the package. Refer to page 2 for detailed pin descriptions. Some of these pins are wired to adjacent pins or grounded as shown in the application circuit. This is to maintain consistency with the evaluation board layout shown below. It is recommended to use this layout and wiring to achieve the specified performance.

To prevent potential damage, do not apply voltage to the Vpc pin that is +1V greater than voltage applied to pin 16 (Vbias/Vcc) unless Vpc supply current capability is less than 10 mA.

See table below for other Vpc logic level resistor values. See AN-064 if using other than Vcc=3.3V for Vpc resistors values.

4.9 - 5.9 GHz Evaluation Board Layout For Vcc = Vpc = V+ = 3.3V Supply

- Board material GETEK, 10mil thick, Dk=3.9, 2 oz. copper finish



DESG	DESCRIPTION
Q1	STA-6033
R1 *	909 OHM, 1% 0603
R2 *	1.10K OHM, 1%, 0603
R3 *	1.47K OHM, 1%, 0603
R4 *	47K OHM, 0603
C1	1uF 16V TANTALUM CAP
C2,6	0.1uF CAP, 0603
C3,4,5	1.8pF CAP, 0603
R5,6 *	0 OHM, 0603

* 0402 STYLE RESISTOR MAY BE USED

Resistor Table for Vcc=3.3V **

VPC(V)	R1(ohm)	R2(ohm)	R3(ohm)
2.9	165	249	215
3.0	357	464	511
3.1	562	665	825
3.2	750	887	1.13K
3.3	909	1.10K	1.47K

** See app note AN-064 for other Vcc and Vpc combinations

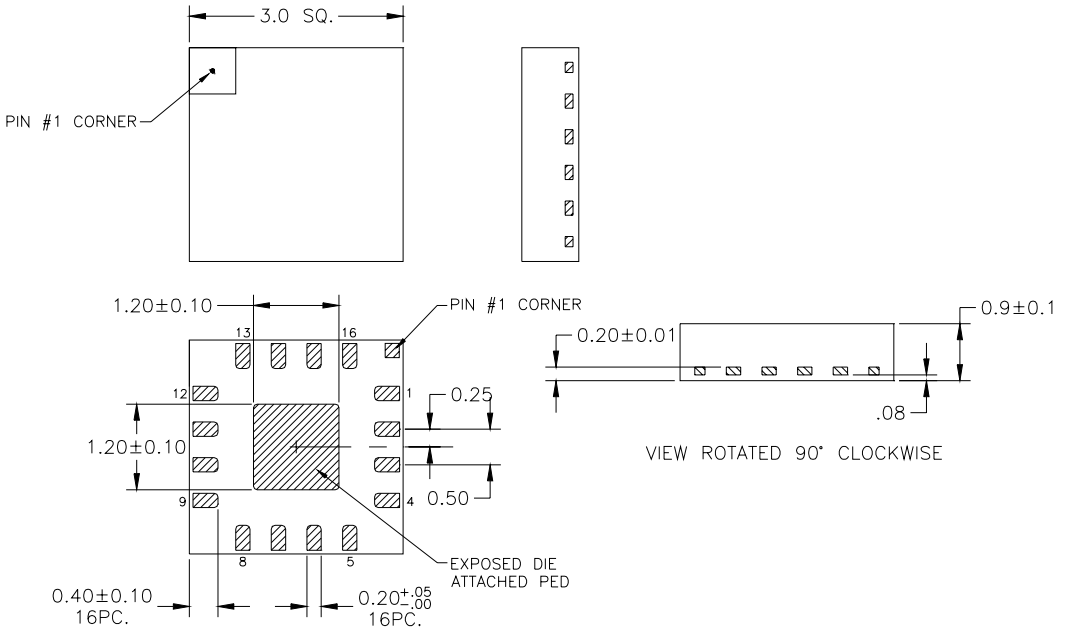
Part Number Ordering Information

Part Number	Reel Size	Devices/Reel
STA-6033	13”	3000

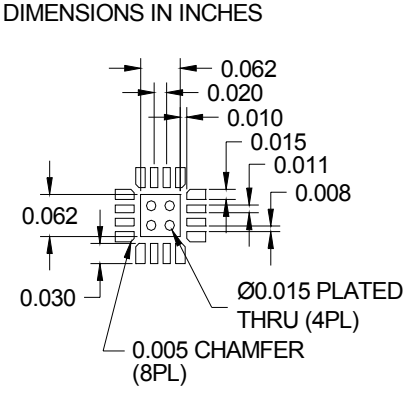
Part Symbolization

The part will be symbolized with an “STA-6033” marking designator on the top surface of the package.

Package Outline Drawing (dimensions in mm):



Recommended Land Pattern (dimensions in inches):



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