TS4985

2x1.2w Stereo Audio Power Amplifier with Dedicated Standby Pins

PRODUCT PREVIEW

- **Operating from V_{CC}=2.2V to 5.5V**
- **1.2W output power per channel @ V_{CC}=5V, THD+N=1%, RL=8Ω**
- **10nA standby current**
- **62dB PSRR @ 217Hz with Grounded inputs**
- **High SNR: 106dB(A) typ.**
- **Near Zero Pop & Click**
- **Lead-free 15 bumps flip-chip package**

Description

The TS4985 has been designed for top of the class stereo audio applications. Thanks to its compact and power dissipation efficient flip-chip package, it suits various applications.

With a BTL configuration, this audio power amplifier is capable of delivering 1.2W per channel of continuous RMS Output Power into an 8Ω load @ 5V.

Each output channel (Left and Right), has an external controlled standby mode pin (STDBYL&STDBYR) to reduce the supply current to less than 10nA per channel. The device also features an internal thermal shutdown protection.

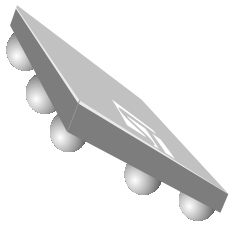
The gain of each channel can be configured by external gain setting resistors.

Applications

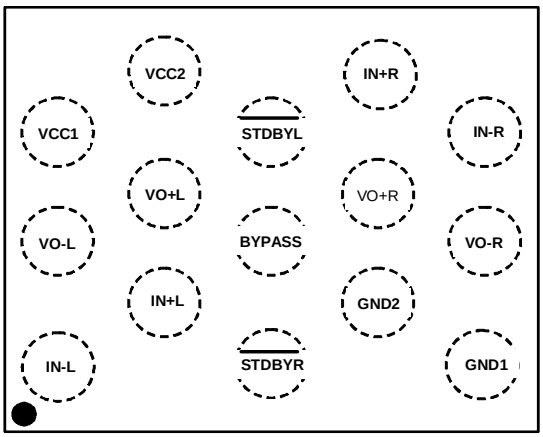
- **Cellular mobile phones**
- **Notebook & PDA computers**
- **LCD monitors & TVs**
- **Portable audio devices**

Pin Connections (top view)

Flip-Chip 15 bumps



Pin Connection (top view)



Order Codes

Part Number	Temperature Range	Package	Packaging	Marking
TS4985EIJT [1]	-40, +85°C	Flip-Chip	Tape & Reel	
TS4985EIKJT [2]				

1) ***E*** *= Lead-free Flip-Chip*

2) ***K*** *= Back coating option*

1 Application Diagram

Figure 1 : Typical application schematics

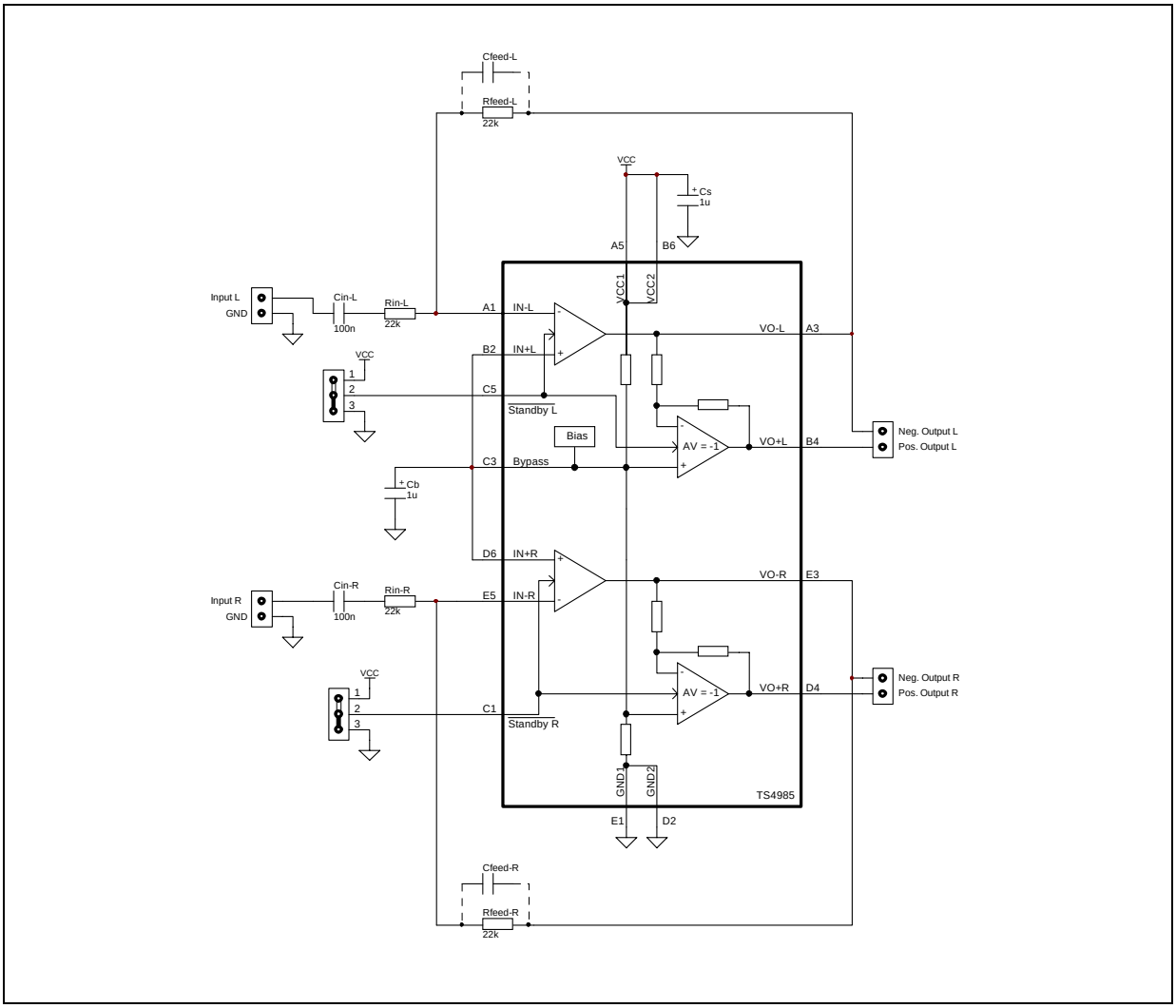


Table 1: External Component Descriptions

Components	Functional Description
$R_{IN\ L,R}$	Inverting input resistors which sets the closed loop gain in conjunction with Rfeed. These resistors also form a high pass filter with C_{IN} (fc = 1 / (2 x Pi x R_{IN} x C_{IN}))
$C_{IN\ L,R}$	Input coupling capacitors which blocks the DC voltage at the amplifier input terminal
$R_{FEED\ L,R}$	Feedback resistors which sets the closed loop gain in conjunction with R_{IN}
C_S	Supply Bypass capacitor which provides power supply filtering
C_B	Bypass pin capacitor which provides half supply filtering
$A_{V\ L,\ R}$	Closed loop gain in BTL configuration = 2 x (R_{FEED} / R_{IN}) on each channel

2 Absolute Maximum Ratings

Table 2: Key parameters and their absolute maximum ratings

Symbol	Parameter	Value	Unit
VCC	Supply voltage [1]	6	V
V_i	Input Voltage [2]	G_{ND} to V_{CC}	V
T_{oper}	Operating Free Air Temperature Range	-40 to + 85	°C
T_{stg}	Storage Temperature	-65 to +150	°C
T_j	Maximum Junction Temperature	150	°C
R_{thja}	Thermal Resistance Junction to Ambient	tba	°C/W
Pd	Power Dissipation	Internally Limited	
ESD	Human Body Model [3]	2	kV
ESD	Machine Model	200	V
	Latch-up Immunity	200mA	

1) All voltages values are measured with respect to the ground pin.

2) The magnitude of input signal must never exceed V_{CC} + 0.3V / G_{ND} - 0.3V.

3) All Voltage values are measured from each pin with respect to supplies.

Table 3: Operating Conditions

Symbol	Parameter	Value	Unit
VCC	Supply Voltage	2.2 to 5.5	V
V_{ICM}	Common Mode Input Voltage Range	1.2V to V_{CC}	V
VSTB	Standby Voltage Input: Device ON Device OFF	 $1.35 \le V_{STB} \le V_{CC}$ $GND \le V_{STB} \le 0.4$	V
RL	Load Resistor	≥ 4	Ω
ROUT-GND	Resistor Output to GND (V_{STB} = GND)	≥ 1	MΩ
TSD	Thermal Shutdown Temperature	150	°C
RTHJA	Thermal Resistance Junction to Ambient Flip Chip[1]	 tba	°C/W

1) When mounted on a 4-layer PCB.

3 Electrical Characteristics

Table 4: V_{CC} = +5V, GND = 0V, T_{amb} = 25°C (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
I_{CC}	Supply Current No input signal, no load		7.4	12	mA
$I_{STANDBY}$	Standby Current [1] No input signal, Vstdby = G_{ND}, RL = 8Ω		10	1000	nA
Voo	Output Offset Voltage No input signal, RL = 8Ω		1	10	mV
Po	Output Power THD = 1% Max, F = 1kHz, RL = 8Ω	0.9	1.2		W
THD + N	Total Harmonic Distortion + Noise Po = 1Wrms, Av = 2, 20Hz ≤ F ≤ 20kHz, RL = 8Ω		0.2		%
PSRR	Power Supply Rejection Ratio[2] RL = 8Ω, Av = 2, Vripple = 200mVpp, Input Grounded F = 217Hz F = 1kHz	 55 55	 62 64		dB
Crosstalk	Channel Separation, R_L = 8Ω F = 1kHz F = 20Hz to 20kHz		 tba tba		dB
T_{WU}	Wake-Up Time (Cb = 1µF)		90	130	ms
T_{STDB}	Standby Time (Cb = 1µF)		10		µs
V_{STDBH}	Standby Voltage Level High			1.3	V
V_{STDBL}	Standby Voltage Level Low			0.4	V
Φ_M	Phase Margin at Unity Gain R_L = 8Ω, C_L = 500pF		65		Degrees
GM	Gain Margin R_L = 8Ω, C_L = 500pF		15		dB
GBP	Gain Bandwidth Product R_L = 8Ω		1.5		MHz

1) Standby mode is activated when Vstdby is tied to Gnd.

2) All PSRR data limits are guaranteed by production sampling tests
Dynamic measurements - 20*log(rms(Vout)/rms(Vripple)). Vripple is the sinusoidal signal superimposed upon Vcc.

Table 5: V_{CC} = +3.3V, GND = 0V, T_{amb} = 25°C (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
I_{CC}	Supply Current No input signal, no load		6.6	12	mA
$I_{STANDBY}$	Standby Current [1] No input signal, Vstdby = G_{ND}, RL = 8Ω		10	1000	nA
Voo	Output Offset Voltage No input signal, RL = 8Ω		1	10	mV
Po	Output Power THD = 1% Max, F = 1kHz, RL = 8Ω	375	500		mW
THD + N	Total Harmonic Distortion + Noise Po = 400mWrms, Av = 2, 20Hz ≤ F ≤ 20kHz, RL = 8Ω		0.1		%
PSRR	Power Supply Rejection Ratio[2] RL = 8Ω, Av = 2, Vripple = 200mVpp, Input Grounded F = 217Hz F = 1kHz	 55 55	 61 63		dB
Crosstalk	Channel Separation, R_L = 8Ω F = 1kHz F = 20Hz to 20kHz		 tba tba		dB
T_{WU}	Wake-Up Time (Cb = 1µF)		110	140	ms
T_{STDB}	Standby Time (Cb = 1µF)		10		µs
V_{STDBH}	Standby Voltage Level High			1.2	V
V_{STDBL}	Standby Voltage Level Low			0.4	V
Φ_M	Phase Margin at Unity Gain R_L = 8Ω, C_L = 500pF		65		Degrees
GM	Gain Margin R_L = 8Ω, C_L = 500pF		15		dB
GBP	Gain Bandwidth Product R_L = 8Ω		1.5		MHz
GBP	Gain Bandwidth Product R_L = 8Ω		1.5		MHz

1) Standby mode is activated when Vstdby is tied to Gnd.

2) All PSRR data limits are guaranteed by production sampling tests
Dynamic measurements - 20*log(rms(Vout)/rms(Vripple)). Vripple is the sinusoidal signal superimposed upon Vcc.

Table 6: V_{CC} = +2.6V, GND = 0V, T_{amb} = 25°C (unless otherwise specified)

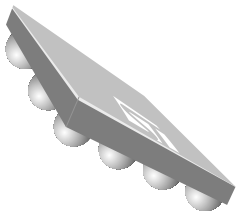
Symbol	Parameter	Min.	Typ.	Max.	Unit
I_{CC}	Supply Current No input signal, no load		6.2	12	mA
$I_{STANDBY}$	Standby Current [1] No input signal, Vstdby = G_{ND}, RL = 8Ω		10	1000	nA
Voo	Output Offset Voltage No input signal, RL = 8Ω		1	10	mV
Po	Output Power THD = 1% Max, F = 1kHz, RL = 8Ω	220	300		mW
THD + N	Total Harmonic Distortion + Noise Po = 200mWrms, Av = 2, 20Hz ≤ F ≤ 20kHz, RL = 8Ω		0.1		%
PSRR	Power Supply Rejection Ratio[2] RL = 8Ω, Av = 2, Vripple = 200mVpp, Input Grounded F = 217Hz F = 1kHz	 55 55	 60 62		dB
Crosstalk	Channel Separation, R_L = 8Ω F = 1kHz F = 20Hz to 20kHz		 tba tba		dB
T_{WU}	Wake-Up Time (Cb = 1µF)		125	150	ms
T_{STDB}	Standby Time (Cb = 1µF)		10		µs
V_{STDBH}	Standby Voltage Level High			1.2	V
V_{STDBL}	Standby Voltage Level Low			0.4	V
Φ_M	Phase Margin at Unity Gain R_L = 8Ω, C_L = 500pF		65		Degrees
GM	Gain Margin R_L = 8Ω, C_L = 500pF		15		dB
GBP	Gain Bandwidth Product R_L = 8Ω		1.5		MHz

1) Standby mode is activated when Vstdby is tied to Gnd.

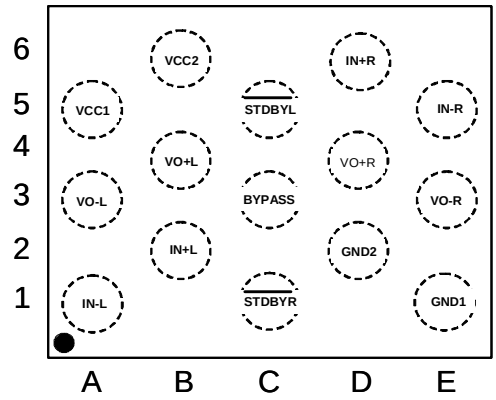
2) All PSRR data limits are guaranteed by production sampling tests
Dynamic measurements - 20*log(rms(Vout)/rms(Vripple)). Vripple is the sinusoidal signal superimposed upon Vcc.

4 Package MechanicaL Data

4.1 TS4985EIJT Pinout and Package Mechanical Data

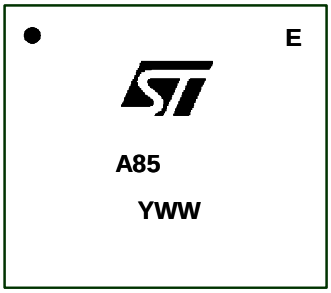


4.1.1 Pinout (top view)



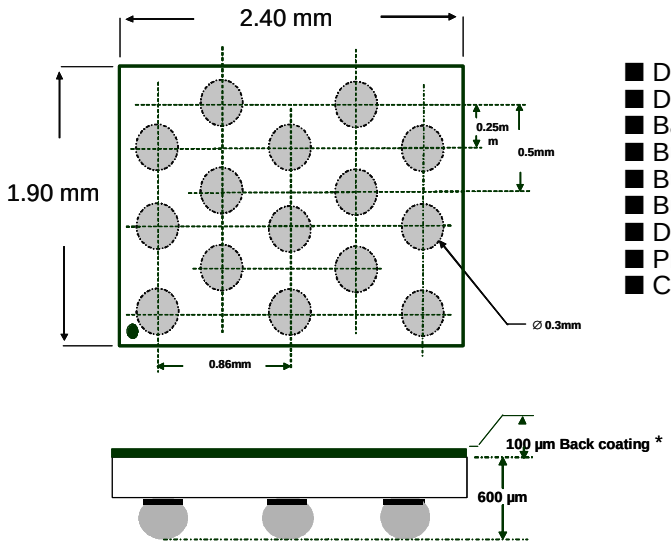
■ Balls are underneath

4.1.2 Marking (top view)



■ ST Logo
■ Part number: A85
■ Three digits Datecode: YWW
■ E symbol for lead-free
■ The dot is for marking pin A1

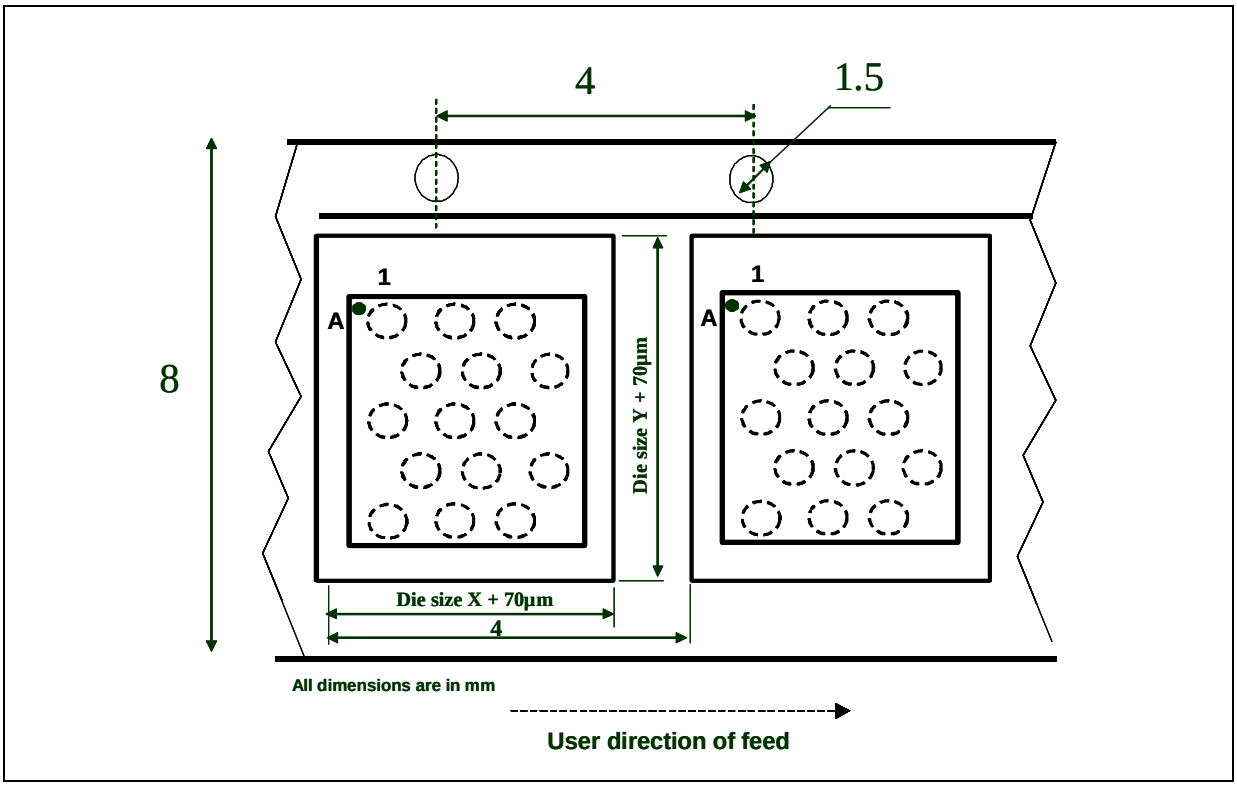
4.1.3 Package mechanical data for 15-bump flip-chip



■ Die size: **2.40 x 1.90 mm ±30µm**
■ Die height (including bumps): **600µm**
■ Back Coating height(optional): **100µm**
■ Bump Diameter: **315µm ±50µm**
■ Bump Diameter Before Reflow: **300µm ±10µm**
■ Bump Height: **250µm ±40µm**
■ Die Height: **350µm ±20µm**
■ Pitch: **500µm ±50µm**
■ Coplanarity: **60µm max**.

* Optional

4.1.4 Tape & reel specification (top view)



5 Revision History

Date	Revision	Description of Changes
01 Nov 2004	1	First Release